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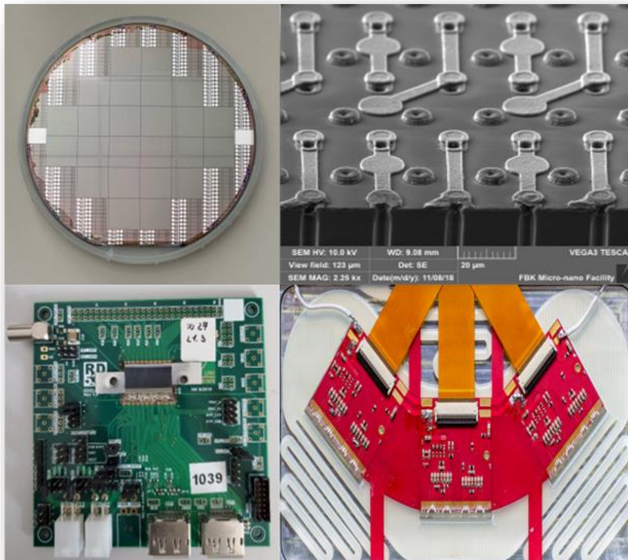
Characterization of 3D Silicon Pixel Detectors for the ATLAS ITk

Md Arif Abdulla Samy



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This work is dedicated to my mother, Mrs. Sajeda Aktheri, who fought for me always, waiting for my work to finish until she could, and finally went to her permanent residence to answer the call from her creator, to whom she always prayed for my success.

Abstract

After ten years of massive success, the Large Hadron Collider (LHC) at CERN is going for an upgrade to the next phase, The High Luminosity Large Hadron Collider (HL-LHC) which is planned to start its operation in 2029. This is expected to have a fine boost to its performance, with an instantaneous luminosity of 5.0×10^{34} $cm^{-2}s^{-1}$ (ultimate value 7.5×10^{34} $cm^{-2}s^{-1}$) with 200 average interactions per bunch crossing which will increase the fluences up to more than 10^{16} n_{eq}/ cm^2, resulting in high radiation damage in ATLAS detector. To withstand this situation, it was proposed to make the innermost layer with 3D silicon sensors, which will have radiation tolerance up to 2×10^{16} n_{eq}/cm^2 with a Total Ionization Dose of 9.9 MGy. Two-pixel geometries have been selected for 3D sensors, 50 × 50 μm^2 for Endcap (ring), which will be produced by FBK (Italy) and SINTEF (Norway), and 25 × 100 μm^2 for Barrel (stave), will be produced by CNM (Spain). A discussion is made in this thesis about the production of FBK on both geometries, as they have made a breakthrough with their Stepper lithography process. The yield improved, specifically for the geometry 25 × 100 μm^2 with two electrode readouts, which was problematic in the mask aligner approach. Their sensors were characterized electrically at wafer-level as well as after integration with RD53a readout chip (RoC) on single-chip cards (SCC) and were verified against Innermost Tracker criteria. The SCCs were sent for irradiation up to 1×10^{16} n_{eq}/cm^2 and were tested under electron test beam, and a hit efficiency of 97% was presented. Some more SCCs have been sent to Los Alamos for irradiating them up to 1.5×10^{16} n_{eq}/cm^2 fluence. As the 3D sensors will be mounted as Triplets, a discussion is also made on their assembly and QA/QC process. A reception testing and electrical testing setup both at room temperature and the cold temperature was made and discussed, with results from some early RD53a RoC-based triplets. The pre-production sensors are already evaluated, and soon they will be available bump-bonded with ITkPixV1 RoC for further testing.

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Chapter 1
Introduction

Since the first phase of the Large Hadron Collider (LHC) is going to end soon, and the second phase, the High Luminosity Large Hadron Collider (HL-LHC) is being planned to start in 2029, all the major parts of the detectors need to get upgraded for the ATLAS and CMS experiments. It is estimated and simulated that the front-end electronics will be required to undergo a very harsh environment with an estimated total ionizing dose (TID) of 1 Grad and 1 MeV neutron equivalent fluence of 2×10^{16} cm^{-2} accumulated during the lifetime of the experiments, and hit rates of the order of 3 GHz/cm^2. In this high luminosity environment, which will reach 5×10^{34} $cm^{-2}s^{-1}$, it is expected to get a yield as high as 200 events/bunch crossing. To cope with this scenario, it was decided that the ATLAS Inner Tracker (ITk), which will be replacing the ATLAS Inner Detector, will be an all-silicon tracker consisting of an outer part made from silicon strip modules and an inner part made from silicon pixel modules. To mitigate the requirements, the target pixel size should be either 50 µm × 50 µm or 25 µm × 100 µm, to maintain the occupancy at the percent level and improve spatial resolution, with a power budget close to 0.5 W/cm^2. Maintaining that, a framework named RD53 collaboration has come up with an advanced pixel Read-Out Chip (ROC) prototype called RD53A with 65 nm CMOS technology. This technology is very promising to have a good radiation tolerance property both for analog and digital circuits, enabling the integration of dense in-pixel digital functions and need to comply with the bandwidth requirement of 1.28 Gb/s. The final design for the ATLAS ITk (RD53B or ITkPix) will consist of pixels size 50 µm × 50 µm arranged as 400 columns and 384 rows, resulting in an active pixel matrix of 20 mm × 19.2 mm. The chip width is between 20.996 mm and 21.176 mm. The estimate of the final physical chip size is 20.086 ± 0.04 mm × 21.086 ± 0 .09 mm.

For tracking applications in High Energy Physics (HEP) investigations, 3D silicon pixel detectors are the most radiation-hard technology [3]. Following their successful usage in the ATLAS Insertable B-Layer [166], 3D pixels were applied to the trackers of the AFP [199] and CT-PPS [200] detectors of ATLAS and CMS experiments, and

they naturally became candidates for the innermost tracking layers of the ATLAS and CMS detector upgrades at the HL-LHC [176].

Aside from radiation hardness, another attribute of 3D pixels that is inherent in their structure is exceptionally rapid signaling [201]. This characteristic, which has not yet been completely utilized, has the potential to improve timing performance, which is needed to overcome the challenge of high track density in detectors for future experiments at particle colliders. Recent research has shown that small-pitch 3D pixels may provide excellent timing resolution (~30 ps), despite non-uniformities in the electric field and weighting field distributions inside a pixel [181]. To increase timing performance even further, other designs with trenched electrodes are being developed [182], and preliminary results (~20 ps) [177] are highly promising.

To meet the ever-increasing criteria for occupancy, radiation hardness, and timing, all modern 3D pixel designs have in common the necessity for lower pixel sizes and thinner active layers, resulting in a dramatic downscale of all geometrical dimensions as compared to prior generation devices. Depending on the electrode design, this might result in dense pixel patterns that are difficult to print with a sufficient yield. The minimum feature size and alignment precision that can be achieved with a mask aligner operated in proximity mode are a few micrometers, making it unsuitable for the most complicated layouts. The stepper available at FBK, on the other hand, has a minimum feature size of 350 nm and an alignment precision of 80 nm, which is enough for the geometries under consideration.

The group working at the University of Trento (UniTN) has been active in the field of 3D radiation sensors for many years, contributing to the development of different generations of 3D pixels in collaboration with FBK. Since 2014, in the framework of a joint ATLAS-CMS effort funded by INFN, the group has been responsible for the design of small-pitch, thin 3D pixels for the HL-LHC upgrades. Besides the usual device-oriented activities (layout, TCAD simulations, electrical measurements, etc.), in the past few years, the group has started to be involved in module-related activities, in view of the ITk production phase. This Ph.D. thesis is aimed at the

development and optimization of small-pitch 3D pixel sensors for the ATLAS ITk, with emphasis on the functional characterization of modules based on the RD53A ROC.

This thesis is organized as follows:

Chapter 2 introduces some basics of silicon radiation detector theory, how the p-n junction works, the classification of detectors, their mechanism of them, how the detector electronics work, what is radiation damage and what is meant by radiation hardness.

Chapter 3 includes a brief discussion about the ATLAS detector, its upgrade to HL-LHC, future plans, new requirements, new design, and mechanism.

Chapter 4 is about 3D sensors, covering simulations, historic upgrades, and experimental results of different generations. Design evaluation of the 3D DDTC sensor for the insertable B layer, which is the state-of-the-art technology is discussed here.

Chapter 5 reports on the new design of small pitch 3D sensors using stepper lithography in FBK, technological overview, and layout, design, comparison between mask aligner and stepper process, and electrical characteristics at the wafer level.

Chapter 6 is devoted to the characterization of 3D pixel modules based on the RD53A readout chip. Electrical characterization at the sensor level and module level is discussed along with data acquisition system setup. Results from different modules are presented and discussed before and after irradiation, along with signal efficiency from the test beam.

Chapter 7 reports on the assembly procedure of 3D triplet modules, the dimensions of the module, and assembly steps. QA/QC process steps, setups, and results from some modules are also presented and discussed here.

Chapter 2
3D Silicon Radiation Detectors

2.1 Silicon Radiation Detectors

2.1.1 Silicon as a detector material

Silicon detectors work in theory as ionizing chambers. The simplest structure one can imagine entails an absorbing medium sandwiched in the middle of two metal electrodes, making either ohmic or Schottky contact with the semiconductor. A signal is induced on the electrodes as the electron-hole pairs produced by radiation are separated by an electric field and drift to the electrodes. To be differentiated, signals should be large enough to equate to noise; thus, a high signal-to-noise ratio (SNR) is essential. This, however, can lead to two contradictory constraints: on one hand, to have a large signal, radiation should produce many electron-hole pairs, and this would involve low-ionization energy, hence a small band gap. On the other hand, to have minimal noise, there should be few intrinsic charge carriers, which is feasible only with large band gaps. As an example, in intrinsic silicon substrates, with the size of a typical silicon sensor (1 cm^2 area, 300 μm thickness), there are $\sim 4\times10^8$ electron-hole pairs at room temperature, whereas a Minimum Ionizing Particle (MIP) would normally generate only $\sim 2\times10^4$ electron-hole pairs. The signal would be entirely lost in this higher number of free-charge carriers. It is thus crucial to reduce the number of free-charge carriers by numerous orders of magnitude. In theory, for silicon and other small band-gap semiconductors, this can be acquired by cooling, since the intrinsic concentration exponentially depends on the temperature [1]. Nevertheless, the most efficient solution is to create a p-n junction and operate it in full depletion condition. On the contrary, wide band-gap semiconductors have a much higher resistivity, that is, a much lower intrinsic concentration (e.g., 10^{-27} cm^{-3} in diamond). As a result, they can be operated at room temperature with ohmic or Schottky contacts.

2.1.2 p-n junction

The simplest structure for a radiation sensor starts from the p-n junction. Two silicon regions, respectively doped with acceptor atoms (or positively doped) on one side

and with donor atoms (or negatively doped) on the other side, are joined together. The positively doped region is called the p-side (anode), and the negatively doped region is called the n-side (cathode). Due to the enormous concentration discrepancy of charge carriers between the two regions, electrons will diffuse across the junction, leaving a positive charge in the n-side region, and holes will diffuse leaving a negative charge in the p-side region. As a result, a region free of mobile charges is created throughout the junction, called the space charge region (SCR) or Depletion region, as can be seen in fig 2.1.

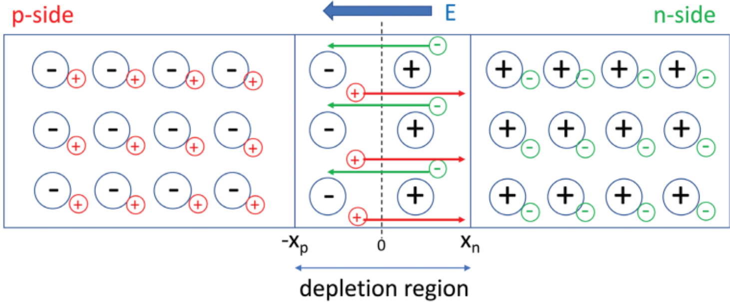


Fig 2.1: Schematic of a p-n junction in silicon material.

Due to the distributions of fixed donor and acceptor ions, an electric field is formed across the SCR, which counteracts further diffusion of holes and electrons through the junction. This electric field is related to the Built-in potential (V_{bi}), which depends on the doping level of the two regions.

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right) \quad (2.1)$$

Where N_a is the acceptor concentration of the p-side region, N_d is the donor concentration in the n-side region, n_i is the intrinsic concentration in silicon, T is temperature, q is the charge of electron and k_B is the Boltzmann constant. Assuming a one-dimensional abrupt junction approximation, it is possible to extract the electric field and electrostatic potential distributions across the junction by sequential integrations of Poisson's equation [1].

$$\frac{d^2\varphi}{dx^2} = -\frac{\partial E}{\partial x} = -\frac{\rho(x)}{\varepsilon_0 \varepsilon_{si}} \quad (2.2)$$

Where φ is the electrostatic potential, E is the electric field, $\rho(x)$ is the charge density, and ε_{si} is the dielectric constant of silicon (~1 pF/cm). To solve the differential equation, boundary conditions come from the continuity of the electric field and the electric potential, as well as from the charge neutrality of the p-n junction, as expressed by equation 2.3:

$$N_a x_p = N_d x_n \quad \text{.......................................(2.3)}$$

Where x_p and x_n are the widths of the depletion regions in the p- and n-side of the junction, respectively. The total depletion width (w_{depl}) can be determined by equation 2.4:

$$w_{depl} = x_p + x_n = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}(N_a+N_d)}{qN_aN_d}V_{bi}} \quad \text{..........................(2.4)}$$

As normally one side of the junction is much more strongly doped than the other side, the depletion region will expand dominantly only on the side where the doping concentration is lower. As an example, presuming an n-type bulk material, Eqn. 2.4 can be simplified and written as:

$$w_{depl} \cong x_n = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}}{qN_d}V_{bi}} \qquad (N_a \gg N_d) \quad \text{..............(2.5)}$$

To detect charges generated by radiation, it is essential to fully deplete the bulk of the detector. Depletion can be attained by utilizing a peripheral potential to the junction, in the identical route as the built-in potential, to additionally eliminate charge carriers and expand the SCR width to the complete device thickness. The electric field, the width of the depleted layer, and the electrostatic potential distributions as functions of the applied bias voltage (V_{bias}) can still be obtained from the integral of Poisson's equation. In specific, the width of the depletion layer can be computed with the help of equation 2.6:

$$w_{depl} = x_p + x_n = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}(N_a+N_d)}{qN_aN_d}(V_{bi} + V_{bias})} \quad \text{....................(2.6)}$$

Again, considering the divergence in the doping levels and the fact that the built-in potential is usually significantly smaller than the outwardly utilized voltage, presuming an n-type bulk material it is feasible to simplify eqn. 2.6 as follows:

$$w_{depl} \cong x_n = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}}{qN_d}V_{bias}} \qquad (N_a \gg N_d) \quad \text{...............(2.7)}$$

The full depletion voltage (V_{fd}) is the bias voltage required to expand the SCR to the entire thickness of the silicon substrate (d). Under the same simplifying assumptions used in eqn. 2.7, it can be written as:

$$V_{fd} \cong \frac{qN_d d^2}{2\varepsilon_0\varepsilon_{si}} \quad \text{.....................................(2.8)}$$

The full depletion voltage is immediately proportional to the doping concentration of the bulk. To sustain a reasonable value of V_{fd}, it is necessary to use high-resistivity silicon as a starting material. Moreover, it should also be emphasized that V_{fd} is immediately proportional to the square of the sensor thickness, which should hence be limited to a few hundred micrometers to keep V_{fd} acceptably small. When the applied bias voltage exceeds the full depletion voltage, the device is said to be over-depleted. One of the most critical parameters of a p-n junction in reverse bias is its capacitance, which can approximately be presumed to be the same as a parallel-plate capacitor with a silicon dielectric of thickness equal to the depletion region width, as can be better understood by following equation 2.9:

$$C_d = A_d \frac{\varepsilon_0\varepsilon_{si}}{w_{depl}} = A_d \sqrt{\frac{qN_d\varepsilon_0\varepsilon_{si}}{2(V_{bi}+V_{bias})}} \quad \text{..........................(2.9)}$$

Where A_d is the diode area. From equation 2.9, we can see the capacitance is inversely proportional to the square root of the bias voltage until it saturates to a minimum (C_{fd}) as full depletion is reached, which leads to the equation:

$$C_{fd} = A_d \frac{\varepsilon_0\varepsilon_{si}}{d} \quad \text{.................................(2.10)}$$

From these equations, it can be understood that measuring the device's capacitance is an effective way to estimate the full depletion voltage. Another essential parameter for the p-n junction in reverse bias is the leakage current (or dark current), which is very low as compared to the diffusion current in forwarding bias. The leakage current (I_{lk}) has multiple components, as illustrated in Fig. 2.2 and summarized in Eqn. 2.11.

$$I_{lk} = I_{gen} + I_{diff} + I_{surf} \quad \text{..............................(2.11)}$$

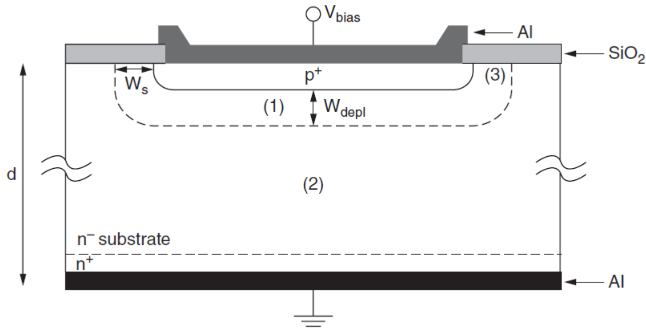


Fig 2.2: Schematic diagram of a reverse-biased silicon diode showing different contributions to the leakage current.

The generation current (I_{gen}) comes from the thermal generation of charge carriers within the depletion region, and can be written as:

$$I_{gen} = \frac{A_d q n_i w_{depl}}{\tau_g} \quad \text{.................................(2.12)}$$

Where q is the electron charge and τ_g is the generation lifetime. The thermal generation current is directly proportional to the width of the depletion region, so it increases with the square root of the bias voltage until saturation occurs at full depletion. It should be emphasized that thermal generation and recombination in silicon are described by Shockley–Read–Hall (SRH) statistics [1] that use localized energy levels within the band gap, due to lattice defects or unwanted impurities (e.g., Au, Cu, Fe). The density and the energy of these deep-level states directly influence the carrier lifetimes, calling for a very high substrate purity and quality of the fabrication process in order to minimize thermal generation.

The diffusion current contribution to the leakage current (I_{diff}) comes from the diffusion of the minority carriers from the quasi-neutral region to the depletion region. With respect to holes in an n-type bulk, it can be written as:

$$I_{diff} = \frac{A_d q n_i^2 D_p}{N_d L_p} \quad \text{.....................................(2.13)}$$

Where D_p is the diffusion coefficient of holes and L_p is the diffusion length of holes, which in turn can be written as:

$$L_p = \sqrt{D_p \tau_p} \quad \text{.......................................(2.14)}$$

Where τ_p is the recombination lifetime of holes. In the case of high-purity silicon, the diffusion length can be very high (∼1 cm), resulting in a very low diffusion current. However, diffusion current is sometimes non-negligible since the other components of the leakage currents are expected to be very low as well.

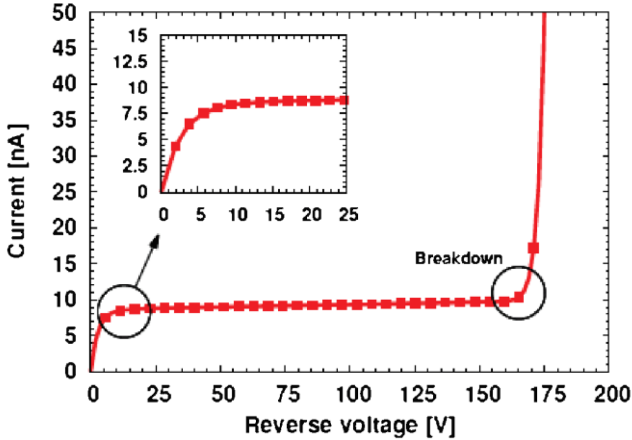


Fig 2.3: A generic Current-Voltage (I-V) of a silicon diode in reverse biased condition.

The last component of the leakage current, the surface current (I_{surf}) is due to the generation of carriers at the depleted surface beneath the SiO_2 passivation layer. It can be written as:

$$I_{surf} = qn_i s_0 P_d w_s \quad \text{....................................(2.15)}$$

Where s_0 is the surface generation velocity, P_d is the diode perimeter, and w_s is the lateral extension of the depletion region at the surface. In most situations of practical interest, w_s is much smaller than w_{depl}, because of oxide charges. Therefore, apart from some device geometries where the perimeter is relatively long (e.g., in strip sensors), the leakage current is governed by thermal generation in the depleted bulk. The latter is strongly dependent on the temperature through both n_i and τ_g. This phenomenon indicates operating the device in a cool environment in order to decrease the leakage current, especially after irradiation. The leakage current at temperature T_2 can be predicted with reference to the leakage current at temperature T_1 by the following equation [2]:

$$\frac{I(T_2)}{I(T_1)} = (\frac{T_2}{T_1})^2 \exp[-\frac{E_{eff}}{2k_B}(\frac{1}{T_2} - \frac{1}{T_1})] \quad \text{..........................(2.16)}$$

Where k_B is the Boltzmann's constant and E_{eff} is the effective band gap (∼1.21 eV). As a rule of thumb, it can be assumed that the current doubles every 7 °K [3]. The p-n junction in reverse bias can be conducted at a large voltage up to the breakdown point, beyond which the current shows an abrupt increase, as seen in fig 2.3. The breakdown mechanism can be constrained by three effects: avalanche multiplication, thermal runaway, and tunneling. Avalanche multiplication is the most important mechanism for junction breakdown in p-n junctions utilized for radiation detection. Carrier multiplication occurs when the electric field is high enough for the kinetic energy of carriers to grow to such an extent that they can shatter the covalent bond of an additional electron in the silicon lattice by colliding with it. This event is called impact ionization, and it leads to the generation of a new electron-hole pair [1]. In silicon, the critical electricity for avalanche multiplication at room temperature is $\approx 4 \times 10^5$ V/cm. If the electric field is high enough, the avalanche effect can be self-sustained, triggering a large increase in the leakage current of the device. If the bias voltage is also extremely high, the power developed in the sensor (P = VI) can be adequate to cause an uncontrollable self-heating mechanism, also known as thermal runaway. To counteract this phenomenon, which could eventually destroy the device, an effective cooling scheme is required. At even larger fields, of the order of 10^6 V/cm, band-to-band tunneling effects could take place, leading to a very high current, but this involves both sides of the junctions to be highly doped, that is not the case with silicon radiation sensors.

2.2 Position-Sensitive Sensors

The position of the incident radiation is a crucial requirement for many applications, especially, in the case of silicon detectors used for tracking elementary particles in high-energy colliders. P-N junctions can be organized in many ways to form simple diode or finely segmented structures, allowing position sensing of the incident particle, such as microstrip or pixel geometries.

2.2.1 Pad Detector or Diode

The simplest sensor structure is a diode, also known as a pad detector. A pad is made on a high-resistivity substrate with a wide range of feasible thicknesses (from some tens of micrometers to a few millimeters). With reference to an n-type substrate, one side of the detector is p^+ doped (junction), and the other side is n^+ doped (ohmic contact), while the bulk is of a (quasi) intrinsic type (hence the name P-I-N diode). Ultrapure silicon ingots obtained from floating-zone (FZ) refinement have bulk resistivity in the range from 1.0 to 30 kΩ cm. As simple diodes, p-n junctions are generally reverse biased, so that electron-hole pairs generated inside the depletion region are stripped away from the SCR and are collected at the p^+ and n^+ contacts. When driven in full depletion mode, the drift velocity of charge carriers is restricted only by the saturation drift velocity of electrons and holes, that is, about 10^7 cm/s in silicon. As a result, the reaction time of a fully depleted silicon detector can be of the order of a few nanoseconds. In reality, not all the created carriers are always collected at the p^+ and n^+ contacts. Some of them could be lost because of aggressive processes such as charge trapping and recombination. Outside the SCR, electron-hole recombination is prevalent, and carrier transport is based on diffusion. Therefore, ionization events happening in the nondepleted regions can contribute to detector efficiency, but they rise the response time. According to equation 2.8, depending on the substrate doping concentration and thickness, it seems that large bias voltages might be essential to fully deplete a P-I-N detector. As an example, a diode made on a standard 300 µm thick substrate with a doping concentration of 10^{12} cm^{-3} has a full depletion voltage of 70 V. The only way to withstand these high voltages, while preserving low reverse leakage currents and avoiding breakdown problems, are (1) to have a very good fabrication technology, able to guarantee carrier lifetime of the order of milliseconds without demeaning the ultrapure starting material, and (2) to optimize the detector layout.

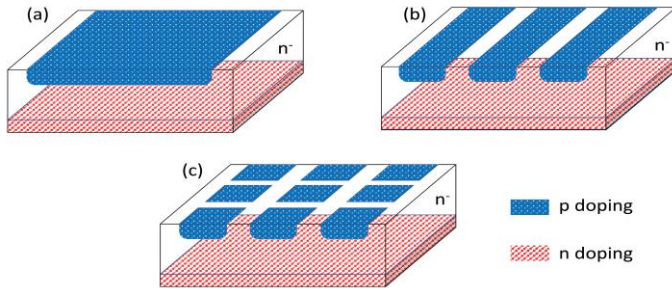


Fig 2.4: Generalize structure of (a) Pad detector, (b) Strip sensor with three strips, and (c) Pixel detectors with six pixels.

2.2.2 Strip Sensors

Another possible sensor structure is the Strip detector, as shown in fig. 2.4 (b). With respect to pad sensors, instead of having a single collection electrode, the anode is segmented in many microstrips a few tens of micrometers wide and up to a few centimeters long. All microstrips are biased at the same reverse voltage, since the charge generated inside the detector by the radiation is not completely localized, the pulse signal can be dispersed out over two or more adjacent strips. In theory, each microstrip should be linked to an electronic readout channel. In this way, a spatial resolution of a few tens of micrometers or better can be attained, depending on the strip pitch and readout mode. In more developed designs, the rear end of the wafers (ohmic side) is also segmented in microstrips at the cost of a significant increase in technological complexity. With respect to those on the junction side, the strips on the ohmic side can be either orthogonal or just rotated by a tiny angle, which is called the stereo configuration. By performing this, 3D devices are attained, with a fine pixel granularity resolution in the x-y direction and 200–300 μm in the z coordinate. On the other hand, it should be underlined that double-sided microstrip sensors are not suitable for high-particle-rate environments. In case they impose on the detector at the identical time, two pairs of particles could fire two identical pairs of strips, though their hit position is different, as can be seen in fig 2.5. Another drawback of microstrip sensors is their superior capacitance, which imposes the use of very minimal noise preamplifiers. In fact, because of the vicinity of electrodes to each other (a few tens of μm at most), the capacitance of every strip is much greater than

that of a simple diode, where the two electrodes are at a space that corresponds to the substrate thickness. The capacitance of a strip electrode is produced by two contributions: the inter-strip capacitance, which depends largely on the strip pitch (but also on other design constraints, like the field plate, and the oxide charge), and the strip-to-back capacitance, which varies with the substrate thickness. In planar microstrip sensors, the initial contribution to the capacitance is by far the most important, due to the peculiar strip aspect ratio. The major advantage of strip sensors is the likelihood of achieving detectors with a very large active area (tens of cm^2) while maintaining a very good position resolution, making this type of sensor a mainstay for tracking in high-energy physics and nuclear physics.

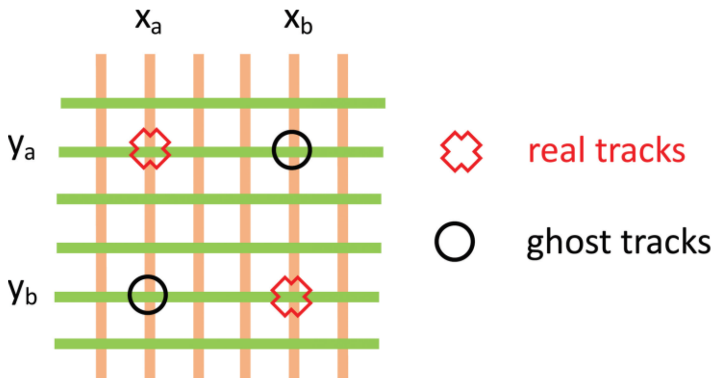


Fig 2.5: The problem of ghost tracks in double-sided strip sensors in case of high hit rates.

2.2.3 Pixel Sensors

The most complex structure in the case of silicon sensors is the Pixel geometries as seen in fig 2.4 (c), which add further complexity in efforts to obtain a "true" two-dimensional position resolution of the incident particle without obscurities in case of high particle rates. Depending on the precise configuration, pixel sensors are engineered with either a single-sided (p-on-n, n-on-p) or a double-sided process (n-on-n, while p-on-p is rarely used). Electrodes are organized as small, embedded regions on the silicon area mimicking a checkerboard. The plainest pixel shape is a square, but rectangular pixels are frequently used, and hexagonal pixels can also be applied. The main concern of pixel systems is the readout of every single channel,

which involves complex and pricey interconnect methods, like bump bonding and flip-chipping [4]. The pixel layout should be devised to flawlessly match the layout of the readout chip. The resulting sensors are usually referred to as hybrid pixel detectors. The chip is classically connected to the sensor through slight solder bumps. The main restriction to the pixel size typically comes from the electronics as a large number of circuit functions have to be fit in a single pixel, with complexity altering depending on the type of readout to be executed. Pixel detectors are applied mostly as vertex detectors in high-energy physics experiments, but they are also very fascinating and are finding their way into imaging in medical applications.

2.2.4 Drift Detectors

The silicon drift detector (SDD), also called the semiconductor drift chamber, was primarily recommended by Gatti and Rehak in 1984 [5, 6]. It is a device produced on high-resistivity n-type silicon wafers with mending p-n junctions implanted on both sides. The detector is fully depleted of mobile charges by utilizing a suitable reverse voltage to the p-n junctions on both sides of the wafer. An electrostatic potential parallel to the surface is then overlaid onto the depleting vertical potential by means of resistive voltage dividers. Fig. 2.6, shows the basic operating mechanism with a schematic view of a drift detector: while holes are brushed away by the p^+ electrodes close to the point of interaction, electrons generated inside the volume of the detector are drifted along the lowermost of the potential valley toward one small collecting anode, where they lastly induce a signal. The number and position of the anodes can be different depending on the application. The most used for spectroscopic applications, the cylindrical SDD, has only one anode placed at the center of the detector area, surrounded by several rings of cathodes. The drift time of electrons processes the radial coordinate of the interaction point since the electric field and the drift velocity are known. The drift time for a detector that is a few millimeters wide is in the order of microseconds, and the radial position resolution that can be attained is less than 10 μm. SDDs of the "linear" type, having two-dimensional position resolution, usually used for tracking applications, can also be attained and exploit the same basic mechanism (drift time) as cylindrical SDDs for

the resolution in the first dimension, whereas the resolution on the second dimension is attained by fragmenting the anode in several adjacent pixel anodes [7].

The key benefit of silicon drift detectors is that the anode capacitance is much lesser than that of typical junction detectors of similar dimensions. Therefore, the electronic system noise can be decreased to a much lower level, and the detector can function with greater energy resolution and at lower shaping times [8]. A drawback of SDDs is the somewhat complex bias electronic circuitry required to allocate the longitudinal potential among all the p^+ electrodes. The peripheral biasing circuitry can be averted by using an integrated voltage divider, comprising of either implanted resistors or MOS transistors [9].

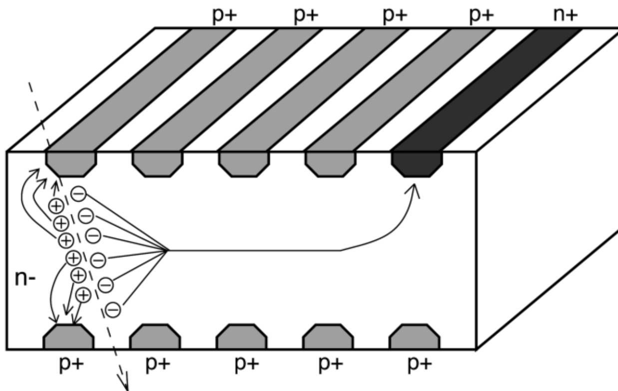


Fig 2.6: Schematic view of a silicon drift detector and its operation.

2.3 Signal Formation

2.3.1 Charge motion inside silicon

The interaction of ionizing radiation with silicon eventually leads to the formation of a certain number of electron-hole pairs. The movement of charge carriers within the sensor volume is dictated by the drift length (L_{drift}) and by the diffusion length (L_{diff}) in the depleted and nondepleted regions, correspondingly. When these lengths are sufficiently long, the charge signal comes to be mostly independent of the incident point of absorption inside the detector-sensitive volume. The relation between drift length and other parameters can be defined by the following equation:

$$L_{drift} = v\tau \text{ ....(2.17)}$$

Where v is the drift velocity and τ is the lifetime. In turn, the drift velocity can be expressed as:

$$v = \mu E \text{ ....(2.18)}$$

Where μ is the mobility and E is the magnitude of the electricity. However, at high fields ($\sim 10^5$ V/cm), the velocity overwhelms to a value of $\sim 10^7$ cm/s for both electrons and holes. The diffusion length is correlated to other physical parameters, and can be expressed as:

$$L_{diff} = \sqrt{D\tau} \text{ ....(2.19)}$$

where D is the diffusion coefficient, which is proportional to the mobility as stated by Einstein's relation:

$$D = \mu \frac{k_B T}{q} \text{ ....(2.20)}$$

Equations stated above are applicable to both electrons and holes by using their respective parameters. If the mobility and lifetime values are high enough, the drift and diffusion lengths will be lengthy. These high values can be acquired by utilizing high-purity materials and very tidy fabrication processes, which also minimize the impact of charge-trapping phenomena, thus enriching the collection efficiency.

After analyzing the preceding equations, it is evident that the collection times of electrons and holes spawned within a depleted region a few 100s μm in width are of the order of nanoseconds. On the other side of the coin, since mobile charges spawned within the neutral region will shift by diffusion, their collection times are much longer, of the order of microseconds. It should also be considered that throughout their motion in the direction of the collecting electrode, electrons and holes also propagate out as a cloud from their point of origin, due to diffusion. The radius of the diffusive cloud (r_c) at the time carriers will reach the electrode can be illustrated as:

$$r_c = \sqrt{2Dt_c} \text{ ....(2.21)}$$

Where t_c is the collection time, which for sure, is longer for the carriers generated far away from the electrodes. Another crucial trait regards the presence of a magnetic field for silicon sensors applied for particle tracking in order to permit measurements of the particle momentum. Nevertheless, the magnetic field, besides manipulating

the trajectory of the particle, also affects the motion of free charges within the sensor volume. As a result, electrons and holes drifting toward the electrodes are deflected by the Lorentz force [10]. The difference in the drift direction is commonly described by the opening angle, θ_L, assessed with respect to the direction of the electric field. Standard values of the Lorentz angle are generally in the range of 0° to 20° and can be evaluated for electrons $\theta_{(L,n)}$ and holes $\theta_{(L,p)}$ with the following equation:

$$tan\theta_{(L,n)} = \mu_{(H,n)}B_{\perp} \qquad tan\theta_{(L,p)} = \mu_{(H,p)}B_{\perp}$$

……………….(2.22)

Where μ_H is the Hall mobility and $B_{\perp}$ is the magnetic field component that is perpendicular to the direction of the charge carrier drift. In turn, the Hall mobility is proportional to the drift mobility: $\mu_H = r\mu$. The Lorentz factor r is slightly temperature-dependent, and its value is 1.15 for electrons and 0.72 for holes at 0° [10].

2.3.2 Induced signal in silicon detectors

In principle, a silicon sensor should be entirely depleted, so that the electrons and holes generated by radiation will drift under the influence of an electric field. In such circumstances, it should be emphasized that the current signals stimulated on the electrodes will appear instantly as the charges start moving, and not when they reach the respective electrode. With reference to a system with an arbitrary electrode structure, the current signal prompted by a single elementary charge on the electrode of interest can be stated by Shockley–Ramo's theorem as [11, 12]:

$$i(t) = -q\vec{v}(t).\overrightarrow{E_W} \quad ……………………………….(2.23)$$

Where two vectors appear, $\vec{v}(t)$ denoting the velocity and $\overrightarrow{E_W}$ denoting the weighting field. In spite of the similarity of their name, the weighting field is very distinct from the electric field. The electric field varies with the bias, and it governs the charge carrier trajectory from its point of creation to the point of collection at the electrode and the carrier velocity (through the mobility). The weighting field depends only on the electrode geometry and regulates the fraction of charge induced on each electrode. The weighting field depends on the weighting potential V_W. In particular, $\overrightarrow{E_W} = -\nabla V_W$. The spatial distributions of these variables for a given electrode are acquired by solving Laplace's equation $\nabla^2 V_W = 0$ (i.e., the Poisson's equation in

the absence of charge distribution), setting the electrode of interest at 1 and keeping all the other electrodes grounded. As an example, an uncomplicated structure, that is, a diode on an n-type substrate, with only two electrodes (one for readout and one for bias) at a distance d equal to the substrate thickness, as illustrated in fig 2.7. Assuming the bias voltage (V_{bias}) to be larger than the full depletion voltage (V_{fd}). In this circumstance, the electric field indicates a linear dependency on depth and can be formulated as:

$$E(x) = \frac{2V_{fd}}{d^2}(2x - d) + \frac{V_{bias}}{d} \quad \text{or,} \quad E(x) = \frac{E_{max} - E_{min}}{d}x + E_{min} \quad ......(2.24)$$

Where,

$$E_{min} = E(0) = \frac{V_{bias} - V_{fd}}{d} \text{ and, } E_{max} = E(d) = \frac{V_{bias} + V_{fd}}{d} \quad ....(2.25)$$

In case $V_{bias} \gg V_{fd}$, equation 2.24 can be shortened, maintaining an approximately constant electric field throughout the whole diode volume ($E \cong \frac{V_{bias}}{d}$) so that the electron ($v_e$) and hole ($v_h$) drift velocities are also constant and can be written as:

$$v_e = \mu_e E = \mu_e \frac{V_{bias}}{d} \quad \text{and,} \quad v_h = \mu_h E = \mu_h \frac{V_{bias}}{d} \quad ....(2.26)$$

Where μ_e and μ_h are the electron and hole mobility, correspondingly. The weighting field is also a constant, $E_W = 1/d$ for both electrodes. As a result, the induced current signals will also be constant throughout the motion of carriers to the electrodes and can be formulated as:

$$i = qvE_w = q\mu E E_w = q\mu \frac{V_{bias}}{d^2} \quad ....(2.27)$$

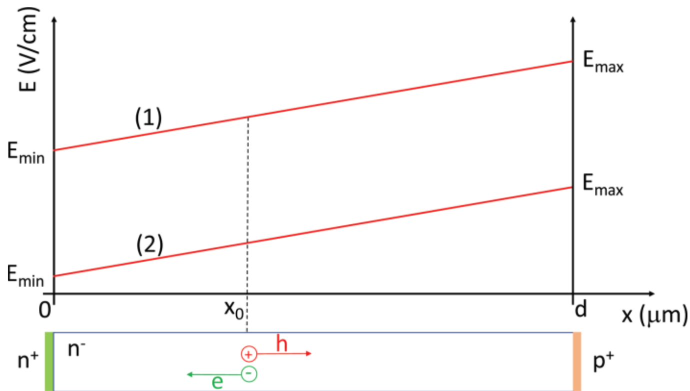


Fig 2.7: An illustration of the electric field in a P-I-N diode slightly above full depletion.

Assuming that an electron-hole pair is spawned at a certain position x_0 amid the n-type electrode (x = 0) and the p-type electrode (x = d). In such a case, the collection times of electrons and holes can be formulated as:

$$t_e = \frac{x_0}{v_e} = \frac{x_0}{\mu_e E} = \frac{x_0 d}{\mu_e V_{bias}} \quad \text{and,} \quad t_h = \frac{d - x_0}{v_h} = \frac{d - x_0}{\mu_h E} = \frac{(d - x_0)d}{\mu_h V_{bias}} \quad \text{........(2.28)}$$

Because of their inverse charge sign and drift direction, the electron and the hole stimulate a signal of the same polarity on one electrode. From Eqns. 2.27 and 2.28, the combined charge signals for electron and hole can be formulated as follows:

$$Q_e = \int_0^{t_e} i_e dt = i_e t_e = q\frac{x_0}{d} \text{ and,} Q_h = \int_0^{t_h} i_h dt = i_h t_h = q\frac{(d - x_0)}{d} \quad \text{...(2.29)}$$

The addition of the two charge signals is the rudimentary charge q; more significantly, the contribution to the total induced charge by the electron and the hole only alters with the generation point. For that, if the charges were spawned very close to the p-type electrode, the hole would be accumulated promptly, inducing an insignificant signal, and the entire signal would be induced by the electron movements, as well as the opposite would happen in the n-type electrode for hole movement. If the only consideration is the total charge signals induced on the electrodes rather than on their time evolution, integration of equation 2.23 can offer a prompt solution:

$$Q_e = -q\int_0^{t_e} v_e E_W dt = -q\int_{x_0}^{0} E_W dx = -q[V_W(0) - V_W(x_0)]$$

$$Q_h = q\int_0^{t_h} v_h E_W dt = q\int_{x_0}^{d} E_W dx = q[V_W(d) - V_W(x_0)] \quad \text{................(2.30)}$$

More generally, an elementary charge $e_0 = \pm q$, moving from an initial point x_i to a final point x_f, will induce a mirror charge on the electrode:

$$Q_{i,f} = e_0[V_W(x_f) - V_W(x_i)] \quad \text{................................(2.31)}$$

If the considered moving charges can carry out their trajectories from the point of origin to the electrodes, the outcome of equation 2.31 becomes the same as in equation 2.29. Nevertheless, if the moving charges could not reach the corresponding electrodes, either because of recombination or trapping, a portion of the induced charge signal will be lost. In such circumstances, equation. 2.23 should include a correction factor for the moving charge:

$$i(t) = -q.\exp\left(-\frac{t}{\tau_{eff}}\right)\vec{v}(t).\overrightarrow{E_W} \quad \text{.............................(2.32)}$$

Where τ_{eff} is the mean free drift time. Again, if the absorption time of the readout circuit is not sufficient as compared to the collection time, a portion of the charge will be lost, causing the ballistic deficit. A more sensible situation of a diode with the same attributes as before but reverse biased, only slightly above full depletion can be considered (case 2 in Fig. 2.7). While the weighting field is still persistent because it only alters with the thickness, the linear dependence of the electric field on the depth can no longer be overlooked, as illustrated in fig. 2.7. As a result, the current signals differ with the position and, in turn, on time, and it can be written:

$$i(x) = qv(x)E_W = q\mu E(x)E_W = q\mu\left[\frac{2V_{fd}}{d^2}(2x-d) + \frac{V_{bias}}{d}\right]\frac{1}{d} \quad \text{..........(2.33)}$$

It is possible to analyze the current signals induced by an electron-hole pair created at a certain depth x_0 [13]. Actually, the time necessary for a charge carrier created at x_0 to reach a generic point x can be expressed by the following equation:

$$t(x) = \int_{x_0}^{x}\frac{1}{v(x)}dx = \int_{x_0}^{x}\frac{1}{\mu E(x)}dx = \frac{1}{\mu}\int_{x_0}^{x}\frac{1}{E(x)}dx \quad \text{................(2.34)}$$

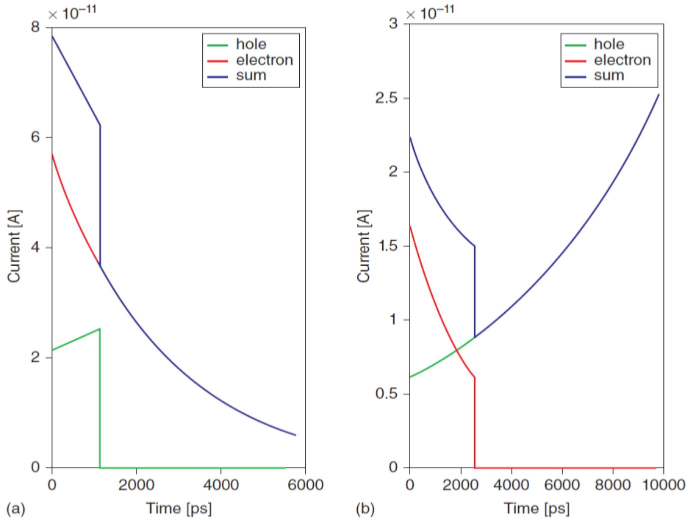


Fig 2.8: Time dependence of current signals induced on the p-side electrode of device in fig. 2.6 by an electron hole pair generated at: (a) x_0 = 250 µm (i.e., 50 µm from the p-side electrode), and (b) x_0 = 50 µm (i.e., 250 µm from the p-side electrode).

The linear dependence of the electric field on the distance generates a logarithmic dependence of the time on the distance, which on the other hand, indicates that the position shows an exponential dependence on time. Since the electron drifts to the n-side electrode (lesser electric field), it tempts a current signal succeeding an exponential decay with time; on the other hand, the hole drifts to the p-side electrode (higher electric field), therefore inducing a current signal, which exponentially rises with time. The total stimulated current is hence the addition of two exponentials. At the point of the charge transit, consistently with equation 2.31, the total induced charge on the p-side electrode is contingent only on the creation position x_0 as in the preceding shortened case, but the assortment time (signal duration) now exhibits a more composite dependence on the creation location. For example, fig. 2.8 illustrates the time evolution of the current signals induced by an electron-hole pair spawned at two separate depths in a 300-μm thick sensor. Figure 2.8 (a) indicates a cohort depth of 250 μm, which is, 50 μm away from the p-side electrode. The hole must drift only a tiny space to the junction, so it can be accumulated very quickly and induces only a slight portion of the total charge. On the contrary, the electron has to drift for 250 μm to the n-side contact, so it induces the foremost portion of the signal. The overall collection time is restricted by the electron, as it has to travel a considerably lengthier space than the hole, using about 6 ns. Figure 2.8 (b) describes the asymmetrical issue, where the electron-hole pair is spawned at a depth of 50 μm, which is, 250 μm from the p-side electrode. In such a case, the electron is accumulated very quickly and induces only a tiny portion of the total charge. The hole must drift for the majority of the depletion region: it induces the biggest portion of the signal and, as its mobility is smaller than that of the electron, it affects the total collection time to be lengthier ($\sim$10 ns). In end, in a simple sensor with only one readout electrode as a diode, the impact on the total signal from the hole and the electron depends only on the creation point. Owing to the different mobility values, the option of the readout (either p or n) can affect the collection time, thus influencing the radiation tolerance. The use of Shockley–Ramo's theorem turns out to be much more complicated in segmented sensors like strips or pixels. Because of the existence of numerous readout electrodes, the weighting potential

(field) profile is not linear (constant) throughout the sensor volume. For example, let's think about a p-on-n strip sensor of 300 µm thickness. The strip pitch and width are 100 µm and 50 µm, respectively. Figure 2.9 illustrates the two-dimensional weighting potential distribution analyzed with reference to the central strip electrode concentrated at x = 0 (Strip 1). The maps were acquired by solving Poisson's equation after substituting the silicon substrate with a dielectric layer to null the charge.

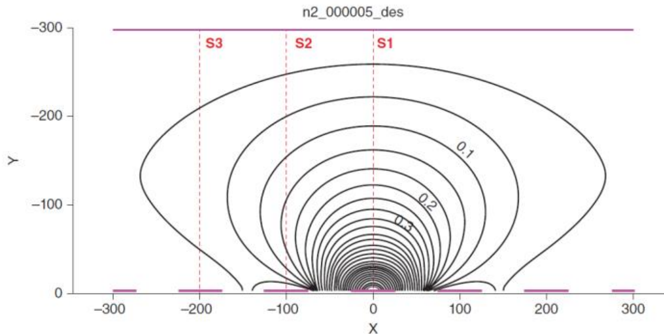


Fig 2.9: Modeled weighting potential distribution in a p-on-n strip sensor (upside down). All geometrical dimensions are provided in micrometers, while the weighting potential is unitless.

The weighting potential quickly reduces as the distance from the central strip electrode rises. This tendency can be better appreciated after viewing the one-dimensional cuts of the weighting potential of Fig. 2.10, taken along lines S1, S2, and S3 of Fig. 2.9, which resemble the centers of the strip (x = 0), first neighbor strip (Strip 2, x = –100 µm), and second neighbor strip (Strip 3, x = –200 µm). The weighting potential in a pad sensor (diode) of a similar thickness is also displayed as a reference. Seeing at cut S1, it can be noticed that the weighting potential is topped in a tight region beneath the electrode and then abruptly drops (at a depth of –100 µm, the value is 0.2). Therefore, the consequent weighting field is elevated only near the electrode, and it is far smaller elsewhere. Consequently, the majority of the signal is induced on Strip 1 by charge carriers that are close sufficient to it, so only those charge carriers that drift near that electrode are actually important. The other carrier type, which goes to the rear, stimulates only a tiny portion of the signal,

except its origin point is extremely near to the strip electrode. In the case of a MIP particle overpassing the contemplated strip sensor perpendicularly to the surface and spawning a roughly uniform charge distribution alongside its track, about 80% of the signal is induced by holes drifting in the direction of the elevated weighting field region. Figure 2.10 also demonstrates that the weighting potentials computed along with cuts S2 and S3 display a nonmonotonic trend, beginning and stopping at 0V (due to boundary conditions). The consequent weighting field alongside those lines will have a bipolar structure (i.e., with both positive and negative values), reliant on the depth. Charges spawned along lines S2 and S3 will drift toward and ultimately be accumulated by Strip 2 and Strip 3, correspondingly, go along with the electric field lines (not shown); these lines are consistent throughout the majority of the bulk since all strips are biased at the identical potential. Even though those charges will be accumulated by neighboring strips, they will also induce a bipolar current pulse on Strip 1, although with zero net integral (null total induced charge). More commonly, at the culmination of the charge motion, a net total induced charge not equal to zero is only noted at the accumulating electrode, but while the charge is shifting also other electrodes can encounter non-negligible bipolar current pulses.

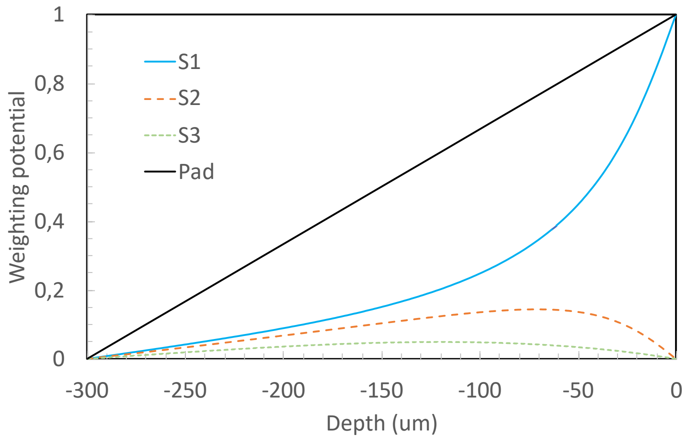


Fig 2.10: 1-D cuts of the weighting potential along lines S1, S2, and S3 of Fig. 2.9, corresponding to the center of three adjacent strips. The weighting potential in a pad sensor (diode) of the same thickness is also demonstrated.

2.4 Readout Electronics and its Noises

Silicon sensors utilized for particle tracking are largely read out with charge-sensitive amplifiers supported by pulse-shaping circuits to improve the noise performance. This is also the traditional composition of a spectroscopic chain. Basic theories on energy resolution and noise issues will be summarized in the subsequent division.

2.4.1 Energy Resolution

Some applications like spectroscopy require a measurement of the incident radiation energy distribution. To do that, a key parameter for performance evaluation is the energy resolution that signifies the detector's capability to differentiate between two or more photons having approximately equivalent energies. To acquire these quantities, the detection system, comprising the sensor as well as the readout electronics, ought to deliver an output signal (voltage pulse) of amplitude proportional to the quantity of energy accumulated in the sensor by each incident photon. In principle, in case the photon is radiated by a monoenergetic source, the detector reaction should be a single impulse, which can be signified as intensity versus energy curve. Still, the detector output spectrum of such type of source is a fairly broad peak on a count (proportionate to intensity) against pulse height (proportionate to energy) curve. In summary, uneven pulse heights are created for photons of equal energy. This effect is called line broadening and can be explained by considering the statistical variations in the number of produced carriers and the magnitude of the probable noise resources [3]. The formation of electron-hole pairs inside a silicon sensor is certainly a statistical process. If such a process follows Poisson statistics, the standard deviation in the number of electron-hole pairs, N, would be equal to the square root of this number. The standard deviation, $\sigma_{Poisson}$, for the Gaussian energy pulse can be found by the following equation [14]:

$$\sigma_{Poisson} = \sqrt{N_{ave}}.E_{ion} \quad \text{.....................................(2.35)}$$

Where N_{ave} is the average number of charge carriers produced. The intrinsic energy resolution, defined as the full width at half maximum (FWHM) of the Gaussian pulse, as portrayed in Fig. 2.11, is related to the standard deviation by the following equation:

$$FWHM = \frac{dE}{E} N_{ave}\sigma_{Poisson} = 2.35\sigma_{Poisson} \quad \text{......................(2.36)}$$

Substituting equation 2.35 into equation 2.36, and considering that $N_{ave} = E_{ph} / E_{ion}$, it can be obtained:

$$\frac{dE}{E} = 2.35\sqrt{\frac{E_{ion}}{E_{ph}}} \quad \text{...................................(2.37)}$$

Equation 2.37 indicates the benefits correlated with low-ionization energy; additionally, it is apparent that the energy resolution weakens with diminishing photon energy. In reality, precise measurements of the energy resolution have resulted in magnitudes decreased by a factor of 3 or 4 than those presented by equation 2.37, thus suggesting that the processes leading to the production of each charge carrier are not independent. Hence, simple Poisson statistics are not suitable for explaining these procedures. This incongruity can be taken into account by introducing the Fano factor, F, as an adjusting parameter in equation 2.37 [14]:

$$\frac{dE}{E} = 2.35\sqrt{F\frac{E_{ion}}{E_{ph}}} \quad \text{..................................(2.38)}$$

Though a comprehensive justification of all the procedures that direct to a non-unity value for the Fano factor has not been presented still, some models have been established that qualitatively account for the experimental interpretations. Numerical values of the Fano factor near 0.12 have been testified for silicon [14].

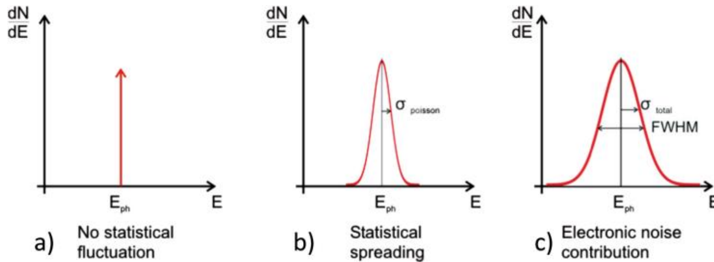


Fig 2.11: (a) Ideal energy spectrum measurement without fluctuations, (b) with Poisson fluctuations only, and (c) with both Poisson and electronic noise fluctuations.

2.4.2 Electronic Noise

The energy resolution of a silicon detector depends on two factors: (1) the fluctuation in the quantity of electron-hole pairs that are created by the incident radiation, and (2) the fluctuation in the quantity of charge that is efficiently detected by the readout

electronics system [14]. The first factor, occurring from the mechanisms engaged in the transition of radiation energy into electric charge, establishes an intrinsic threshold for energy resolution. The second factor is associated with the physics of the electric charge transportation and measurement; the latter is defined by the "electronic noise" present in the detection system and establishes an extrinsic threshold to the energy resolution that might also differ with time (drift). If all these sources of fluctuation were independent, the total energy resolution (FWHM) would be provided by the quadrature sum of the FWHM values for each particular source:

$$FWHM_{total}^2 = FWHM_{satistical}^2 + FWHM_{noise}^2 + FWHM_{drift}^2 + \cdots \quad ...(2.39)$$

Where the dots define room for another autonomous source of fluctuation. In the area of radiation detection and measurement, the energy resolution due to electronic noise is typically stated in terms of equivalent noise charge (ENC) as a substitute for (FWHM) noise. ENC is described as the quantity of charge, which, if utilized in the input terminal of the detection system, would give an increase to a unitary SNR—that is, to an output signal equivalent to the RMS level of the output due to noise only. Eliciting equations 2.35 and 2.36, it can be written for silicon at room temperature:

$$FWHM_{noise} = 2.35 \cdot 3.6 \cdot ENC = 8.5ENC \quad ....(2.40)$$

Where $FWHM_{noise}$ is articulated in units of eV, and ENC is articulated in units of electrons RMS. The analysis of the various noise impacts related to the detector and the readout electronics can be conducted with respect to a standard spectroscopy system, whose fundamental graphic is portrayed in fig. 2.12. The comprehensive study of the ENC is quite complex since it alters many variables. Only a fundamental analysis is registered here, while further particulars can be discovered in [15]. While the time scale for the discharge of radiation energy in silicon is at the level of nanoseconds, the sensor output signal can be epitomized by a current pulse of intensity Qδ(t), where Q is the total amount of produced charge and δ(t) is the delta-Dirac function. The current pulse Qδ(t) is devoured into a feedback amplifier that transforms it into a voltage signal. If the preamplifier and the subsequent processing stages are appropriately constructed, their involvement in the total system noise is insignificant. To protect the fundamental data brought by the magnitude of the produced charge, Q, the most frequent design of the input preamplifier is that of a charge-sensitive amplifier (CSA). Following preamplification, signal and noise have

to be filtered to optimize the SNR. This is achieved by eradicating the low- and high-frequency elements of the signal, while conserving the most valuable data, which is, the amount of produced charge, in the output voltage pulse height. In theory, the finest SNR would be acquired if the pulse shape were an infinite cusp [15], but in reality, filters employ triangle, Gaussian, semi-Gaussian, and other shaping functions that demonstrate S/N ratios that are just marginally worse than the theoretical ceiling. As defined in [15], the noise sources can be classified into those that are efficient in series and parallel with the signal source. Both of them can be explained by their power densities, (A_W + A_f) and B_W, correspondingly, as exhibited in fig. 2.12, where other significant circuit rudiments are also designated: the detector capacitance (C_d) and leakage current (I_d), the bias resistance (R_b), the input capacitance (C_i), and the feedback network of the CSA (the feedback capacitance C_f and resistance R_f), and the shaping amplifier transfer function T(s).

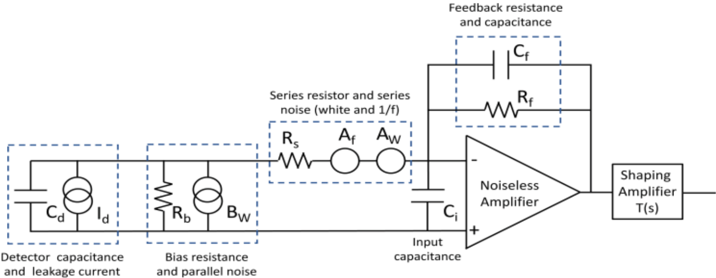


Fig 2.12: Drawing of a conventional radiation spectroscopy chain, comprising the sensor, the bias, and readout circuits, highlighting the different electronic noise sources.

The white series noise A_W is roughly solely influenced by the thermal noise in the current of the input transistor of the CSA and by the stray resistance (R_S) in series with the input, and it can be written as:

$$A_W = \frac{4k_B T\Gamma}{g_m} + 4k_B T R_s \quad \text{.....................................(2.41)}$$

Where g_m is the transconductance of the input transistor as well as the parameter Γ , which also alters with the type of input transistor ($\Gamma \cong 2/3$ for long channel transistor and have a tendency to 1 for short channel ones). Regarding the parallel noise, its main impacts are the shot noise in the detector leakage current, the shot

noise in the input transistor gate current (I_g), and the thermal noise of the CSA feedback resistor and the detector bias resistor, thus it can be written as:

$$B_W = 2qI_d + 2qI_g + \frac{4k_BT}{R_f} + \frac{4k_BT}{R_b} \quad \text{.............................(2.42)}$$

Again, as it was suggested in [15], the square of the corresponding noise charge can be conveyed as:

$$ENC^2 = A_W C_T^2 \frac{A_1}{\tau_{ch}} + A_f C_T^2 A_2 + B_W A_3 \tau_{ch} \quad \text{......................(2.43)}$$

Where $C_T = C_d + C_i + C_f$ is the total capacitance at the input of the amplifier, τ_{sh} is the shaping time, whereas A_1, A_2, and A_3 are the "shaping factors" that depend on the type of shaping and can be found in the literature for the most common formations. The coefficient A_f is linked to the 1/f noise, which is only reliant on the kind of input transistor utilized in the CSA. It is usually obtainable in datasheets or obtained from suitable measurements [16]. Counting equation 2.43 and utilizing the appropriate set of factors, it is conceivable to assess the noise of nearly any readout system. The three terms in equation 2.43 have divergent gradations of dependency on the shaping time: (1) The series noise is inversely proportional to τ_{sh} and directly proportional to the total capacitance, (2) the parallel noise is directly proportional to τ_{sh}, while (3) the 1/f noise alters only with the total capacitance and not with τ_{sh}. These circumstances are demonstrated in fig. 2.13 as a function of the shaping time. The quadrature sum of the three components generates a total ENC, which primarily reduces with the shaping time, extends to the bottom, and then begins to increase again. By means of discovering the lowest of this function, it is conceivable to ascertain the ideal shaping time for each system (τ_{opt}). Nevertheless, the shaping time similarly puts a restriction on the time resolution of the detection technique, which in turn regulates the highest pulse count rate. In spectroscopic functions, the optimal shaping is picked principally on the foundation of noise constraints without considerable restraints on the speed of the scheme, since the rate of arriving photons is typically minimal. In tracking functions, the shaper output is typically fed to a comparator that triggers only if the signal surpasses a particular limit. Additionally, the timestamp of the inbound particle is collected. Ever since the amplitude of a signal from a MIP pursues a Landau distribution, the ceiling of the comparator should be set minimum adequate to seize most of the signal. Consistently, it should be high

ample to preclude phony peaks due to noise and threshold dispersion from being logged as a hit into the system. Therefore, having a minimum ENC or, better, a decent signal-to-noise ratio is extremely crucial; utilizing the optimal shaping time would assist, but this is not every time feasible. In high-energy physics experiments, the shaping time is solidly constrained by the bunch crossing, which can be incredibly small (e.g., 25 ns at LHC), affecting the noise to be greatly reliant on detector capacitance.

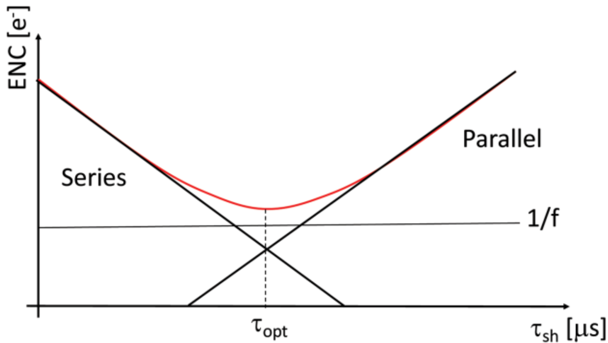


Fig 2.13: Summary of the various contributions to the ENC. Parallel, series, and 1/f noise are mapped vs the shaping time.

2.5 Radiation Damage

When silicon devices are controlled in extremely radioactive conditions, they endure acute impairment to their formation. Thorough research was made on this issue by numerous groups operating in several applications and has directed to an equitably comprehensive understanding of radiation damage in silicon devices, both from the microscopic establishment and from the progression of defects and the macroscopic properties on signal and noise deprivation [17-22]. This discussion will be mainly concentrated on the latest findings acquired because of the requirement for vigorous tracking devices for the Large Hadron Collider experiments at the European Organization for Nuclear Research (CERN) [23-26]. From such a perspective, it should be emphasized that the radiation level accrued by tracking devices in colliders' experiments is directly proportional to the beam-integrated luminosity calculated in inverse femtobarns. The inverse femtobarn (fb^{-1}) is a quantity of

particle-collision events and counts for both the collision number and the amount of data accumulated. One inverse femtobarn corresponds to roughly 100 trillion (10^{12}) proton-proton collisions.

Tracking detectors are typically positioned in the innermost part of the experiments and are visible to an assorted radiation field succeeding a negative exponential law, reliant on their radial distance from the center of the beam and their distance along the beam axis (Z) with respect to the beam's contact point. The eventual radiation tolerance goal for tracker detectors is hence the one conforming to a beam-integrated luminosity of about 4000 fb^{-1}, which will be achieved afterward after about 10 years of LHC operation succeeding luminosity upgrades, former of which should start in 2026 with instantaneous peak luminosity of $7.5 \times 10^{34} cm^{-2} s^{-1}$. This last factor hangs on several aspects but in brief, signifies the instantaneous number of interactions per second.

From the experimental, macroscopic point of view, radiation effects on silicon detectors can be split into two well-observed classifications: surface damage and bulk damage. On one side of the coin, surface damage influences alteration to the device's breakdown performance, the inter-electrode isolation, the surface carrier recombination, and consequently the overall device leakage current. Bulk damage, on the other side of the coin, influences the junction effective space charge and subsequently the device's full depletion voltage, the leakage current, now bulk generation, and the forfeiture of signal due to charge carriers entombed by radiation-induced imperfections, some of which are the identical ones accountable for the radiation-induced leakage current [17].

2.5.1 Surface Damage

An extremely essential step in any silicon device is surface passivation. It shields the semiconductor surface from peripheral agents and every feasible mechanical damage. Passivation in silicon devices is rendered largely by about 1 micron of silicon dioxide (SiO_2), occasionally supplemented by silicon nitride and an over glass. Conventionally, silicon dioxide has been the favored passivation technique utilized in silicon devices ever since it is instantly obtainable in any silicon-related process

fabrication facility, with a comparatively easy high-temperature step comprising of divulging the device to an oxidizing atmosphere.

Silicon dioxide is well-known to inhibit defects [27]. These defects, which are spawned both within it and at its edge with the silicon bulk, typically behave as extremely active charge traps. Such trapped charge can be separated into two distinct classifications:

1. Interface trapped charge, which can be positive or negative and is instigated by structural defects or oxidation defects, such as matured open bonds or radiation-induced bond breaking. Interface traps, stationed at the Si–SiO_2 interface, are vacant or loaded with electrons, dependent on the employed surface potential, and they frequently produce interface states. The major impact of interface states on the device characteristics is a feasible escalation of the surface carriers' generation–recombination, depending on their energy level surrounded by the bandgap and, hence, an expansion of the surface leakage current.
2. Oxide charge, which again can be separated into:
   - Mobile oxide charge is primarily instigated by the existence of ionic impurities such as sodium (Na), lithium (Li), and possibly hydrogen (H). In state-of-the-art detector technologies, this is not a concern anymore.
   - Fixed oxide charge, which is positive and close to the Si-SiO_2 interface. This charge typically shapes a layer, which draws negatively charged electrons on the other side of it, in the silicon bulk. The existence of the electron layer can take the lead to the current paths and shorts in the device, conceivably influencing the functionality and broken data of the sensor.
   - Oxide trapped charge, which can be either positive or negative, which outcomes from exposure to ionizing radiation, avalanche injection (e.g., during breakdown), or other processes and be able to be annealed at low temperature.

Ionizing radiation adjusts the intrinsic characteristics of these imperfections [17]. When a particle traverses a SiO_2 layer with adequate energy, it produces a charge via ionization. Greatest produced electron-hole pairs will recombine immediately, but a portion of them won't. Because of the exceedingly dissimilar mobility of electrons ($\mu_n \sim 20$ cm^2 V^{-1}s^{-1}) and holes ($\mu_p \sim 2\times10^{-5}$ cm^2 V^{-1}s^{-1}) in silicon dioxide, electrons can get away promptly whereas holes will hop to the Si-SiO_2 interface where they become trapped, consequently in a rise of the entire positive oxide charge.

Another supplementary radiation-induced impact on SiO_2 is the growth in interface states concentration, along with a substantial surge in surface recombination velocity and surface current [28]. It is evident that for <111> crystal orientation substrates, the oxide charge intensity begins, even in excellent oxides, from a limited unit of $10^{11} cm^{-2}$, whilst smaller values have been monitored for <100> ones [29]. The exposure to ionizing radiation affects this number to rise by at minimum one order of magnitude, and consequently up to ~10^{12} cm^{-2}. In the same instance, a universal amount for surface recombination velocity (s_0) is roughly 10 cm/s or less before irradiation, whilst it rises several orders of amount following irradiation [28].

An extremely critical facet associated with surface damage that is frequently undervalued is its deep dependency on the device's functioning requirements while exposed to ionizing radiation. This is the case for all silicon devices employed in collider experiments or those utilized as beam monitors at beamlines, which necessitate biasing the silicon p-n junction to achieve its complete depletion and, consequently, an efficient signal collection. Depending on the substrate polarity, while exposed to radiation beneath bias affecting the electric field via the oxide to point to the Si-SiO_2 interface, the oxide charge intensity and surface recombination velocity begin rising significantly already at low radiation doses. Even further astonishingly, the oxide charge intensity can attain values in the order of 4×10^{12} cm^{-2} at the doses of concern for tracking detectors and achieve even greater values in X-ray free-electron laser functions [29].

The major aftereffects of the exposure to ionizing radiation on the silicon device's oxide surfaces can be reviewed as follows:

1. Variation in total charge concentration owing to the accretion of positive charge trapped in the oxide, which entices negative charge on the opposite side of the interface heading to:
    - Negotiated isolation among divisions specified by n^+ doped electrodes. This could trigger shorts in pixels or strip readout electronics.
    - Enhanced parasitic capacitance among adjoining zones could worsen the noise performance of the device.
    - Altered electric field distribution at the silicon-silicon oxide interface, might alter the voltage-handling abilities of the sensor.

2. Customized interface conditions and surface recombination velocity heading to an expansion of the surface-related leakage current.

2.5.2 Bulk Damage

The destruction of the bulk is instigated by charged hadrons like protons, pions, or neutrons or highly energetic leptons like electrons or muons, in the silicon detectors utilized for tracking in highly radioactive atmospheres. The damage process is described principally by the failure of the kinetic energy of the crisscrossing particle within the silicon lattice via numerous collisions with the silicon atoms. If the energy of the studied particle is greater than the dislocation threshold energy E_d = 25 eV, the outcome is the dislocation of a primary knock-on atom (PKA), which shapes an interstitial and vacancy (Frenkel) pair [17]. Both interstitials and vacancies can drift in the silicon lattice with distinct mobility, varying with temperature [30].

In the end, they create stable defects after they correlate with impurities or doping atoms occur in the material. These defects can behave as effectual acceptors or donors. If the particle energy is greater than ∼5 keV, then extremely displaced defect clusters can be established. The shudder atom from an extremely energetic collision can hypothetically trigger additional damage to the silicon lattice [31]. Its energy deficit can happen via ionization or additional displacements. At the ending of a substantial recoil range, displacement predominates, and defect clusters are established, as can be observed in fig. 2.14, which indicates the mean displacement created by a 1MeV neutron, with a PKA of 50 keV.

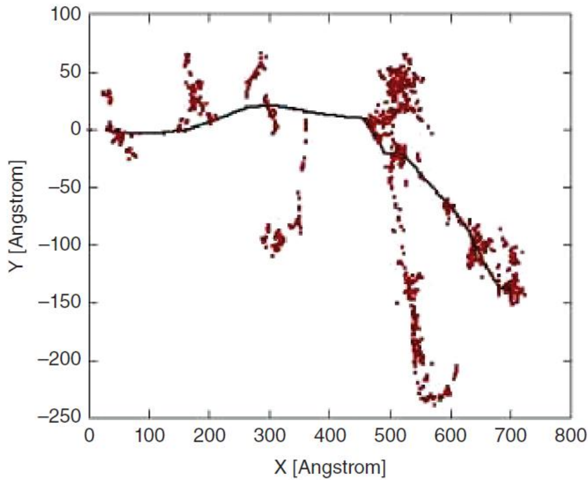


Fig 2.14: Displacement created by 1 MeV neutrons in silicon. This event produces 1159 displaced silicon atoms, 1053 developed vacancies, 106 supplants the dislocated atom, and 1159 interstitials are created. [32]

This simulation was presented using TRIM, an open-source simulator. This event generated 1159 displaced silicon atoms, among which 1053 grew into vacancies and 106 supplanted the displaced atom; 1159 interstitials were created [3]. As distinct particles and energies have been demonstrated to create a multiplicity of defects that affect, in a multiplicity of aspects, the sensor's parameters, it was critical to discover a technique to scale radiation damage with respect to the macroscopic effect's pragmatic in silicon [33-35]. The non-ionizing energy loss (NIEL) [36] was launched to analyze the displacement destruction in the material, which was demonstrated to scale linearly with the quantity of energy conveyed in the displacing collisions. By utilizing the displacement damage cross-section D(E), it was feasible to distinguish a hardness factor "k," which permits analogy of the damage efficiency of various radiation sources with distinct particles and particular energy spectra Φ(E):

$$k = \frac{1}{D(E_n)} \cdot \frac{\int D(E)\Phi(E)d(E)}{\int \Phi(E)d(E)} \quad (2.44)$$

Where E is the energy of the considered particle, Φ(E) is the energy spectrum of the radiation field, and D(E) is the displacement damage cross-section. The value of E_n

is 1MeV. Figure 2.15 indicates in what way the displacement damage cross-section of various particles correlates to one another at separate energies. The hardness factor is generally utilized to evaluate the damage generated by a particular kind of irradiation to the damage that would be triggered by the identical fluence of 1 MeV monoenergetic neutrons. The 1 MeV neutron equivalent fluence Φ_{eq} linking to certain irradiation can be analyzed utilizing the subsequent equation:

$$\Phi_{eq} = k\Phi = k\int \Phi(E)dE \quad \text{..................................(2.45)}$$

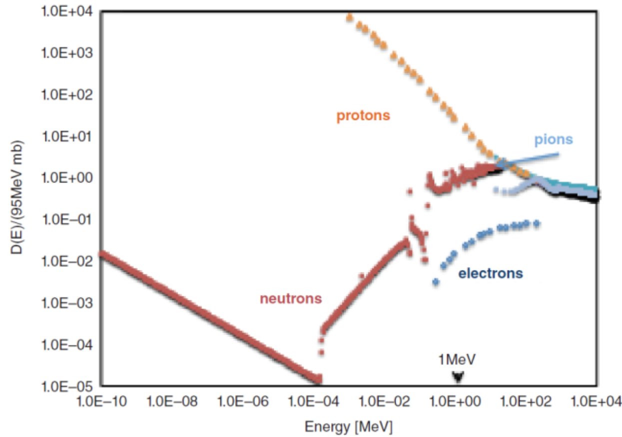


Fig 2.15: Displacement damage function D(E) normalized to 95 MeV mb, for various kinds of particles and energies. Mapped from data in [4].

The displacement-induced defects in the silicon lattice practically convert into the formation of energy levels within the forbidden bandgap, acting like acceptors or donors that can seize or radiate electrons. In thermal equilibrium, the charge state of the defect is meticulously associated with the Fermi level. An acceptor is always negatively charged while it is inhabited by an electron, whilst a donor in a similar situation is neutral. The acceptor gets a negative charge, and the donor becomes neutral when the Fermi level is superior to the defect level, and vice versa.

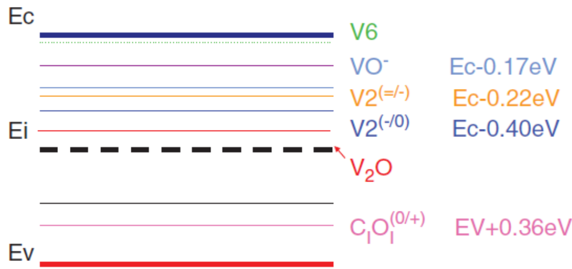


Fig 2.16: Interpretation of energy levels of steady defects detected after neutron and proton irradiation contained by the silicon bandgap. Vacancies and interstitials can relocate in the lattice till they encounter impurities and dopants present in the material establishing steady centers, which play as valuable donors and acceptors [4].

Figure 2.16 is a depiction of the defect dissemination inside the bandgap following the irradiation. The launching of donor-like and acceptor-like defects, in the center of the bandgap, may manipulate the efficient doping concentration of the silicon bulk and the leakage current as of the enrichment of the generation recombination rate. For instance, pondering a defect energy level E_t, the overall energy required to energize a trapped electron to the conduction band will resemble:

$$\Delta E = E_c - E_t \qquad (2.46)$$

2.5.2.1 Leakage Current

The establishment of radiation-induced energy levels in the prohibited band gap augments the generation–recombination methods in silicon. In reverse-biased p-n junctions, this explains an escalation in the reverse leakage current, which will eventually influence the ultimate signal-to-noise detector performance and the system power budget [17]. The escalation in leakage current after revealing to radiation was quantified on several devices, with n- and p-type substrates irradiated with various particles to be linearly proportionate to the irradiation fluence following the relationship stated by the equation:

$$\Delta I = \alpha \cdot \Phi_{eq} \cdot V \qquad (2.47)$$

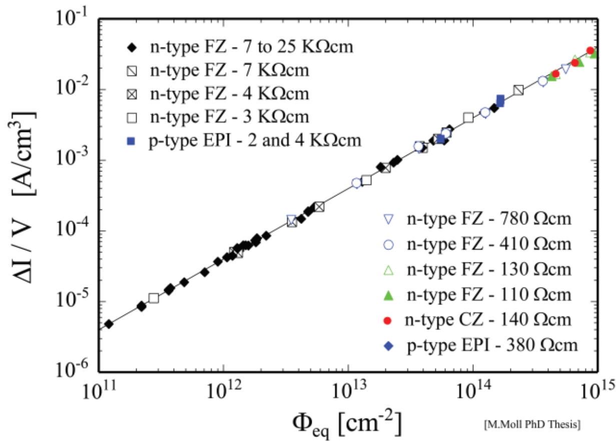


Fig 2.17: Leakage currents of devices manufactured in different materials revealed various types of radiation vs. fluence after thermal treatment at 60°C for 80 minutes [17].

Where α is the current-related damage parameter, Φ_{eq} is the 1 MeV neutron equivalent fluency, and V is the volume of the total depleted sensor, as can be witnessed in fig. 2.17. The leakage current is solidly temperature reliant, so the entire measurement is typically scaled to the constant reference temperature, typically 20°C, where the amount of the destruction parameter veers to be the value = (3.99 ± 0.03) × 10^{-17} A/ cm [17]. Nevertheless, it is impractical to rationalize the gauged current strength established on straightforward Shockley–Read–Hall generation–recombination procedures utilizing assessed midgap defects such as the di-vacancy V_2. Rectified current amounts were attained by incorporating the intercepter charge transfer progression where electrons are "hopping" to materially close defects in the direction of the conduction band [37]. Leakage currents assessed at various temperatures T can be associated by applying the following equation [38]:

$$I(T_R) = I(T) \cdot \left(\frac{T_R}{T}\right)^2 \exp\left[-\frac{E_g}{2k_B}\left(\frac{1}{T_R} - \frac{1}{T}\right)\right] \quad \text{.........................(2.48)}$$

Where T_R is the reference temperature (usually 20°C) and k_B is the Boltzmann constant. The damage-induced leakage current is supposed to be annealed at high temperatures whereas the damage constant α was demonstrated to reduce with time at distinct annealing temperatures [17]. From these results, it can be concluded that the silicon devices exposed to high radiation fluences had better be functioned below

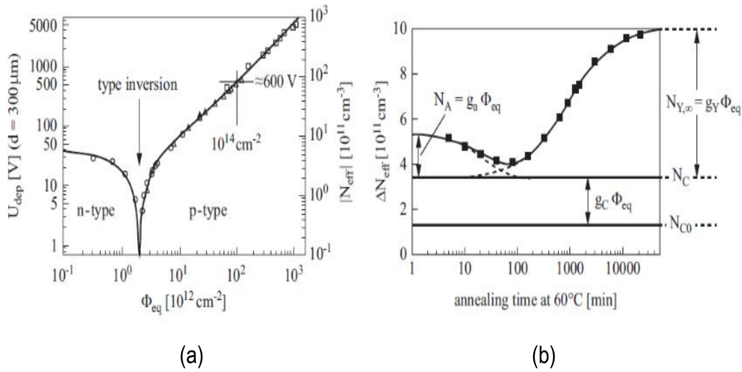
0°C to alleviate the upsurge of leakage current and subsequent signal-to-noise ratio and conceivably thermal runaway, but the devices should be kept at room temperature for limited days through downtimes to permit leakage current advantageous annealing. The material adjustment after irradiation outcomes in a significant alteration in the current-voltage (I-V) characteristics of silicon devices. The device does not demonstrate the characteristic forward and reverse current performance anymore but, rather, an expanding resistive dependency of the substrate exposure to radiation, which grows into symmetric at high fluences. The material is then said to be "relaxation-like" as a consequence of the Fermi level being "pinned" close to midgap, the place for lowest conductivity [39-41]. The moment of breakdown in the forward bias I-V curve has an immediate correlation with the fluence as well as the charge collection characteristics [41].

2.5.2.2 Effective Bulk Doping Concentration

Silicon detectors are typically regulated with the junction marginally over depleted (i.e., at a bias voltage marginally higher than the full depletion voltage), so that the active region is as viable free of charge carriers. In planar sensors, the depletion voltage is associated with the substrate thickness and the substrate doping concentration. If the junction is not fully depleted, the total signal generated by a particle crossing the device will be lessened.

Because displacement defects can perform either like acceptors or donors, relenting on their position in the bandgap, they can alter the full depletion bias voltage and in particular incidents the space charge's "effective" polarity. Numerous tests have indicated that the radiation-induced doping concentration can fluctuate differing on the fundamental material attributes. A dissimilar performance was also noticed in subsequent irradiation with separate particle types (extra precisely with neutron vs. proton irradiation) as they stimulate a discrepancy of point defects vs. defect clusters in the final owing to Coulomb interaction. A paragon of the alteration of effective doping concentration (N_{eff}) for an n-type beginning substrate is demonstrated in fig. 2.18 (a). The effective doping concentration is primarily decreased by a potential donor elimination, escorted by instantaneous efficient acceptor inclusion at minimal

fluences that ultimately lead to a p-type effective space charge-type inversion and an additional upsurge of N_{eff} proportionate to radiation fluence.



(a) (b)

Fig 2.18: (a) Variant of the effective doping concentration of an n-type silicon sensor as a function of the equivalent particle fluence (plot from [17] based on data from R. Wunstorf, Ph.D. thesis, University of Hamburg, 1992), and (b) its annealing behavior as a function of time at 60°C after irradiation at a fluence of 1×10^{13} n_{eq}/cm^2 [17].

N_{eff} endures both an advantageous and inverse annealing, which doesn't transpire to the current associated damage parameter α. The reason for overturn annealing is yet uncertain but may be correlated to the establishment of a multi-interstitial defect witnessed with photoluminescence [42]. Both impacts are demonstrated in fig. 2.18 (b). Oxygenation has been demonstrated to regulate the alteration of the space charge and overturn annealing following proton irradiation, behaving like an extremely economical taker for vacancies whilst carbon has been exhibited to improve deleterious impacts [43].

The efficient doping concentration in p-type materials was additionally noticed to boost fluence, as can be viewed in fig. 2.19 [44]. At the comparatively significant irradiation fluences of interest for collider experiments, for n-type substrates, the steady destruction span can be transcribed contemplating simply the acceptor initiation that ensues following type inversion and snubbing the preliminary donor elimination.

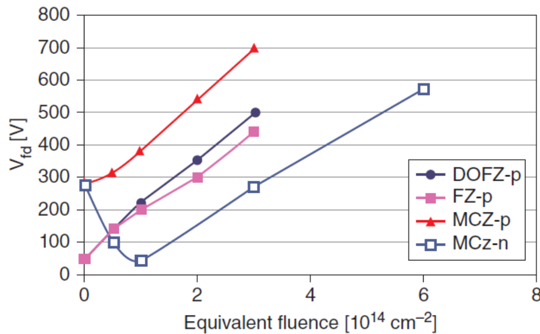


Fig 2.19: Dependence of full depletion voltage (V_{fd}) on neutron fluence for MCz and FZ p-type materials (From Kramberger, G. et al., Nucl. Instrum. Methods A, 2007) [42].

The current obtainability of pure p-type substrates permits their usage for radiation hard sensors meanwhile the junction electrode in p-type devices remainders on the identical side similarly subsequently substantial irradiation, dodging the noteworthy signal deprivation and the forfeiture of spatial resolution owing to under depletion that distresses p-on-n sensors [45, 46]. Prior To irradiation, p-on-n sensors deplete from the p+ electrode in the direction of the backplane. Following irradiation (left outline in fig. 2.20), the bulk endures type inversion, turns out to be p-type. The depleted region expands from the n+ electrode, and owing to irradiation, the substrate has a higher N_{eff}, which enhances the full depletion voltage. Parenthetically, it should be emphasized that after irradiation the weighting field, may not alter its structure while it alters only with the electrodes' geometry, and it peaks close to the accumulating electrode for a parted geometry. Holes and electrons spawned in the depleted zone now near the backside zone are prompting a very low signal on the accumulating electrode from the time when the weighting field tops close to the surface and goes to zero swiftly. At high-radiation levels, segmented planar p-on-n sensors might have complexity depleting up to the accumulating electrode with a substrate thickness worthwhile to provide sufficient charge (200 microns), so the signal will be incredibly little.

Meanwhile, n-on-p detectors can overpower this dilemma as no type inversion ensues following irradiation [44] as well as n-on-n detectors following type inversion,

as the junction will constantly be adjacent to the readout electrode where both electric and weighting field are stout, illustrated in fig. 2.20 (right sketch). While the most important part of the signal (≈ 80%) is stimulated by carriers shifting to the readout electrode that accumulates electrons, these detectors are intrinsically quicker than p-on-n, also counteracting trapping probability.

It has been noticed that n-type materials following type inversion have exhibited a tenacity of the main junction. This dual electric field peak, renowned as a "double junction," has been exhibited to marginally enhance the overall accumulated charge [47,48].

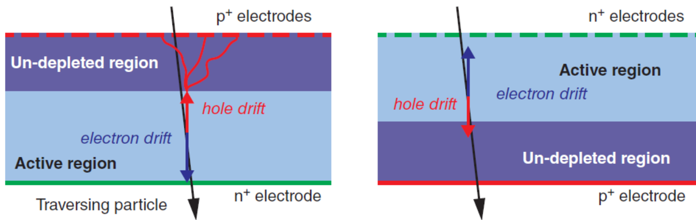


Fig 2.20: Graphic cross-sections of p-on-n (left) and n-on-p (right) partitioned sensors, both with effectual p-type bulk following irradiation and functioned in an under-depleted ailment [4].

2.5.2.3 Signal Degradation due to Charge Trapping

The prevalent reason for signal deficiency in detectors irradiated to beyond a fluence of 1×10^{15} $n_{eq}.cm^{-2}$ has been perceived to be trapped, as the majority of defects behave as extremely effective trapping centers for free carriers. If free carriers spawned from an impinging particle are detained, they are typically not freed prior to hours or retentive at room or smaller temperatures [49]. Such carriers hence terminate to contribute to the ultimate sensor's signal inside the current electronics readout times (~25 ns for the Large Hadron Collider experiments). The entire trapping probability is inversely proportional to the irradiation fluence, which can be described by the following equation:

$$\frac{1}{\tau_{eff,(n,p)}} = \beta_{n,p}(t,T)\Phi_{eq} \quad \text{......................................(2.49)}$$

Where τ_{eff} is the effective trapping time and β is the trapping time constant, is time and temperature reliant and is also affected by the nature of particles utilized for

irradiation. The effective drift length for electrons and holes varies with their effective trapping times. The greater the fluence the silicon bulk gets, the smaller the carrier's effective drift length (λ), which can be observed from the following equation:

$$\lambda = \tau_{eff} v_D \quad \text{...(2.50)}$$

Where v_D is the drift velocity, implying that smaller trapping times will end in a greater quantity of carriers being entombed. The aggregate quantity of drifting charge that stimulates current on the readout electrodes pursues Shockley's and Ramo's theorems and takes into account the trapping probability in a negative exponential, which can be stated as:

$$N_{e,h} = N(0)\exp\left(-\frac{t}{\tau_{eff,(n,p)}}\right) \quad \text{..............................(2.51)}$$

Classifying a signal induced by spawned charge in a detector was a significant work prior to Ramo and Shockley determined at the same time in 1939 that a signal spawned by shifting charges in a conductor could be merely obtained utilizing their "weighting potentials" and "weighting fields.". In a parallel-plate detector of thickness L with an applied bias voltage V_b, the electric field, which is different from the weighting field, across it would be $E = V_b/L$. A charge produced inside the detector volume would thus have a velocity of $v_D = \mu E = \mu \frac{V_b}{L}$. If a potential equivalent to 1 on the collecting electrode and zero on the bias one, then it has been seen that a weighting field would be consistent and equal to $E_W = 1/L$. The induced charge Q_0 on the accumulating electrode by a charge q was computed applying electrostatic laws to be $Q_0 = -qV_W$, where V_W is the weighting potential. The association between the weighting potential and the weighting field is $E_W = -\nabla V_W$. If a one-dimensional case is considered, alongside the x coordinate, then it can be written that, $E_W = -dV_w/dx = 1/L$. The stimulated current on the collecting electrode (the one at potential = 1) is presented by the equation:

$$i(t) = qv_D E_W = \frac{qv_D}{L} \quad \text{.................................(2.52)}$$

If an electron-hole pair was spawned at position x inside the sensor's volume, the stimulated charge will hinge on the time the electrons and holes will need to reach their corresponding electrodes. The stimulated charge for electrons and holes would hence be is written as:

$$Q_e = it_e = \frac{q_e}{L}x \quad and \quad Q_h = it_h = \frac{q_h}{L}(L-x) \quad \text{.........(2.53)}$$

Where q_e and q_h are the electron and hole charges correspondingly. Because of the existence of trapping, the charge stimulated to the accumulating electrode will be decreased by the lifetime of the carriers. The portion of charge Q_{tr} lingering following trapping can then be articulated as $Q_{tr}(t) = Q_0 \exp(-t/\tau)$, where Q_0 is the charge with no trapping and where the time to pass through a remoteness x is defined as $t = x/v_D = x/\mu E$. By replacing the articulation of t in the preceding exponential equation, the induced charge as a function of distance x can be attained as:

$$Q(x) = Q_0 e^{-\frac{x}{\mu\tau E}} = Q_0 e^{-\frac{x}{\lambda}} \quad \text{............................(2.54)}$$

The mobility lifetime product $\mu\tau$ is a marker of the class of the sensor, whereas $\mu\tau E$ is the effective drift length λ. The signal growth with trapping, presuming a produced unit charge q = 1 in spot x within the active volume, can thus be classified as ensues:

$$\frac{dS}{dt} = \frac{dQ(x)}{dt} = \frac{d}{dt}\left(Q_0 e^{-\frac{x}{\lambda}}\right) = \frac{d}{dt}\left(-V_W e^{-\frac{x}{\lambda}}\right) = \frac{d}{dt}\left(-V_W e^{-\frac{x}{\lambda}}\right)\frac{dx}{dx} =$$
$$\left(-\frac{dV_W}{dx}\right)e^{-\frac{x}{\lambda}}\frac{dx}{dt} = E_W e^{-\frac{x}{\lambda}}\frac{dx}{dt} \quad \text{... ....(2.55) [4]}$$

Where the derivative over a distance of the weighting potential turns out to be the weighting field and the minus sign vanished. It is possible to obtain the ensuing signal by integrating the preceding equation from point x to the accumulating electrode at point 0:

$$S = \int dS = \int_x^0 E_W \frac{dx}{dt} e^{-\frac{x}{\lambda}} dt = \frac{1}{L}\int_x^0 e^{-\frac{x}{\lambda}} dx$$
$$= \frac{1}{L}\left[\left(\lambda e^{-\frac{0}{\lambda}}\right) - \left(\lambda e^{-\frac{x}{\lambda}}\right)\right]$$
$$= \frac{\lambda}{L}\left(1 - e^{-\frac{x}{\lambda}}\right) \quad \text{.............. ....(2.56) [4]}$$

For a charge which is trapped prior to making to the collecting electrode (x>>λ), S = λ/L. In another way, the charge that even becomes trapped creates some signal. It should be emphasized that the drift velocity v_D following irradiation is typically inundated to a value ~10^7 cm s^{-1} and hence is persistent in place owing to the necessity to run irradiated detectors through a lofty electric field. Therefore, the efficient drift length is likewise persistent and autonomous on stance as a lofty bias voltage is employed. The efficient trapping probability for electrons and holes has been calculated [50] and can be observed in fig. 2.21.

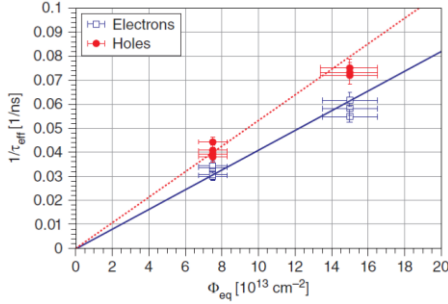


Fig 2.21: Reliance of the effective trapping probability of electrons and holes vs. fluence, demonstrating that electrons have an extended lifetime and consequently a greater probability of impacting a greater signal than holes. A slender disparity in trapping probability has been remarked with irradiation achieved with neutrons and protons [50].

Considering data in fig. 2.21, it is feasible to obtain the trapping time constant τ_{eff} , for electrons and holes, which is, for electrons $3.7 \times 10^{-16}cm^{-2}$ s^{-1} and $5.4 \times 10^{-16}cm^{-2}$ s^{-1} ; and for holes $5.7 \times 10^{-16}cm^{-2}$ s^{-1} and $6.6 \times 10^{-16}cm^{-2}$ s^{-1} following neutron and proton irradiation, correspondingly. Therefore, while a lesser trapping time constant implies lengthier drift, electrons get a lengthier lifetime prior to being trapped and hence can add to a greater signal. The latest research of fluences up to $10^{17}n_{eq}cm^{-2}$ appear to tip to a saturation of the trapping probability. This outcome would clarify some inspection of saturated signal efficiency at high fluences [51].

Effective trapping probability, doping concentration, leakage current hangs on time, and annealing temperature. The easiest model that illustrates the advancement of the trapping probability is the decay from one electron or hole trap state to further steady destruction. When annealing is operated at 60°C [50], it is noticed that the long-term annealing is advantageous for electrons and not advantageous for holes. In reality, along with time, the trapping probability falls for electrons (∼15%) and rises for holes (∼30%). The temperature of the annealing phase does not alter the amount of the trapping probability after the ephemeral phase, but just the time constant to the changeover from one state into the other. The time constant of the transition is ≈ 600 minutes at 60°C. In the case of room temperature, the constant time increases up to 50 days. It can be concluded that again, electron readout has to

be preferred to hole readout since electrons are 3 times faster than holes and have a lower trapping time constant τeff concerning holes. In addition, the annealing tends to lower the trapping probability for electrons while it increases it for holes. A full description of these important measurements can be found in [50]. For the situation in which charge is generated uniformly between the p+ and n+ electrodes, one can show that the signal efficiency (SE), defined as the ratio of the maximum signal with trapping to the maximum signal with no trapping, is:

$$SE = \frac{\lambda}{L} - \left(\frac{\lambda}{L}\right)^2 + \left(\frac{\lambda}{L}\right)^2 e^{-\frac{\lambda}{L}} \quad \text{.....................................(2.57)}$$

This equation is valid for one charge carrier and can have the highest value of 0.5. Electrons and holes that have separate effective drift lengths, λ_e and λ_h, correspondingly, should be added. Equation 2.57 is obtained by integrating equation 2.56 throughout the inter-electrode length L for a consistent charge density for equally irradiated and not irradiated diodes. The proportion of these two integrations can provide the SE outcome shown in the previous equation. Based on computed effective drift lengths [52], the hole (λ_h) and electron (λ_e) effective drift lengths can be associated as:

$$\lambda_h = 0.4\lambda_e \quad \text{...(2.58)}$$

The factor 0.4 is principally owing to the variation in hole and electron motions and trapping times. A fitting to SEs can be rendered utilizing the abridged equation:

$$SE = \frac{1}{1+K_c\Phi} \quad \text{...(2.59)}$$

Where K_C is the damage constant for the signal efficiency. K_C hangs on the trapping damage constant (K_τ), the inter-electrode distance (L), and the drift velocity (v_D):

$$K_C = 0.6LK_L = \frac{0.6LK_\tau}{v_D} \quad \text{.....................................(2.60)}$$

Where, $\frac{1}{\lambda_e} = \frac{1}{\lambda_0} + K_L\Phi \approx K_L\Phi$ and $K_L = \frac{K_\tau}{v_D}$ and that λ_0 is large, v_D is the drift velocity saturated and K_τ is the damage constant for the electron effective trapping time. Abrupt inter-electrode spacing describes the enhanced radiation tolerance execution of 3D sensors whose geometry advantages from this, jointly with the probability of adopting the thickness of the substrate, which offers the initial quantity of charge published by an ionizing particle.

An anthology of signal competence vs. fluence for planar and 3D sensors handled on a float zone (FZ) and epitaxial substrates are demonstrated in fig. 2.22. The SEs of planar FZ and epitaxial sensors, computed following irradiation at several fluences, are described in the literature [53-63]. The SE was calculated utilizing either low-intensity infrared lasers (3D) or least ionizing particles (3D and planar), which allocate charge evenly between the electrodes; therefore, the formalism depicted above relates. Fig. 2.22 depicts that the SE reduces fewer following severe irradiation for devices including a smaller inter-electrode distance L.

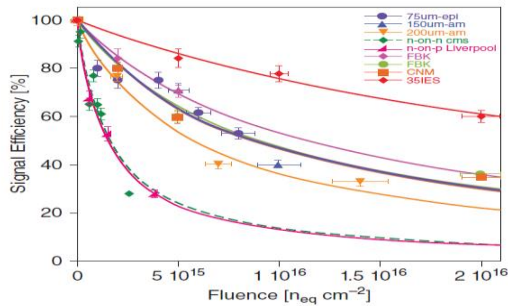


Fig 2.22: Anthology of signal efficiencies vs. fluence of silicon sensors planar and 3D handled on either float zone or epitaxial substrates with inter-electrode distances from 35 (3D sensor) to 285 microns [4].

Slim silicon substrates can thus be a decent explanation for radiation damage in rough conditions if the noise of the readout electronics is minimally adequate to assure a nice signal-to-noise ratio [64-67]. A bunch of remarkable improvements have been made new in this trend through the advancement of new readout chips [68].

A fascinating process that has been noticed mostly in irradiated thin silicon sensors, is the existence of overflow of charge owing to charge multiplication at lofty bias voltages, creating the signal amplitudes yet surpassing the pre-irradiation amounts. The multiplication is produced by impact ionization owing to hot electrons shifting in the elevated electric field that grows close to the intersection in the irradiated sensors. Charge multiplication has been autonomously noted by numerous research clusters in the planar pad and strip detectors afterward exposure to huge radiation

fluences [68-73]. Extremely elevated bias voltages, in the order of 1000 V, are usually employed in order to achieve the crucial electric field quantities (of the order of 20 V/μm), triggering the onset of avalanche effects. Alongside experiments of collected charge with LHC-like readout chips, additional research (e.g., by the edge transient current technique [73]) targets a profound knowledge of the charge multiplication occurrence and its modeling [74, 75]. Furthermore, amended sensor designs alleviating the electric field control are being explored in order to permit dependable manipulation of charge multiplication in forthcoming research [76,77].

2.6 Ways of Controlling Radiation Damage

Radiation damage is a vital concern for the silicon sensors while using it in High Energy Physics applications. Though it might not be easy to stop it, several techniques can be implemented to lessen some of its results of it.

2.6.1 Surface Damage

The rise of positive oxide charge towards an extremely significant amount can trigger numerous distinct concerns. Amongst them the highly pertinent are the following:

- In p-in-n devices, a sturdy alteration of electric field distribution at the surface, conceivably taking to projected breakdown, as well as an enhanced inter-electrode capacitance following irradiation.
- In n-in-p and n-in-n devices, the initiation of a surface electrons coating will ultimately short all the segmented n+ readout electrodes, appallingly conceding position resolution.

There are some well-known solutions for the second problem, such as (a) p-spray, (b) p-stop, and (c) moderated p-spray [77] are obtainable to thwart the surface inversion layer and avert the shorting of n+ electrodes. Because of numerical simulations, the comportment of these techniques is incredibly perfectly appreciated [78]. The flawless selection of isolation techniques is however not always feasible, but by appropriately assessing the various alternatives, it is conceivable to discover the finest one for a particular application. The key factors that should be maintained are:

- Breakdown voltage equally prior to and following irradiation, to be capable to conduct the device at optimum bias
- Inter electrode capacitance to regulate the noise budget
- Inter electrode resistance, essential for proper isolation

All of the solutions have both sides of the coin. A summary is discussed below:

1. **p-Spray:** Comprising of a medium-dose insertion of p dopant on the n+ side of the wafer. This method has the major gain of being extremely easy. The anticipated outcome is a charge reparation of the surface electron layer that is created as a result of the positive charge entombed in the oxide. The key drawbacks of this method are associated with a somewhat low breakdown voltage beforehand irradiation, instigated by the comparatively elevated doping concentration of the p-spray area in interaction with the n+ electrodes, whose potential inclines to shadow the substrate potential, and by a greater inter-electrode capacitance. It should be remarked, nevertheless that the decreased breakdown voltage before irradiation is not essentially a significant concern since the entire device can be conducted at instead small bias voltages. Following irradiation, the total oxide charge strength boosts, which outcomes in smaller electric fields, greater breakdown voltages, and smaller inter-electrode capacitances.
2. **p-Stop:** It is a solution aimed to disrupt the continuous elongation of the surface electron layer with local high-dose p+ implants enveloping the readout electrodes. The finest geometric enactment of p-stops is with tight implantations to curb the pairing with the substrate bias and hence enhance the sensors' breakdown voltage. In this situation, the surface electron layer is in immediate connection on one side with the n+ junctions and will thus be grounded, and on the other side, it is in immediate connection with the high-concentration p+ implant. The breakdown voltage of the p-stop is usually elevated prior to irradiation, but, as the oxide charge improves, it begins reducing. If the inter-electrode capacitance is apprehensive, it raises the charge oxide concentration. The key improvement of the p-stop above the p-spray is the robust separation amongst electrodes.
3. **Moderated p-spray:** It is a method that comprises merging both p-stop and p-spray with a moderate-/soft –dose of regular implant and an elevated dose of the limited implant to combine both properties. As long as breakdown voltage is the issue, it begins small, and it rises with irradiation dose (typical of p-spray). If the p-spray layer is treated with a low-dose implant, to amplify breakdown prior to irradiation, it might occur that the improved oxide charge will end in full reparation and surface inversion. The formation will act in the same way as a p-stop, with breakdown voltage reducing as the total radiation dose rises.

Comparably, the inter-electrode capacitance will primarily reduce (p-spray) and then boost (p-stop) [79].

2.6.2 Bulk Damage

Bulk damage is another key issue and can be altered in three major ways:

1. **Material Engineering:** This method comprises mostly of the development of substrates with the type and quantity of impurities efficient of alleviating the defect structure accountable for leakage current production and entrapping. Numerous experiments were staged in the 1990s heading to crucial assumptions on the issue of the usage of oxygen. Oxygen is considered to seize vacancies in steady and unbiased point defects following irradiation, leading to a further homogeneous effective doping change in various substrates [80-82]. The advantageous impact of oxygen is restricted to steady destruction, and it was demonstrated that reverse annealing might be better managed following proton but not after neutron irradiation. Other materials such as GaAs [83] and newly diamond [84] have drawn interest due to their extremely small leakage current owing to bigger band gaps. In spite of the elevated price, specifically that of monocrystalline diamond substrates, numerous remarkable innovations have been made utilizing the less costly polycrystalline diamond with laser-ablated 3D geometries [85].
2. **Device Engineering:** This method comprises the layout skilled at beating the structural shortcomings of irradiation. The earliest pioneering model adjustment for tough radiation environments of silicon devices comprised shifting from the conventional p-on-n to n-on-n structures [86]. This selection, jointly with the utilization of oxygenated substrates, permitted the current pixel devices at LHC experiments to endure up to a fluence of 1×10^{15} n_{eq} cm^{-2}. The next revolution was then to shift to n-in-p formations, thanks to the manufacture of high-resistivity p-type substrates [87]. Together new designs benefit from the improved electron compilation for their greater agility, their greater signal owing to the lengthier electrons' effective drift length, and conserved spatial resolution since the junction always depletes from the n+ side. The subsequent crucial milestone in device engineering was the usage of 3D designs, which allocates crucial alterations to the conventional silicon detector theory.
3. **Device Operational Conditions:** This process can help alleviate some of the impacts of irradiation. The process at elevated bias voltages permits a lengthier carrier drift beforehand trapping and consequently a greater signal and conceivable charge multiplication with the improved

signal; the process at temperatures just underneath 0°C can regulate the amplitude of radiation-induced leakage current and failure owing to thermal runaway; and forward bias process subsequently elevated fluences making usage of the material alteration, with resistive I-V characteristics at both forward and reverse bias, can be utilized to assure the junction polarization at forwarding bias with little applied voltages [25]. Lastly, the procedure at cryogenic temperatures, specifically at 130 K, has demonstrated encouraging outcomes with improved speed and recuperation of the charge at both reverse and forward bias following intense irradiation. The Lazarus effect was comprehensively examined in the 1990s, but it was slumped from the major LHC arena owing to the complexity of running a huge scheme at liquid nitrogen temperatures [88-90].

Chapter 3
ATLAS Detector in CERN

The biggest instrument within the globe, the Large Hadron Collider (LHC) was established between 1998 and 2008, with the good cooperation of the ECU organization of nuclear analysis, called the Conseil Européen pour la recherche Nucléaire (CERN). The key purpose of the accelerator is to explore through empirical observation and evidence the originated particles via scientific theory theories. It in addition provides the prospect to investigate through empirical observation the theories pertinent to Higgs, substance additional dimension, etc. The accelerator includes a 27km long and 37m wide undergrounded double ring of the superconducting proton-proton collider, that progressed from the Large Electron-Positron collider (LEP) in 2000 [91]. The development of LHC likewise nucleon machine on top of LEP doesn't have the similar synchrotron radiation problem and would ideally have lengthier bends and gouger straight segments for the similar perimeter wherever the antecedently created was a cheap answer. The superconductive RF fissures and electromagnets at 2 K and smaller temperatures are utilized within the model by levying chemical elements for antagonistic the tiresomely reducing electrical conduction with a rising magnetic flux. The augmented heat transport property, the low bulk consistency, empowers the chemical element to penetrate to the core of magnet windings and retain the equilibrium throughout the LHC method. A major objective of the LHC lingers to divulge the physics outside the Standard Model with the facility of mass collision forces of up to 14 TeV and exceptional luminosity (10^{34} $cm^{-2}s^{-1}$). This concern is to research the number of incidents per second, spawned in the LHC collisions can be derived from:

$$N_{event} = L\sigma_{event} \quad \text{……..…………………..(3.1)}$$

Where σ_{event} is the cross-section used for the incident under investigation and L is the machine luminosity. The machine luminosity hinges only on the beam constraints and can be inscribed for a Gaussian beam distribution as:

$$L = \frac{N_b^2 n_b f_{rev} \gamma_r}{4\pi \varepsilon_n \beta^*} F \quad \text{……………….……..…….(3.2)}$$

Where N_b is the number of particles per bunch, n_b is the number of bunches per beam, f_{rev} is the revolution frequency, γ_r is the relativistic gamma factor, ε_n is the normalized transverse beam emittance, β^* is the beta function at the collision point, and F is the geometric luminosity reduction factor owing to the crossing angle at the interaction point (IP), which can be expressed as:

$$F = (1 + (\frac{\theta_c \sigma_z}{2\sigma^*})^2)^{-\frac{1}{2}} \quad \text{.................................(3.3)}$$

Here θc is the full crossing angle at the interaction point, σ_z is the RMS bunch length, and σ^* is the cross RMS beam size at the interaction point. These alleged spherical beams, with $\sigma z \ll \beta$, and with identical beam factors for each beam. to look at the bizarre events from LHC collisions, each high beam energy, and high beam intensities square measure necessary.

The fundamental arrangement of the existing LHC is recounted in figure 3.1. The LHC is outfitted with eight arcs and eight straight sections. Four of the straight sections accommodate the LHC experiments whereas the other four are used for auxiliary facilities and beam abort. Points one and five, these two straight sections accommodate the A toroidal LHC apparatus (ATLAS) detector and therefore the Compact muon solenoid (CMS) detector correspondingly with the association of large hadron Collider forward (LHCf) at point one and TOTal cross-section, Elastic scattering, and diffraction dissociation measurement at the LHC (TOTEM) at point five. The other 2 experiments, A Large Ion Collider Experiments (ALICE) and Large Hadron Collider beauty (LHCb) are positioned at point two and point eight correspondingly for examining the results of the many collisions amongst Pb-Pb and p- Pb. Pb-Pb collision is rendered with a layout luminosity of $10^{27}cm^{-2}s^{-1}$ at the middle of the mass of 5.5 TeV per nucleon pair to get the minuscule capacities of such stuff. These are recognized because of the quark-gluon plasma, and reviewing them directs us to grasp the progression of the universe nowadays. LHCb investigates the charge parity resistance of b-hadrons to explicate the Matter-Antimatter imbalance of the universe. The ring is organized by 9600 magnets in a very mixture of dipoles, quadrupoles, sextuples, octupoles, decapods, etc., amongst that 1232 dipole magnets are used to sustain particles in a spherical path. The

highest order of various magnets is used for guiding the beam to spice up the particle contacts in four junction points of committed experiments.

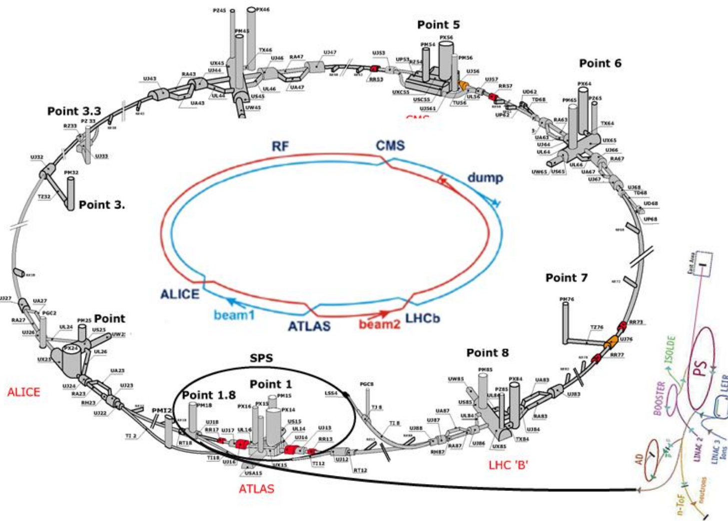


Fig 3.1: Large Hadron Collider Design. The enclosure of the larger ring displays the two parallel beamlines and four collision points of dedicated experiments: ATLAS, CMS, ALICE, and LHCb [92].

The CERN accelerator is a complex structure that accelerates particles to elevated energies in consecutive growing directions. Every specific part of LHC enhances the beam energy, before shifting the beam into the subsequent one within the consecutive fast string. In the LHC, the ultimate fast part of this monumental device, the beam area unit sped up to the best energy of 6.5 TeV. The container of hydrogen is used to harvest protons from hydrogen atoms using the electric field. Linac 2, the earliest accelerator within the franchise, quickens the protons to realize the energy of 50 MeV. The beam is later on ironed into the proton synchrotron Booster (PSB) and achieves a 1.4 GeV energy state. Next, the proton synchrotron (PS) enhances the beam to 25 GeV magnitude and sends it into the Super Proton Synchrotron (SPS). At this point, the accelerated protons achieve energy up to 450 GeV. The protons are ultimately transported to the double beam pipes of the LHC, wherever one beam distributes clockwise while the additional one distributes in an anticlockwise manner.

The whole procedure necessitates four minutes and twenty seconds to load a single LHC ring, and twenty minutes overall to realize the highest energy for the protons (~6.5 TeV). In a typical operational circumstance, beams may be circulated for prolonged cycles of your time. As presently because the beams contain most of the energy, they're junction rectifiers into four colliding nodes, that area unit ALICE, ATLAS, CMS, and LHCb detectors. The energy at the collision points can be up to 13 TeV.

3.1 Upgrade of LHC

The LHC is still the most important accelerator within the globe for at least the following twenty years. It completing its operation is the most important for the ECU Strategy for high-energy physics. This policy has been embraced by the CERN Council Associate in association with the goal of the high-energy physics Strategy of America and, to a selected degree, Japan. To expand its invention capability, the LHC would require a key improvement within the 2020s to expand its operability by a further decade and to reinforce its physical property (and so collision rate) by a factor of 5. The essential advancements necessitate around ten years to model, test, and perceive new equipment. The novel machine alignment, the High physical property LHC (HL-LHC), can depend upon many crucial pioneering sorts of machinery correspond to outstanding scientific tasks. These involve amongst others: the latest 11–12 T superconducting magnets; extraordinarily dense superconducting craters for beam spin with ultra-precise part control; the contemporary ability for beam collimation; and high-octane superconducting links with much zero energy indulgence.

HL-LHC unites the endeavors and R&D of a considerable international population within the direction of the glorious HL-LHC aims and participates in forming the European research area (ERA) as a polar purpose of worldwide analysis collaboration and leadership in leading-edge experience and technologies. HL-LHC depends on solid involvement from many allies, in specific from the highest American and Japanese laboratories. This involvement is going to be necessary for the implementation of the building stage as a worldwide venture. for example, the US LHC Accelerator R&D Program (LARP) has established some crucial technologies

for the HL-LHC, like the large-aperture niobium-tin (Nb3Sn) quadrupoles and therefore the crab cavities. The suggested management model is being reworked and is currently tailor-made to back the assembly part.

3.2 HL-LHC in a Nutshell

The new LHC standard program, specified in June 2015, is exhibited schematically in fig. 3.2. Subsequently, electrical connections between the superconducting magnets (and countless other merging activities) in the Long Shutdown 1 (LS1), the LHC has functioned in Run 2 at 13 TeV with center-of-mass energy from 3 June 2015 and has gradually amplified the luminosity achieving the trifling strategy luminosity of 1×10^{34} cm^{-2} s^{-1} on 26 June 2016. Despite a decreased amount of clusters (about 2200 cf. 2800 nominal) a pinnacle luminosity up to 1.2×10^{34} has been consistently achieved in 2016. This crest is mostly thanks to decreased emittance from the injectors and a β^* amount of 40 cm (cf. 55 cm minimal value) at the high luminosity interface places. This outstanding performance, collectively with an accessibility that is significantly greater than in earlier years, has given a whole combined luminosity of about 190 fb^{-1} for the year. In the cycle 2019–2021 the LHC has optimistically advanced to improve the highest luminosity. Restrictions in the layout of the minimal LHC are anticipated to permit about two times the nominal model execution. The standard curriculum for the next ten years is portrayed in fig 3.2, while fig. 3.3 demonstrates the probable progression of peak and incorporated luminosity.

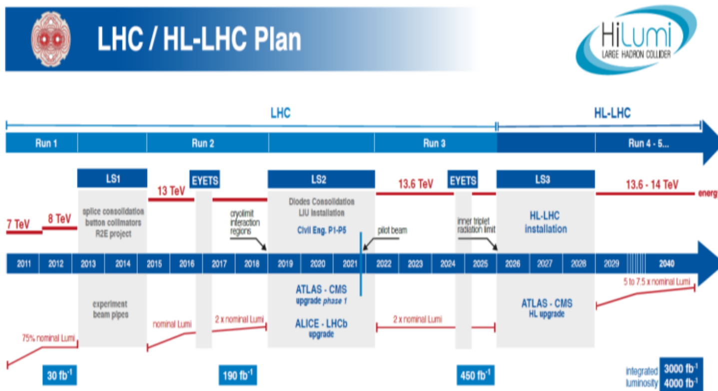


Fig 3.2: Standard proposal for the following decade and beyond demonstrating the energy of the collisions (upper red line) and luminosity (lower green lines). [93]

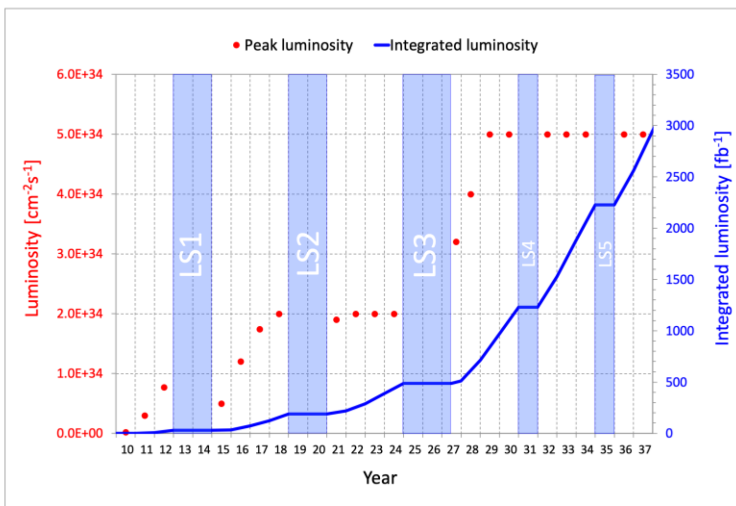


Fig 3.3: LHC luminosity scheme until LS5: both crest (red dots) and incorporated (blue line) luminosities are shown. Major shutdown cycles are also demonstrated. [93]

Following Run 3, the arithmetic gain in operation of the accelerator with no wide luminosity growth outside its model and supreme values can become stripped. The operational time needed to divide the statistical inaccuracy of a specific magnitude, when 2020 is already an additional 10 years. Thus, to sustain scientific development

and utilize its full capability, the LHC would force to possess a big rise in its luminosity after 2020. Therefore, the CERN Council approved the European Strategy for particle physics in 2006 [94], its first concern was 'to utilize the physics possibility of the LHC. A consecutive key luminosity improvement, inspired by physics outcomes and method understanding, is expedited by dedicated R&D, the European Strategy for particle physics has been incorporated into the European Strategy Forum on Research Infrastructures (ESFRI) Roadmap of 2006, as has the renewal of 2008 [95]. The precedence to fully utilize the capability of the LHC has been recently verified because the main concern amongst the 'High priority large-scale scientific activities' within the latest European Strategy for particle physics – Update 2013 [96]. This revision was accepted in Brussels on 30 May 2013 with the following phrasing: 'Europe's prime priority ought to be the exploitation of the complete potential of the LHC, as well as the high luminosity upgrade of the machine and detectors to gather 10 times more knowledge than within the initial design, by around 2030'[93].

The standing of the LHC luminosity elevation for the forthcoming high energy physics has additionally been reiterated within the May 2014 commendation by the particle physics Project Prioritization Panel (P5) to the High Energy Physics Advisory Panel (HEPAP), which successively counsels the US Department of Energy (DOE) [97]. The suggestion, an important introduce the renewing of the US policy for informed, declares the subsequent: 'Recommendation 10: The LHC upgrades represent our highest-priority near-term giant project' [93].

In the year 2012 in Japan, a piece of writing by a commission within the informed society determined that an e+e− linear collider and a large-scale neutrino detector would be the first ventures in Japan, with the notion that the LHC and its development are followed de facto. The revised KEK roadmap in 2013 declares that 'The primary plan at LHC/ATLAS is to persistently contribute to the analysis and to require a preventive initiative in development programs within the international alliance at each the accelerator and detector amenities. As this helped, the ATLAS-Japan cluster has commenced rigorous R&D on the detector enhancements, and also the KEK refrigerant Science Center has begun the R&D for the HL-LHC separation dipole magnets (D1).

From such a perspective, CERN made the High Luminosity LHC (HL-LHC) project at the end of 2010 [98]. Began as model research, and following the consent of the CERN Council on 30 May 2013 and the inclusion of a steady part of the HL-LHC budget in the CERN Medium Term Plan (MTP) granted by the Council in June 2014, the HL-LHC has to turn into CERN's key building plan for the next decade. The text of the Conceptual scientific requirements and the Preliminary Design Report [99] are crucial deliverables of the FP7-HiLumi LHC Design Study. Additional measures have been carried out in 2015 to obtain a comprehensive authorization of the HL-LHC:

- Cost & Schedule Review (international committee of specialists, comprised of the CERN Machine Advisory Committee accompanied by extra experts). Initial gathering on March 9-11, 2015. The incredibly optimistic article is accessible upon request.
- Alteration of the design for civil engineering, further fitting to the factual requirements and circumstances;
- Incorporation into CERN's MTP of 2015 of the full budget for the years 2016-2020 (the 5-year contained by MTP granted in 2015), with the suggestion of the complete CtC (Cost-to-Completion) of the project up to complete fitting in 2026. The material expense is about 950 MCHF, without incorporating the preliminary Design Study and prototype stages.

Because of the above-stated steps, the project and its budget for the building were granted for the phase of the MTP by the Council at its 16 September 2015 Meeting.

In spring 2016 the CERN executives presented to Council the plan for a global appreciation of the HL-LHC, explaining the ambitions of the update, the physics issue for the HL-LHC, and the equipment disputes. The proposal, [100], includes all the project cycles involving fitting and commissioning in 2026, and provides a complete material expense for the HL-LHC of 950 MCHF. It should be mentioned that this number includes the High Luminosity LHC, i.e. the raw material for the collider with its structure, but it does not comprise the expense of the detector upgrade. The paper was accepted in the 181st session of the CERN Council on 16-17 June 2016. Astonishingly, HL-LHC has come to be the first project officially sanctioned by the CERN Council ever since the ultimate authorization of the LHC in 1996.

The key purpose of the High Luminosity LHC layout examination was to ascertain a set of beam parameters and the hardware composition that will facilitate the LHC to reach the subsequent objectives:

- A peak luminosity of 5×10^{34} cm^{-2} s^{-1} with leveling
- An incorporated luminosity of 250 fb^{-1} per year with the target of 3000 fb^{-1} in around a dozen years past the development. This incorporated luminosity is around ten times the anticipated luminosity achieved in the initial twelve years of the LHC lifetime.

The principal objectives are the fitting of the primary hardware for the HL-LHC throughout LS3, planned for 2025–2028, completing the hardware commissioning at engine re-start in 2029 while considering all actions to ensure high effectiveness in the process until 2035-2040.

Because all apparatus is being constructed with a 50% margin concerning the rapid heat accumulation and the incorporated radiation dosage, the idea of supreme performance has been specified, where all edges are utilized for performance growth. By utilizing these boundaries, it should be feasible to push the system's highest directed luminosity to about 7–7.5 × 10^{34} cm^{-2} s^{-1} rising the median pile-up, i.e. the number of events per bunch crossing, in the detectors up to about 200. This luminosity level should facilitate the assortment of up to 300–450 fb^{-1}/year providing the tests can absorb this pile-up level. In terms of overall cohesive luminosity, the final performance relates to a value of around 4000 fb^{-1}.

Likewise, all magnetic circuits have been designed with a 10% allowance concerning driving at a minimal beam energy of 7TeV. By applying these margins, it could be hoped to drive the LHC from the magnet circuit viewpoint at a beam energy of 7.5TeV. Still, such an expansion in the beam energy indicates supplementary tasks for many other structures (e.g. the machine protection and power systems and the collimation and beam dump systems) and can thus not be taken for granted at this point. Although the HL-LHC project standard is 'only' for 7.0 TeV and does not involve this ‘ultimate beam energy' in its requirement, the probability of prospective individual energy raised to 7.5 TeV should be unambiguously thought in the ongoing HL-LHC upgrades. If considerable additional endeavors and improvements are essential for this energy, which are not viable in simple synergy within the HL-LHC

resource envelope, then at a minimum the restrictions and necessary supplementary improvements should be discovered.

All of the hadron colliders in the earth before the LHC, have yielded a collective overall combined luminosity of about 10 fb^{-1}. The LHC provided approximately 190 fb^{-1} by the end of 2018 and should achieve 450 fb^{-1} in its initial 13–15 years of operation. The High Luminosity LHC is a key, exceptionally difficult, improvement. For its effective understanding, a lot of crucial novel technologies have to be established, substantiated, and incorporated. The effort was commenced as soon as possible: theories were flowing at the start of the LHC building [101] and this persisted during the building [102]. From 2003 forward, LARP has been the major and constant motor for technological progress dedicated to the LHC upgrade, paired in Europe by a research endeavor organized by the EC-FP6-CARE program (HHH and AMT networks and NED program). Later a period throughout which the exaltation was perceived in two phases, the initial one via reputable Nb-Ti technology (support by the FP7-SLHC-PP program) and the subsequent founded on novel Nb3Sn technology and succeeding the overthrow of the Phase-I advancement project, all revisions were focused in 2010 underneath the recently formed High Luminosity LHC Project. The initial move involved introducing a Design Study underneath the auguries of FP7 with the running title 'HiLumi LHC'. After authorization by the European Commission (EC) in 2011, FP7-HiLumi LHC has been involved in originating a new international alliance for the LHC, complementing the essence of the global consumer society of the LHC experiments. The High Luminosity LHC project is also acting in close alliance with the CERN project for the LHC Injector complex Upgrade (LIU) [103], the fellow ATLAS and CMS upgrade projects of 2019–2021 and 2026–2028.

3.3 ATLAS Future Plans for HL-LHC

The HL-LHC is specifically distinguished by its targeted beam bunches filled with 2.2×10^{11} protons per bunch (the borderline being 1.15×10^{11}), low emittances, and fine-tuned beam optics to enhance the chance of proton-proton interactions. the quantity of collisions per bunch crossing, termed as the pileup, μ, at the crucial HL-LHC mode of procedure is anticipated to attain 200. this can be a massive uphill

move regarding the LHC layout and presently realized complete of up to around 75. As some of the present detector sub-systems of ATLAS are not proficient in taking part optimally at $\mu \approx 75$, the best luminousness is flattened down to right down to 58 by cacophonous beams at the start of each LHC fill [104-105]. For the remainder of the pack, μ reduces, ultimately achieving values right down to 10, before beams are abandoned. This methodology stemmed from a very median collision of ≈ 38.3 in 2017. The sensitivity to perpetually growing pileup circumstances is of a particular apprehension to the experimentation since sure resources scale exponentially aside from linearly with μ, thus making extrapolations and specific forecasts more durable to realize than they need be below the lesser pileup circumstances distinctive of the data on which current annotations are grounded. without an acceptable improvement of basic hardware and software system structures, ATLAS wouldn't be capable to resist the rougher operative circumstances of HL-LHC [106].

The ATLAS detector can endure a key development within the 2 stages that are regular thus far and henceforward delineated as section 1 and phase 2, correspondingly, in synchronization with the HL-LHC schedule. The principal enthusiasm and chance of modernization within the many sub-systems are outlined by the physics significance and by the convenience of the state-of-the-art types of machinery. a further matter for the enhancements is material maturing, involving technology outmodedness, providing the ATLAS detector was instructed over twenty-five years ago and several other of its components were created and mounted over ten years ago. The radiation doses and injuries experienced by the sensors and electronics throughout the Run 1 (2010–2012), Run 2 (2015–2018), and Run 3 (2021–2023) procedure ought to be counted as well [106].

The ATLAS collaboration is in control of all the facets of the various detector parts and processing. This signifies a huge human strive and a particular technological accomplishment. The detector ponders 7000 tons and sizes 46m in length and 25m in diameter as can be seen in fig. 3.4. over 3000 physicists from around 182 organizations in 38 nations are collaborating as of these days. The ATLAS detector can be divided corresponding to its major operational units, specifically, the inner tracker, calorimeters, lepton spectrometer, and trigger and data acquisition. the

subsequent segments represent a concise outline and some features from the renovation technical design factors per sub-system.

3.3.1 Inner Tracker

The current tracking detector will be retired and swapped by a completely innovative Inner Tracker (ITk). It includes one of the extremely crucial techniques of the enhanced detector which will perform a critical role in the data taking at extremely high pileup. ITk is an all-silicon scheme that comprises a pixel detector at a modest radius and a sizable area strip detector containing it. It will be mounted as a monolithic division into the center of the ATLAS detector.

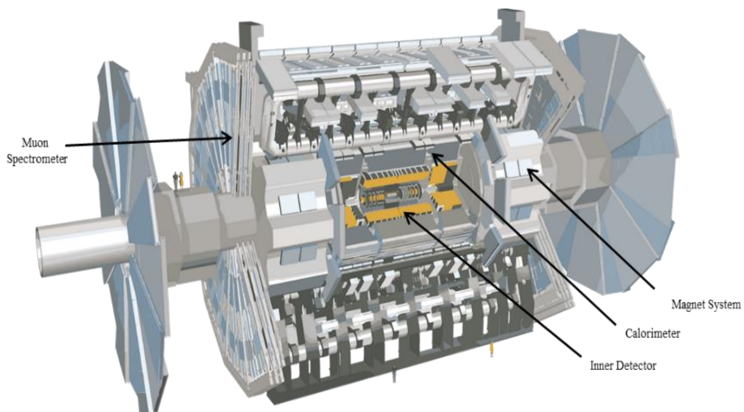


Fig 3.4: ATLAS Detector in comparison with human body [107].

Excellent hermeticity, the establishment of an adequate quantity of hits on track, as well as reduced tracking execution mortification due to material inside the detector volume are essential constraints in the engineering layout of ITk. The employment of these provisions will guarantee the capability to recognize charged particles with elevated proficiency and transparency and calculate their assets with extreme accuracy in the existence of up to the middling pileup of 200 that is anticipated at the HL-LHC The upgraded detector must at the minimum sanctuary, and if conceivable augment, the physics act of the existing Run 2 detector, underneath the Phase 2 functioning circumstances.

The collective Pixel and Strip ITk detectors offer a total of 13 hits for tracks with $\eta < 2.6$, with the exemption of the barrel/endcap conversion of ITk Strip, where the hit count is 11 hits. The ITk Pixel endcap scheme is assembled to provide a least of at minimum 9 hits after the end of the Strip detector exposure to $|\eta| \approx 4$. The full ITk will be reading out at a 1 MHz L0 rate in the single L0 trigger scheme.

3.3.1.1 ITk Pixel Detector

The information achieved over twenty years of building and management of the present ATLAS pixel detector aids like a foundation for the improved layout which was chosen from among a spread of sensor technologies, involving high-resistivity, planar and 3D silicon detectors. The newest ITk pixel detector is a hybrid fabrication of a high-resistivity silicon detector bump-bonded to a CMOS binary chip readout at a very high speed [105]. Novel technologies have been examined thoroughly and explained to acclimatize to the HL-LHC circumstances.

Meticulous simulations are accomplished to reinforce and freeze the outline and crucial physical factors of the pixel pattern before the mechanical manufacture will begin. The pixel detector includes four-barrel layers and four layers of endcap ring as can be seen in fig. 3.5. the 2 innermost barrel layers and also the inner-most endcap ring layer can be replaced, the others are constructed to operate for the complete life of the HL-LHC. The barrel predisposed style theory with slanted sensors within the permits for various hits per layer (tracklets) and fewer materials to be resisted for a specific lowest incidence angle. These advances to enhanced d0 and z0 resolution and superior tracking effectivity are attributable to having many tracklets as close as possible to the contact point. The endcap layout includes distributed rings (instead of flat disks), called optimized rings, such this implausibly specific arrangement offers a steady amount of hits vs. η. The bigger territory is coated by the pixel volume with an increased amount of rings at very high η.

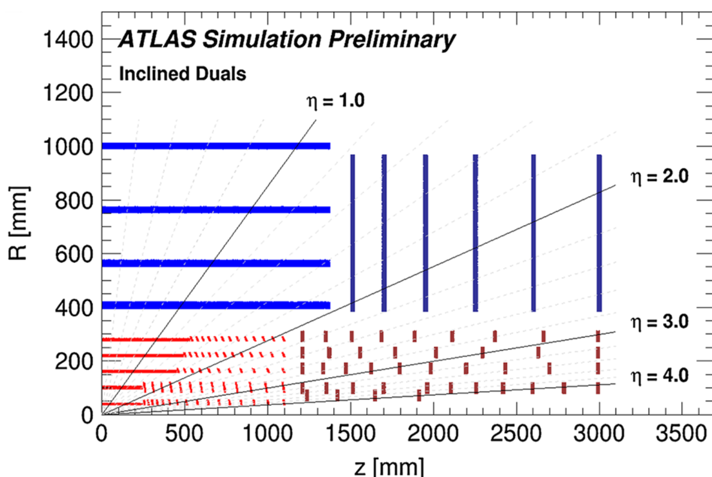


Fig 3.5: A graphical interpretation of the ITk design for HL-LHC with the coverage of the Pixel/Strip detector (in red/blue).

The new 3D pixel sensors are comprised of an active silicon layer of 150 μm thickness and a passive support layer of 100 μm thickness. Furthermore, the front-end chip is comprised of a 150 μm thick silicon wafer including a 20 μm diameter Sn-Ag bump-bond per pixel channel. The complete number of channels is more than 400 M (which is 5 times greater than the existing Pixel detector). This inhabits the innermost pixel layer (L0) and has comparatively larger thicknesses. Planar pixel sensors can be 100 to 150 μm thick of active silicon in layers 1 (2–4). The outermost barrel layer (4) is being pursued by Monolithic CMOS pixel sensors as modules. The complete readout will be strengthened by the three outer Pixel layers, barrel, and endcaps at 4MHz. A complete readout at 4 MHz would need an exorbitant number of data cables for the two inner Pixel layers; this portion of the detector will just help complete readout at 1 MHz and will be read out at L1.

3.3.2 The New Small Wheel system

The New small Wheel system includes 2 five-meter radius wheels (one for A-side, another for the C-side) within the end-cap region ($1.3 < |\eta| < 2.7$). each wheel is built by 2 outer little strip thin gap chambers (sTGC) wedges (utilized principally for the

trigger, for bunch crossing recognition, and vector chase) and 2 inner micro mega wedges (utilized principally for tracking with a spatial resolution of fewer than one hundred microns).

The New small Wheels target is to decrease the negative muon triggers made by noise or unintentional correlations within the end-cap region, by making a correlation amongst the present detectors, the large Wheel, and therefore the New little Wheel. As delineated in fig. 3.6 (right), solely the theoretical “A” track is allowed, whereas the “B” track (generating solely hits within the huge Wheel) and therefore the “C” track (not indicating to the contact point) would be abandoned. the development of the bureau is presently ongoing, and therefore the bureau detector is anticipated to be complete for installation by the tip of 2021 [107].

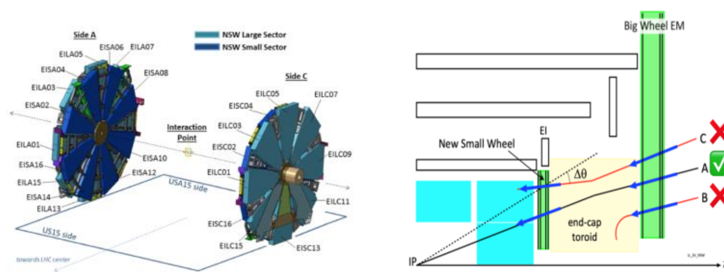


Fig 3.6: Left: the layout of the two New Small Wheels, for large and small sectors. Right: working principle of the track selection trigger of the NSW (transverse view) [108].

3.3.3 Calorimetry

It is not regular to change the sampling parts (i.e., the lead bars and scintillating tiles) for the LAr and Tile calorimeters, correspondingly. still, the anticipated rise within the fluxes of particles from the HL-LHC needs the substitute of the prevailing electronics after Run 3 as many on-detector parts won't be able to face up to the planned radiation dose of HL-LHC.

The latest trigger methodology necessitates access to the digital data from each calorimeter cell at a forty MHz rate and with the highest latency of regarding 1.7μs. Adjusting the readout to perpetually digitalize and transmit the calorimeter-cell data off-detector utilizing high-speed optical links has an additional profit to cut back

single event effects (SEE) within the digital pipelines. The mathematical accuracy, the improved exactness within the energy calibration, and therefore the lessened level of electronics noise, aiming comparable values to the offline data, can enhance the trigger property significantly. The calorimeter data can comprise the remodeled and tag energy, time (i.e., bunch crossing identification or BCID), and quality issue for every cell.

3.3.3.1 LAr Calorimeter

The readout methodology registers the energies within the scale of 0.5 MeV to 3 TeV for around 182 k channels. The signals are wrought and digitized and delivered along to the trigger and also the data acquisition (DAQ) techniques. the best readout ratio at the L1 trigger is presently 110 kHz. The readout structural design includes the front-end, FE, (on the detector), and back-end, BE, (off-detector) electronic modules. a huge FE (58 crates) is crucial because of implementation constraints, e.g., to accomplish the mandatory resolution and incident magnitude relation. The FE operates, on one aspect, per-channel analog handling, 12-bit ADC conversion, and optical data broadcast at 1.6 Gb/s to the BE electronics, and on the opposite aspect, analog signal computation and broadcast to the L1 calorimeter trigger (L1Calo). The BE completes digital filtering, computes the accumulated energy, and delivers the readout interface to DAQ [106].

The phase 1 development can stress enhance that calorimeter practicality associated with L1 triggering. the degree of data can expand by a part often, whereby a present trigger tower can have ten supercells, every supercell fitting to 1 of four layers comprehensive of the LAr calorimeter (in the entire η-range) and is four times higher in Δη within the 2 central coatings (for $\eta < 2.4$). The FE analog totaling electronics are going to be substituted with LAr Trigger digitizer Boards (LTDB) and these digitized signals are going to be handled distantly by the LAr Digital process System (LDPS) also BE, that processing functions as an interface to the recent L1 calorimeter trigger approach [106].

For HL-LHC in phase 2, an advancement of the readout electronics style is critical for a free-running program wherever all information is relayed off-detector. The phase 1 FE boards (FEB) are going to be swapped by FEB2 boards, whereas the LAr Signal

Processor System (LASP) hardware completion is going to be an advancement of the LDPS. the total data flow of detector signals digitized at forty MHz is going to be accessible within the LASP modules. this can allow a fortitude of adjusted cell powers and of signal times relating to the bunch crossing time involving a good modification for out-of-time pileup. the newest FE electronics components should be radiation repellent (up to thirty kGy). At high collision and over time the first attributes of the electronics appliances like dynamic range, linearity, noise, analog pulse shaping time, etc, mustn't be cut back. In phase 2 a significant constraint for the LAr update implemented by the TDAQ scheme is that the help for one MHz (up to four MHz) enables rate for processing, output bandwidth, and buffering ability. Again, the LAr scheme shall use knowledge managing, e.g., noise refusal and zero-suppression, to regulate the bandwidth needs of the trigger CPUs. this control and low-voltage (LV) power dissemination arrangement would require to be changed in phase 2 as of the restricted radiation forbearance of the present FE elements and compatibility with the newest TDAQ layout. the modern FE electronics can largely use voltages smaller than this one (1–4 V in its place of up to 11 V). The lv power supply is going to be additionally repositioned to an additional offered location that may be accessible in fast intervals throughout data-taking [106].

3.3.3.2 Tile Calorimeter

The proposal for the Tile calorimeter is to substitute the FE electronics and also the high-voltage (HV) control mechanisms. moreover, 768 PMTs containing the cells that are extremely subjected to radiation are substituted with the foremost recent prototype PMTs. The phase 2 TDAQ design anticipates a digital calorimeter trigger with larger coarseness and accuracy, contrasted to the present structure with analog adding that is accomplished on-detector. Tile digital trigger input is complete just for Run 4, not like Run 3 for LAr. In Phase 1, the Tile on-detector electronics can persist untouched, as can the trigger signal digitization completed by L1Calo Pre-Processor Modules (PPMs). The PPMs are outfitted with new TREX processors (Rear Transition modules) pushing signals to the new L1 trigger system.

Information is digitized at forty Mhz and forwarded off-detector, whereas most of the on-detector electronics and issues are pushed out of the detector, owing to the

accessibility of high-quality, high-speed optical links and receivers (e.g., established on the alleged GBT protocol). it's conjointly crucial for the part a pair of themes be steady with the newest trigger and dormancy seeable of the large rise of rate and pileup equated to those of the phase 1 upgrading. the provision to the electronics for preservation can develop by dividing the current super-drawer body into four components (called mini-drawers). Such segmentation into minor autonomous readout units can prohibit the number of unused cells due to malfunctions impacting a whole super-drawer. within the most awful state of affairs, the deceased zone would be a simple fraction of the region compact by a collapse within the existing scheme. the newest Tile on-detector electronics are maintained at intervals in these mini-drawers. moreover, the newest HV scheme is shifted to the far side of the detector radiation surroundings [106].

3.3.4 Muon Spectrometer

The muon spectrometer contains monitored drift tubes (MDT), Cathode Strip Chambers (CSC), endcap thin-gap chambers (TGC), and barrel resistive plate chambers (RPC). RPC and TGC are presently utilized for triggering. The muon detector components meet the factors for lengthier operative and bigger rates (and radiation doses) than initially expected, because of the fundamentalist original security issues, thence they'll not be modified.

In phase 2 a large portion of the FE on- and off-detector readout and trigger electronics for RPC, TGC, and MDT are substituted to be harmonious with elevated trigger rates and lengthier dormancy known by the new L0 trigger. the ability structure for the RPC, TGC, and MDT compartments and electronics would require to be switched because of module outmodedness, elderly, and radiation injury. A superior-η trigger is beneath concern to expand the angular acceptance for lepton detection. as of information from each beam-crossing from the TGC and RPC detectors are transferred to the deliberation chamber USA15, wherever the entire report is accessible for trigger handling. within the NSW zone (1.3 < |η| < two.7), the mm and sTGC compartments can along take the twin responsibility of trigger and accuracy cavities. The (barrel within little sectors seven and 8) BIS78 MDT compartments are swapped by combined bases of the latest RPC and small-

diameter MDT (sMDT) compartments to boost the trigger exposure during this space.

Adding to the enhancements of the detectors and of the trigger and readout electronics, the lv and HV power methodology of the muon spectrometer (together with controls and power supplies) also will be substituted to ensure a secure and consistent method throughout the entire operating part of the HL-LHC. The setup is to form innovative, exactly backward-harmonious mechanisms. In such an endeavor, the substitute is often stretched over a part of diverse years, between Phases two and three, at a time once these components reach the ending of their anticipated existence. This doesn't give house for defined modifications in an endeavor wherever AN utterly different power methodology would be designed [106].

3.3.5 Trigger and Data Acquisition

The layout of the improved style of the TDAQ theme validates a typical scenario with a single-level hardware trigger (L0) with the highest rate of one MHz and 10μs latency. The modified two-level design stipulates a Level-0 (L0) trigger rate up to 2–4 MHz and 10 10 latency, with a Level-1 (L1) trigger rate of 600–800 kHz and latency up to 35μs. The L0-only possibility appears as if this L1 hardware trigger with the initial (i.e., smallest) level of the trigger being known as L0 rather than L1. The key shift and check within the double L0–L1 selection is that the execution, for the primary time, of hardware-based track restoration within the L1 trigger methodology and mixing tracks with calorimeter- and muon-based L1 trigger substances. All sub-systems of ATLAS are skillful of embryonic to the dual-level hardware trigger construction as an extenuation approach in circumstance pile-up things at the HL-LHC what is more drive the readout competences of detectors to the reach of the bandwidth offered, or in an instance, the rates of hadronic trigger signatures with the fascinating brinks surpass the prevailing provisions. The L0 trigger technique is comprised of the L0 calorimeter trigger (L0Calo), the central trigger processor (CTP, and also the L0 muon trigger (L0Muon) sub-systems. within the phase one advancement, the current bunch and jet processors are substituted by the novel calorimeter feature abstraction trigger processors (FEX): eFEX for e/γ and τ, jFEX for single jets, and gFEX for larger-radius (or multi-jet) triggers, and also the calculation

of universal measures like Emiss T and HT. In phase 2 the FEX structures are supplemented by a modern forward FEX (fFEX) to recreate progress electrons (jets) within zone $2.5(3.2) < |\eta| < 4.9$, thus complementing the pseudo-rapidity exposure of the most recent tracker scheme. The brand new L0 {muon|negative muon|mu-meson|lepton} sub-system can utilize the improved RPC and TGC section logic and NSW trigger processors for the restoration of muon contenders. In supplement, the MDT data are used in recently committed processors to reinforce the toughness and effectiveness of the lepton trigger, its Pt resolution, and fussiness. the global Trigger can substitute and extend the Run 2 and phase one topological processor (L1Topo), by retrieving full-granularity calorimeter data to shine the trigger substances premeditated by L0Calo, execute offline-like algorithms, and compute event-level sizes beforehand applying topological assortments. the ultimate trigger finding of fact verdict by the CTP, which might utilize adaptably prescales and prohibits to the trigger elements. The CTP additionally pushes the trigger, timing, and control (TTC) logic system to start the readout methodology of the detectors.

The outcome of the L0 trigger assessment is communicated to every detector and trigger processor, upon which the following detector and trigger info, correspondingly, are communicated to the DAQ scheme over the alleged readout and dataflow sub-systems. each sub-system is made on service pc servers and traditional networking organizations. The readout sub-system incorporates the front-end link exchange (FELIX) module that employs the interfaces to the detector-specialized electronics through custom, point-to-point sequential links, e.g., the CERN Versatile Link+ and lpGBT protocol. FELIX also behaves as an interface to the rest of the DAQ method through changed input/output (PCIe with Xilinx FPGA) cards that remodel the detector front-end protocol info into customary packets for usage during a commodity multi-gigabit network. the improved event filter (EF) method offers high-level, software-based trigger practicality, and includes a CPU-centered process farm amid hardware-centered tracking co-processors for the trigger (HTT). The EF methodology enhances the trigger items to decrease the very best yield incident rate. The HTT includes each regional (rHTT) and global (gHTT) track restoration talents. The EF trigger verdict permits the transmission of information regarding chosen cases from the DAQ method to a stable area. The HTT reference

layout is established on associative memory (AM) ASICs for pattern identification and FPGAs for track rebuilding and matching. This choice is encouraged by the widespread knowledge of this technology within ATLAS (i.e., the continued incorporation of the prevailing quick tracker, FTK, into the HLT trigger) and also the ability to develop the HTT methodology for usage within the hardware primarily based on the L1 trigger. the quality selection could also be reevaluated in an issue of progression or a key scientific revolution of different technologies, like commodity CPU-centered servers, techniques established on accelerators (e.g., GPGPUs), or upcoming styles established on gadgets incorporating machine learning talents. The extremely profitable process program for the EF package is the commodity laptop server, which demonstrates a bent toward ways holding multi-core CPUs with an increasing core count. an extra applicable technology is the heterogeneous hardware styles, combining GPGPUs or FPGAs. Thus, the updated EF package ought to allow for each parallel algorithmic rule implementation at the event level (i.e., multiple events) further as manipulation of core correspondence (intra-event, i.e., concomitant handling of localities of interest, or intra-algorithm). The optimum level of correspondence is complete by harmonizing the possible benefits of knowledge and also the endeavor needed to regulate and preserve code. it's predicted to form interfaces that may allow for the operation of the EF as a rather heterogeneous theme, most likely as well as many teams of hardware, i.e., GPGPUs and commodity servers [106].

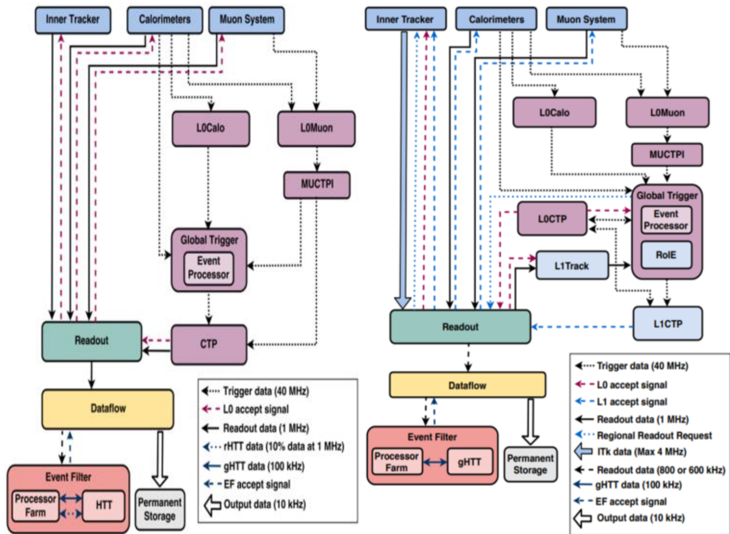


Fig 3.7: TDAQ Structure in Phase-II: standard (left) and progressed (right) circumstances [109].

Chapter 4

Design Evaluation of Small Pitch 3D Sensor

Arrays of doped columnar electrodes of both p and n types are placed in neighboring cells and are perpendicular to the wafer surface in 3D detectors, allowing them to detect in three dimensions. To create the columns, the high-resistivity silicon substrate is etched through [110]. Parallel to the wafer surface, electric field lines begin at one electrode type and finish at the nearest electrode of the opposing kind. Similar to typical planar detectors, the bias voltage controls the intensity of the electric field. A single-column or multi-column configuration may be used to create different types of detectors (e.g., pixel, strip, pad, and so on) using metal and/or polysilicon and/or diffusion surface connections.

In planar detectors, to make the depletion zone develop vertically, electrodes are implanted on both the top and bottom surfaces of the wafer as can be seen in fig. 4.1 (b). A 3D detector, on the other hand, allows for a decoupling of electrode distance L and substrate thickness (a). Because of this, the depletion zone may be made considerably smaller (10x) than the thickness of the substrate. Depletion voltage is substantially lowered in contrast to planar detectors as a result of this. There are several situations in which complete depletion of planar detectors is difficult due to junction breakdown and/or thermal runaway. To name only two, there are thick detectors utilized in the field of radiation detection and severely irradiated detectors used in high-energy particle detection (HEP). For example, at a given value of leakage current (that would increase with irradiation in the same way in planar and 3D sensors), the power savings from 3D sensors might be important to simplify the implementation of complicated systems. 3D architecture's charge collection characteristics are in some aspects superior to the planar one. A high-energy particle crosses the detector and creates a homogeneous pair density (e-h), as stated in Figures 4.1(a) and (b). The quantity of charge produced stays the same for the two types of detectors at the same substrate thickness. However, the distance of charge collection in 3D detectors is significantly shorter, and sufficiently high electric fields and carrier velocities can be obtained at bias low voltage. The charge collection

times can thus be significantly quicker (in the order of a few ns, to be compared to a few tens of ns for planar detectors).
Ramo's theorem, in particular, may be used to calculate the signal current from the carrier velocity and the weighting field. This is because each charge carrier is produced at a different distance away from the collecting electrodes, resulting in distinct peak signals. In 3D detectors, where all charges along the ionization track are formed within a significantly shorter distance from the electrodes, as can be seen in fig. 4.1 (a), this effect is well addressed.
There is no substantial difference between planar and 3D sensors in non-irradiated conditions. The 3D technology, on the other hand, is a cure for the charge trapping effects caused by high levels of radiation damage. As the last point, 3D detectors have significantly less charge sharing between neighboring electrodes than planar detectors with lower pixel sizes, which is a crucial need for photon imaging applications [111]. These gains come with a few drawbacks: the signal response to particles is not spatially homogeneous because dead regions occur (very low field) within the active volume. When charge carriers produced in these locations diffuse towards the region with a suitable electric field, the signal response is delayed, and it may contribute to poorer charge collection efficiency. Moreover, the capacitance in 3D detectors is significantly higher than in planar ones. This is due to the tiny spacing between electrodes and the fact that the electrodes extend to the bottom of the substrate. Because of this, the noise performance of these fast detectors degrades at short shaping periods, which is the main reason for their existence.

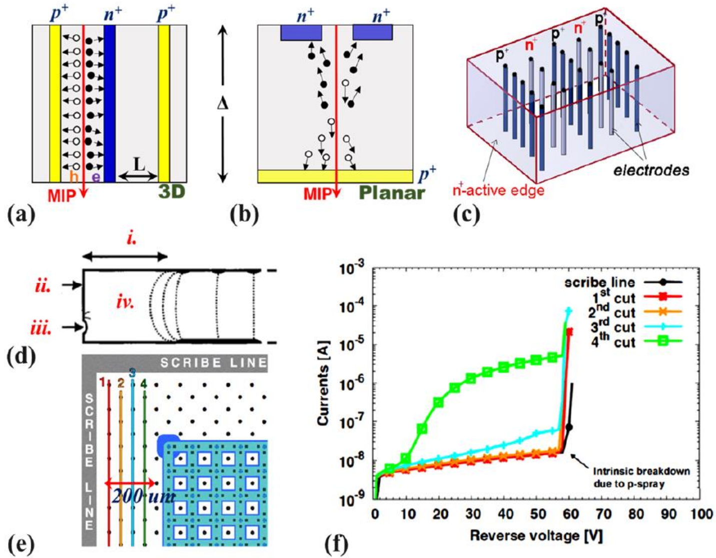


Fig. 4.1: Graphic cross-sections of a 3D detector **(a)** highlighting the decoupling of the active thickness (Δ) and collection distance (L) in 3D detectors and **(b)** of the planar detector. **(c)** Representation of 3D sensors with the active edge. **(d)** Graphic cross-sections of edge-region in a typical planar detector **i.** demonstrate the purpose for taking huge insensitive areas: **ii.** locations stand for adjusting guard ring, **iii.** defects generate from the saw-cut scheme and **iv.** the lump at the boundary of the electric field in the depletion zone, that should stay far away from the defect [112]. **(e)** Graphic of slim edge created on 3D Silicon sensors, and **(f)** investigation of I-V curves of double-sided 3D diodes with the slim edge of 200μm with the subsequent dicing done as described in (d) [113].

Diamond saws are used to remove the sensors from the wafer in conventional procedures. To prevent the electric field from reaching flaws (e.g., fractures, chipped areas) generated by the saw cut, planar detectors as can be seen in fig. 4.1 (d)) keep the active zone at a distance (~1mm) from the dicing line. It is common for planar sensors to include several guard rings at the perimeter to reduce the lateral voltage drop and improve the breakdown performance [114].

A huge quantity of current will be injected into the device if the depletion zone approaches these flaws, resulting in an early failure. A huge insensitive edge area is seen in fig. 4.1 (d). Defining an extra border condition around the sensor's active region can help limit the depletion expansion [112]. Fig. 4.1(c) shows a 3D model of it. The active region of the device is etched with a deep trench, which is then doped and passivated. A polysilicon-filled trench acts as an ohmic contact in this case. A support wafer is required for this method. The addition of supplementary difficulties to the fabrication procedure is factually not reasonable for the double-sided method, implemented in IBL construction.

A slim edge via columnar fence wall (as in fig. 4.1(e)) is another edge design for double-sided 3D Si sensors. It was employed in all of FBK's double-sided 3D processing batches since the method does not require a support wafer. An experimental saw cut to a thin edge (as in fig. 4.1(e)) and the sensor's I-V behavior (fig. 4.1(f)) confirm this. Compared to the IBL 3D sensor design, the slim edge can be further reduced in its size in case of a smaller pitch between the columns.

4.1 Simulation

Numerical simulations of 3D detectors, performed by TCAD software such as SILVACO or SYNOPSYS, can be used to forecast performance before construction. Simulated electrical and functional findings for 3D detectors were described in [110]. An example of a 3D detector with 25 µm spacing between columns and a typical unit cell is illustrated in fig. 4.2. (a). We have a variety of options when it comes to bulk doping concentration. The simulator domain can be decreased to a fourth of the unit cell only due to symmetry considerations. A slice of the complete 3D structure can be used to simulate the device's performance in 2D. (taken from the middle of the substrate).

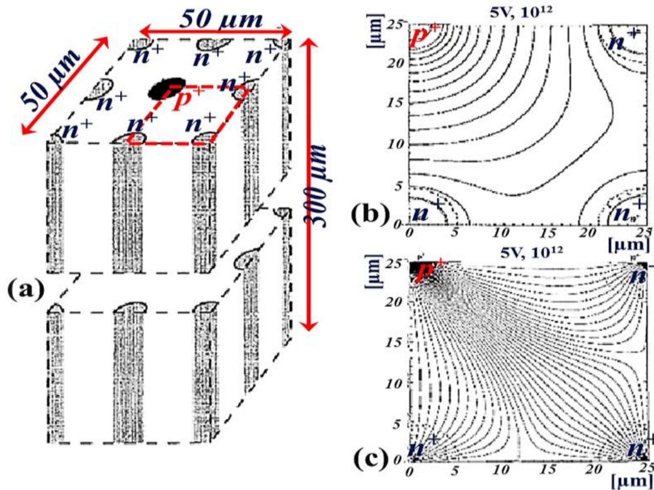


Fig. 4.2: (a) Simulated representation of a unit cell in a 3D detector, **(b)** equipotential outlines for 1/4 of the unit cell (red dotted marked in (a)) with 10^{12} cm^{-3} p-type substrate doping intensity at 5-V reverse bias voltage, **(c)** drift lines in the equal situation as in (b) [110].

A reverse bias ramp is applied to the other electrode type while doing simulations on electrical quantities. The complete depletion voltage for a p-type substrate detector with N_A=10^{12} cm^{-3} doping concentration is predicted to be just 1.6 V. (including the contribution from the built-in voltage). At N_A=10^{13} cm^{-3}, the full depletion voltage may be raised to 8.8 V. A quarter-cell with a N_A of 10^{12} cm^{-3} is shown in fig. 4.2(b) with a reverse bias of 5V as an example. Fig. 4.2 (c) illustrates the drift lines. The less-dense mesh schematic of the electric field along n+ columnar electrodes in fig. 4.2 (b) and (c) show the dead areas of the virtually zero-field region (2-3mm [110]). Un-even spatial response is predicted by this device when charged particles travel through it. However, the particle impact position is closely linked with the drift of charge carriers: electrons and holes produced by a single cell center may be collected in 1ns, but charges produced by n+ electrodes can take 5ns to collect [110]. Fig. 4.3 shows the time response of the signal to the input. When particles impinge on the detector surface perpendicularly, as shown in fig. 4.3 (a), the electrode current pulses are recorded, and the signal response behavior for particles

that hit between n+ electrodes is displayed in fig. 4.3 (b). 3D detectors produce signals considerably faster than planar ones, but with smaller peak fields, for particles hitting the null point.

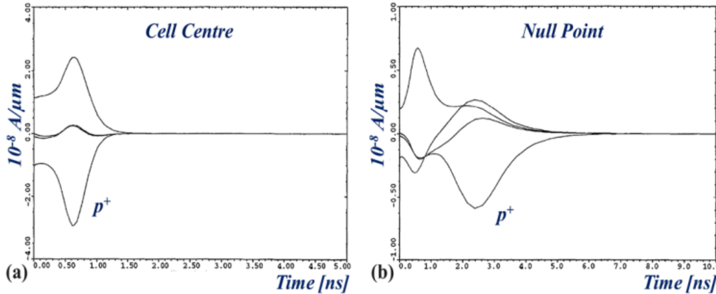


Fig. 4.3: Pulses of current on the electrodes in reaction to a MIP for a particular track parallel to the electrodes that drift **(a)** through the cell focus and **(b)** through the zero position in mid of two n+ electrodes (doping intensity 10^{12} cm^{-3}, reverse bias 10 V) [110].

For most applications, RC time constants linked to electrode resistance and capacitance are in the range of 100-200ps [4]. Close to the top and bottom surfaces, there is a deviation from the predicted behavior in both static and signal properties. Surface isolation structures such as p-spray or p-stops and the electron accumulation layer at the interface caused by oxide fixed charges vary from the forecast in these regions. Consequently, the charge collection characteristics are also impacted. To correctly anticipate these impacts, 3d simulations should be performed, which, of course, need a lot more computing power.

4.2 Historic Evolution of 3D Silicon Sensors

Since the fast development of MEMS technology in the 1990s, it has been feasible to produce 3D detectors. Columnar electrodes may still be made with a high aspect ratio of depth to diameter thanks to Deep Reactive Ion Etching (DRIE). Etching speeds can be as high as 3 μm/s, masking material selectivity can be as high as 70:1, and non-uniformities can be as low as 5%. In DRIE, the so-called "Bosch method" has become a de facto norm. Multiple cycles of 2-phase etching using

fluorine compounds are repeated to create a high anisotropy in the overall etching profiles [115]. Aspect ratios of 30:1 can be maintained in this technique today, but the value must be carefully optimized to the present constraints of 3D technology.

According to [116], the first few prototypes were produced at Stanford Nanofabrication Facility, SNF (Stanford, USA) using a long and complex processing cycle, which resulted in a relatively low yield due to the non-standard processing processes. Later, the Norwegian Foundation for Scientific and Industrial Research, SINTEF (Oslo, Norway), was tasked with determining if the SNF-recommended technique could be produced industrially.

As a result of the feasible modified 3D designs used by FBK (Italy), VTT (Finland), and CNM (Spain) in conjunction with major research groups, the manufacturing of 3D Si sensors was simpler and had a higher yield. "Single Type Column" (3D-STC) 3D sensors were the first simple 3D Si sensors created at FBK, with a single non-passing through columnar electrode (n+ doped) while the reverse side was uniformly doped with p+ material (fig. 4.4 (a)) [117]. When the columnar electrodes reached this stage, they were still hollow. There was another 3D-STC detector design (fig. 4.4 (b) [117]) that was also presented by FBK, but it was never realized. Only the electrodes were doped with p-type poly-Si [118]. For example, the p+ areas are patterned and implanted on the front side (fig. 4.4 (c)) rather than on the back side, according to Brookhaven National Laboratory, BNL (Upton, NY, USA), in collaboration with CNM [119].

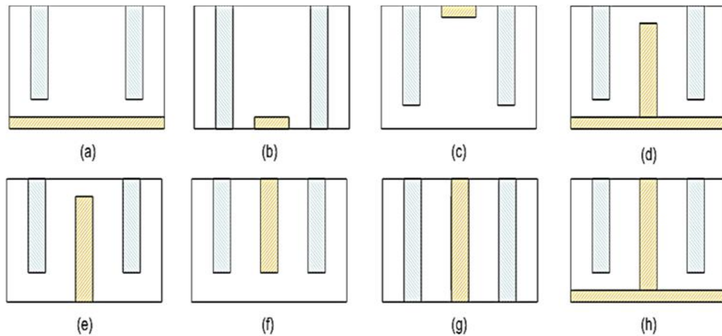


Fig. 4.4: Graphic cross sections unfolding the improved 3D detector constructions so far stated: **(a)** single-type column 3D detectors, likewise termed semi-3D detectors, with back-side ohmic contact, autonomously anticipated by FBK [117] (3D-STC) and VTT [118] (Semi-3D); **(b)** an substitute type of (a) with passing-through column, anticipated by FBK [117]; **(c)** single-type column 3D detectors with front-side ohmic contact, planned by BNL/CNM [119]; **(d)** and **(e)** double-sided, double-type column detectors with marginally diverse back-side formation, autonomously planned by FBK [121] and CNM [122], correspondingly; **(f)** single-sided, double-type column detector planned by BNL [123]; **(g)** and **(h)** alternative forms of double-sided, doubletype column detectors planned by FBK containing passing-through columns [125, 126].

Single type column only 3D Si sensors among all these versions come with a major simplification in the fabrication technology with respect to the standard process followed for full 3D detectors. Such architectures have to deal with the slower response times and limited charge collection efficiency and radiation resistance [120]. The revolutionary Double-type-column 3D detectors (3D-DDTC) were then independently proposed by FBK [121] and CNM [122] as it could be seen in fig. 4.4 (d) & (e). The fabricated solution of this 3D-DDTC came up with better performance compared to single columnar type solutions owing to fully shielding property. In both approaches followed by FBK and CNM, columnar electrodes are etched from both wafer sides. In particular, in the CNM approach (fig. 4.4 (e)), both types of electrodes stop a short distance from the opposite surface. This solution still provides several advantages from the viewpoint of process complexity, owing in particular to the absence of a support wafer. FBK detectors (fig. 4.4 (d)) slightly differ from CNM ones in the fact that they feature a uniform doping layer on the wafer back-side between

the ohmic columns in order to feature a singular ohmic contact region. These columns remained hollow rather than being partially filled with poly-Si. Also for double-type column detectors, BNL proposed a one-sided alternative [123] (fig. 4.4 (f)), for which, however, no results are available

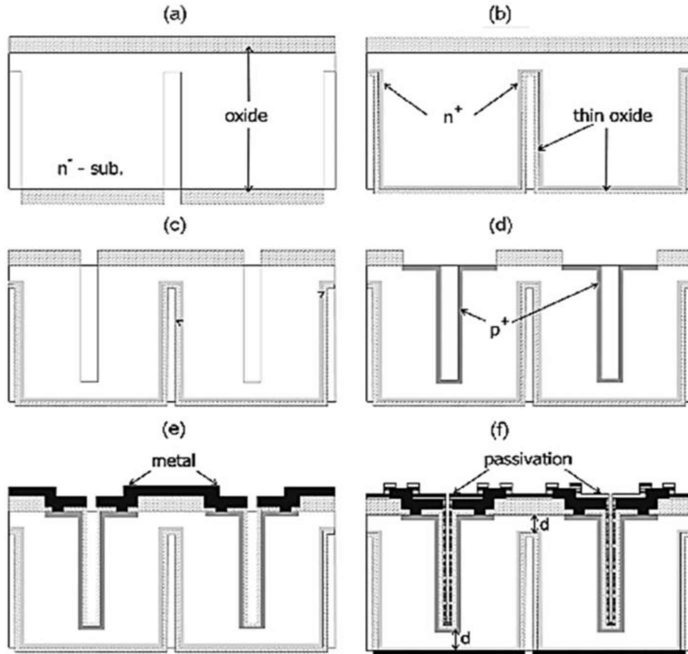


Fig 4.5: Diagram of the key stages of the fabrication of 3D-DDTC detectors on n-type substrates at FBK [121].

The main process steps for the fabrication of 3D-DDTC detectors on the n-type substrate at FBK are presented in fig. 4.5 [121].

a. On the backside, a thick oxide is formed to be utilized as a mask for the first DRIE step.
b. After patterning and removing the thick oxide, Phosphorus is diffused from a solid source into the columns and on top of them. Afterward, a thin oxide layer is formed to prevent the dopant from diffusing out of the semiconductor device.
c. To define readout electrodes, the oxide layer on the front side is patterned and a DRIE process is conducted on the top surface.

d. Around the columns, the thick oxide layer is removed, and boron is diffused into the columns and on the surface to facilitate the creation of contacts between the columns and the metal.
e. Also on the front side, a thin oxide layer is grown to prevent the dopant from escaping. In addition, contact holes are defined and etched through the oxide, while aluminum is sputtered and patterned.
f. Another layer of passivation is deposited and patterned to define the metal layer access, while aluminum is sputtered to provide a metal electrode on the backside.

Similar techniques are used to fabricate 3D-DDTC detectors manufactured on the p-type substrate, however, there is an inversion of column doping types and a new process step to create n-column surface isolation using p-spray surface isolation. An additional mask is required when using P-stop or P-stop/P-Spray as part of a multi-step patterning process. Others, such as fig. 4.4 (g), which includes full-through columns of both doping types and is produced by employing a relatively thin stack of passivation layers as an etch stop for DRIE [124], has been developed at the FBK. Another variant developed at FBK is illustrated in fig. 4.4 (h), where ohmic columns are passing-through, through, and doped by diffusion along with the entire wafer backside, whereas the readout columns stop at a safe distance from the backside to avoid early breakdown.

4.3 Experimental Results

4.3.1 Full 3D Detectors from Stanford

Using a p-type 121 m active-thickness 3D detector, the initial electrical measurements showed leakage current densities of about 1nA/mm^3, breakdown voltages of around 60V, and full depletion voltages of 8V up to 200 mm electrode pitch design [116]. There is a little difference between the actual values of capacitance (0.1 pF/column) and the calculated projections [96]. X-ray and particle charge collection properties are described for the first time in [127]. In this work, the readout shaping time of 1ns ensured minimal charge sharing between neighboring cells. Using coincidence scintillators and rapid electronics for a ^{106}Ru source, an effective -scan response was produced. Irradiation with 24 GeV/c protons for 5×10^{14} cm^{-2} cumulative fluence, and with 55 MeV protons up to 10^{15} cm^{-2} fluence was checked. The leakage current damage constant was 4 to 5×10^{-17} A/cm, and the

depletion voltage increased to 105V for the highest fluence [128]. Using infrared microbeam experiments, researchers at the University of New Mexico found that after irradiating with 55 MeV proton, devices had active volume extensions of up to 5 µm[129,130]. These findings were in line with those of another study [131] that used planar-type sensors that had been exposed to 12.5 keV X-rays. For 10^{15} cm^{-2} proton irradiated sensors, charge collection efficiency was estimated to be up to 60% [132]. It was also shown that particles traveling through columnar dead areas may still be detected using a 12.65 keV X-ray synchrotron beam, although at a much smaller scale since the induced charges have to diffuse first to the active region of a sufficiently high electric field [133,134].

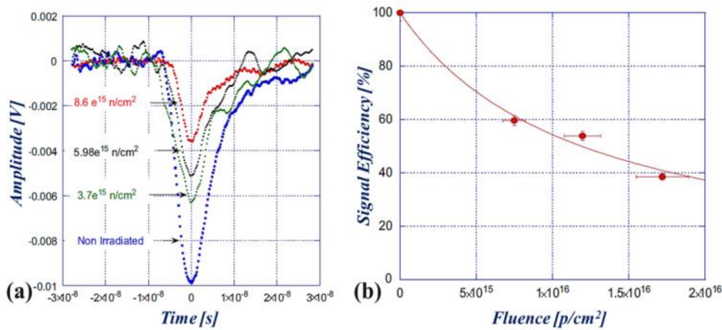


Fig 4.6: **(a)** Oscilloscope traces of 1000 averaged samples of 3D detector signals responding to rapid IR pulsations at 1,060-nm wavelength. Information pertinent to several irradiation fluences is evaluated, **(b)** Signal efficiency of 3D detectors irradiated with neutrons vs. the fluence, which was transformed to proton equivalent utilizing the Non-Ionizing Energy Loss (NIEL) scaling to 24 GeV/c cm^{-2} [135].

A 3D detector with a 71 mm inter-electrode pitch responds to IR laser pulses up to 8.6×10^{15} cm^{-2} neutron irradiation fluences in fig. 4.6 (a) [134]. The corresponding Signal Efficiency (SE) as a function of the fluence normalized to 24 GeV/c protons is shown in fig 4.6 (b). SE tends to be approximately 38 percent for the High-Luminosity LHC's requirements. To circumvent this restriction, 3D detectors can be designed with a smaller electrode pitch [135]. An investigation of the noise produced by 3D pixel detectors with varied electrode arrangements (bump-bonded to the

ATLAS FEI3) is presented in the same publication, showing the influence of the capacitance reliance upon the number of electrodes.

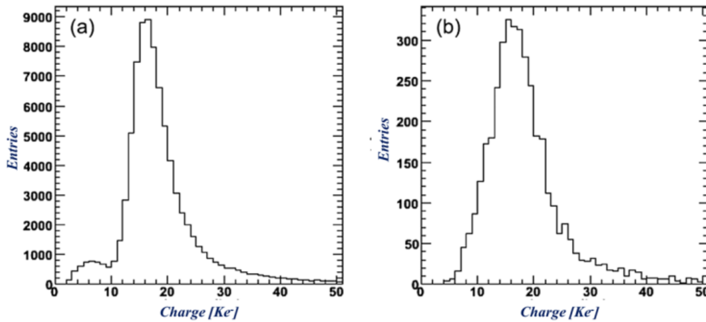


Fig 4.7: Quantified distributions of cluster charge for 100-GeV pion tracks beneath distinct incline angles: **(a)** 0° angle of incidence (i.e., rectangular to the detector surface) and **(b)** 15° angle [136].

Three-dimensional pixelated sensors (FE-I3) were tested at CERN's Super Proton Synchrotron (SPS) with 100 GeV pions, and their hit efficiency was 95.9% ± 0.1% for orthogonal incidence and 99.9% ± 0.1% for 15° tilt [136]. As an example, Fig. 4.7 compares the recorded Landau distributions of the cluster charge for tracks orthogonal to the detector surface (fig. 4.7(a)) and tracks impinging at an angle of 15° (fig. 4.7(b)). As a result of non-uniform spatial efficiency, low charge inputs influence the 0° plot. For a 5V bias reference, another test-beam experiment with 24 GeV/c protons reported a signal efficiency of up to 21% [137].

4.3.2 3D-STC or Semi 3D Detector at FBK and VTT

Depletion happens in two stages for Semi-3D sensors depicted in fig. 4.4 (a): lateral depletion in between columnar electrodes, followed by an upward vertical depletion from columns' tips to the backside [137]. Once lateral depletion is attained, the electric field at the exact mid-point of columnar electrodes cannot be increased anymore, and it is solely dependent on the substrate doping concentration. If the MIP hits a semi-3D structure at the exact midpoint of columnar electrodes, the signal

response is approximately 100 times lower than if it hits a semi-3D structure near the columnar electrode [117].

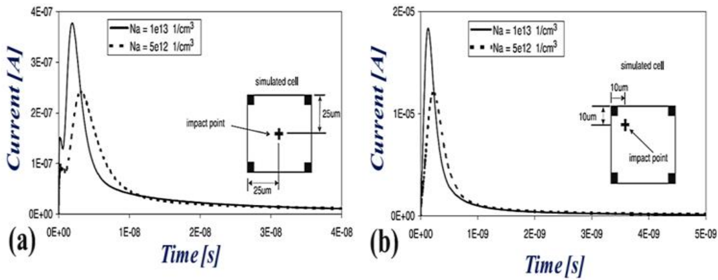


Fig 4.8: Simulation of the current signals induced by a MIP particle impinging a 3D-STC detector in two different positions (see insets) [117].

Due to electrons and holes migrating horizontally towards the closest electrode and the center of the structure, a rapid signal component of a few ns is present. As can be seen from the different peak locations in the two examples, the collecting time of electrons is highly dependent on the impact position (fig. 4.8). When the holes slowly diffuse towards the rear plane, they produce a long tail that lasts for many microseconds. In this case, the impact position has no bearing on the signal. However, holes do not begin drifting until they reach an area below column tips with a high vertical electric field. Ballistic deficit effects can emerge as a result of this slow signal component when fast electronics are utilized for the readout [117, 138].

Three-dimensional STC detectors have been extensively studied since their construction [137-142]. As shown in fig. 4.9, the measured signal response was quick and lengthy, regardless of particle impact, as predicted by simulations, using the Transient Current Technique (TCT), which was done at JSI using a 1060 nm pulsed laser system. As with planar strip detectors, Ramo's theorem may be used to explain this phenomenon. It's possible to enhance spatial resolution in 3D-STC detectors due to non-negligible generated signals. It's important to note that in this

case the fast signal component would be muted since a positive and a negative fast signal would be created on two columns of the same strip (fig. 4.9).

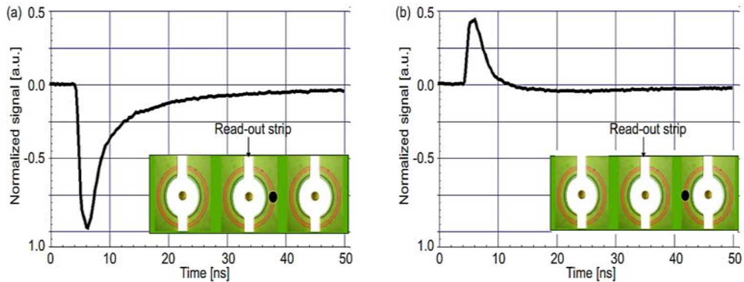


Fig 4.9: Transient Current Technique signal stimulated on the central strip by a 1060-nm pulsed laser (black spot) in the situation of **(a)** a beam concentrated close to the readout strip and **(b)** a beam concentrated near the neighboring strip [138].

After neutron irradiation up to 5×10^{15} cm^{-2} fluence, the TCT approach was used to extract the signals from the sensors. The signal efficiency was found to be about 10% for particles that struck the same center. It was confirmed that 3D-STC detectors did not respond uniformly to high irradiation levels, which meant that the charge collection efficiency could never be measured.

Sensors with similar leakage current density and capacitance reported by VTT at 100 V (far beyond full depletion) were reported to have leakage current densities of a few pA per column. Samples irradiated with CERN PS proton at a dose of 6×10^{15} cm^{-2} had a depletion voltage of less than 100V [144]. As a result, several sensors bonded to the Medipix2 read-out chip showed good imaging characteristics for 35 KeV X-rays [145].

4.3.3 3D Double-sided Double-type Column Detector at FBK and CNM

FBK and CNM both independently suggested 3D Double-sided Double-type Column (3D-DDTC) detectors, but in somewhat different forms (fig. 4.4). While lowering the overall process complexity, this detector design promises to deliver performance comparable to full 3D detectors. TCAD simulations produced a 3D-DDTC detector

for a quarter-volume cell of 40×40×250 μm^3 between readout columns on a p-type substrate with an 80 µm pitch (fig. 4.10 (a)). Oxide charge and p-spray isolation are also given, with values typical of FBK technology, as are 2×10^{12} cm^{-3} substrate doping concentrations.

Different shapes were examined to see how the distance d impacts performance. P-spray isolation was implemented on the rear surface for the whole passing through design (d=0). Fig. 4.10 (b) depicts the electric field arrangement along the diagonal of the simulated cell in fig. 4.10 (a) when the voltage is 16 volts (beyond full depletion).

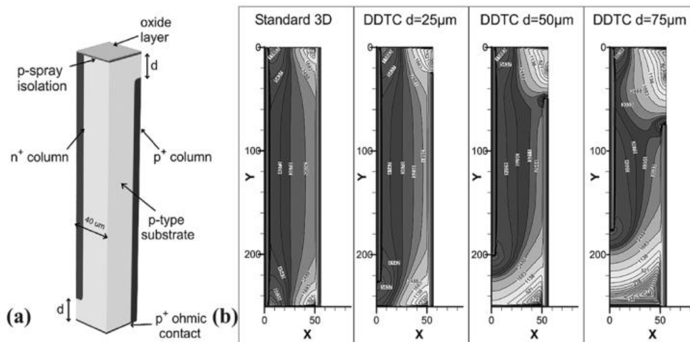


Fig 4.10: (a) Outline of a 3D Double-side Double-type Column detector of 80 µm pitch on a p-type substrate. The single-cell signifies one-fourth of the standard model appears in the design. (b) Simulated Electric field distribution of a two-dimensional cross-section captured around the diagonal of the quarter cell. The column junction is placed at x=0 and the ohmic column is at x=40. The four plots (from left to right) are mentioned to a full 3D and three 3D-DDTC with d=25 µm, d=50 µm, and d=75 µm [124].

As can be observed, the electric field lines in complete 3D are horizontal and extremely uniform across columns, save from regions near the surfaces, because of the impact of p-spray. At larger gaps (d), the electric field gets distorted and only a tiny portion of the field lines is comparable to those of full 3D. Low field areas at the top and bottom surfaces of 3D-DDTC detectors lead to a reduction in the effectiveness of charge collection. Raising bias voltage over the depletion value increases the electric field between columns and carrier drift velocity, resulting in much shorter collection times as compared to 3D-STC.

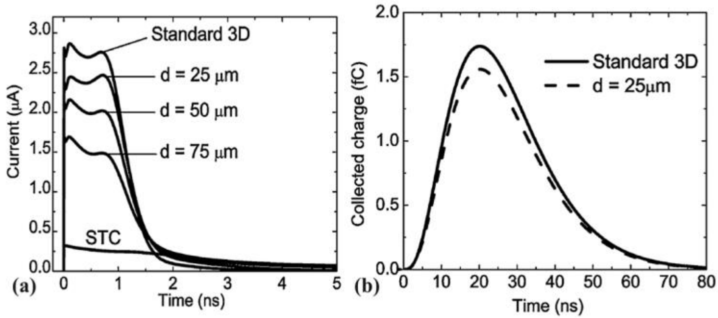


Fig 4.11: (a) Simulated Transient current signals in 3D detectors of diverse geometries at a bias of 16V in retort to a MIP particle, (b) Replicated transient signals in 3-D detectors of diverse geometries irradiated at 10^{16} cm^{-2} 1-MeV n_{eq} fluence, at the yield of a semi-Gaussian CR-$(RC)^3$ filter with a shaping time of 20ns [124].

Fig. 4.11 illustrates the induced currents of transient simulation, where a MIP particle impinges on the cell at a few microns from the ohmic p+-column, for varied depths of junction columns at 16V. Static electric field models predicted that the shorter the distance d, the greater the peak current, and the shorter the collection time were the results found to be (see, the tails). Full 3D and 3D-DDTC with d=25 µm produce equivalent charge collection efficiency when accounting for bulk radiation damage (10^{16} cm^{-2} 1-MeV n_{eq} fluence) (fig. 4.11 (b)) [124].

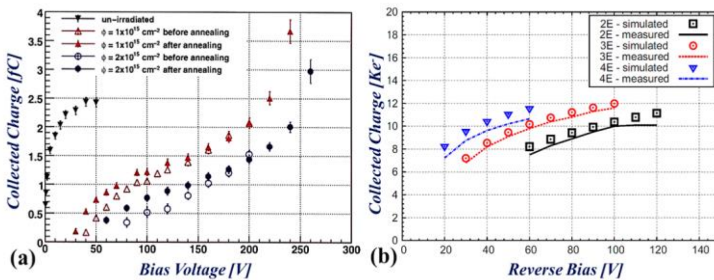


Fig. 4.12: (a) Graphical representation of charge collection of two 3D-DDTC detectors irradiated with 25 MeV protons at $1{\times}10^{15}$ cm^{-2} and $2{\times}10^{15}$ cm^{-2} fluences. The picture contains information calculated before and after an annealing step at 60º for 80 min targeted at getting benefit from the short-term annealing [149]. (b) The analogy between calculated and simulated

accumulated charge as a function of reverse bias voltage for pixel sensors with distinct electrode configurations (2E, 3E, 4E) irradiated with 25 MeV protons at 1×10^{15} n_{eq} cm^{-2} [157].

Another intriguing finding of leakage current, depletion voltage, collected charge, capacitance, and associated noise in different electrode configurations of these 3D detectors in comparison to the present ATLAS pixel architecture was published in [146]. FBK's 3D-DDTC detectors, which were built on 300 μm thick n-type substrates, showed encouraging results, although the structures had not been optimized in terms of column overlap. 0.1pA/column at complete depletion was reported as the leakage current, which is excellent [124]. To perform functional characterization, the ATLAS SCT ABCD3T readout module (20 ns shaping time) used a ^{90}Sr beta source system in conjunction with 3D-DDTC strip detectors attached to it. Although the device capacitance was greater in that generation, the charge collection efficiency was better concerning 3D-STC for the sensors under evaluation, which had a 1cm^2 area with 102 strips and 102 columns per strip [147]. The tracking efficiency, charge sharing, and location resolution were all excellent in a beam test [148-150].

Three distinct fluences up to 2×10^{15} cm^{-2} irradiated 25 MeV protons on 3D-DDTC detectors. After irradiation, the samples were annealed for 80 minutes at 60°C to take advantage of beneficial annealing and achieve the lowest possible depletion voltage. A plot of the collected charge at two higher fluences, 1×10^{15} cm^{-2}, and 2×10^{15} cm^{-2}, is shown in fig. 4.12 (a). To be clear, the annealing step lowered the effective doping concentration since the lateral depletion of both detectors happened at lower voltages following the annealing. Higher trappings produced at higher fluences considerably lower the collected charge compared to the pre-irradiation value. Up to 1.5 fC may be collected from sensors exposed to 1×10^{15} cm^{-2} and 2×10^{15} cm^{-2} irradiation when the bias voltage is 150 V. All 3D-DDTC detectors show an exponential rise in the collected charge above this voltage. As anticipated by TCAD simulations [151], this behavior may be ascribed to avalanche multiplication induced by particles and aided by strong electric field effects at the column tips. The other 3D-DDTC batches were fabricated at FBK on 200-220 μm thick p-type

substrates, resulting in a greater column overlap (100 to 150 µm), which improved the performance [152-155]. The sensor's behavior before irradiation was further examined in a high-energy pion beam test at CERN, with and without a 1.6T magnetic field [156].

The 3D-DDTC sensor's performance was found to be equivalent to that of full 3D sensors, with no noticeable influence from the magnetic field and very little charge sharing across cells. After irradiation, the performance of the initial FBK 3D-DDTC pixel sensors was restricted by the non-optimized column depth, which led to low field areas and charges trapping effects. The collected charge of sensors with various electrode configurations bombarded with 25 MeV protons at 1×10^{15} n_{eq} cm^{-2} and evaluated with a ^{90}Sr beta source is shown in fig. 4.12 (b) [159]. The charge reaches saturation at various reverse bias voltages as predicted, depending on the inter-electrode spacing used in the characterization of the various configurations. When compared to TCAD simulations (also shown in fig. 4.12 (b)), the charge collected is quite close, even if the signal efficiency is still limited to 70%. Several beam experiments performed on these sensors and others irradiated with neutrons up to 1×10^{15} $n_{eq}.cm^{-2}$ yielded promising results in terms of hit efficiency, charge collecting, and charge sharing [158].

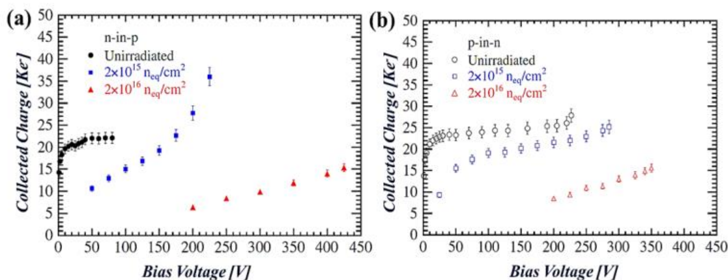


Fig 4.13: Graphical representation of signal as a function of the reverse voltage for several irradiation fluences computed with **(a)** n-in-p sensors and **(b)** p-in-n sensors. Computations were accomplished at temperatures of T= -16°C (before irradiation), T= -40°C (2×10^{15} $n_{eq}.cm^{-2}$) and T= -43°C (2×10^{16} $n_{eq}.cm^{-2}$) [163].

Double-sided CNM 3D detectors with electrodes 250 µm deep on 300 µm thick n-type Si wafers have been reported as the first results for 3D detectors by CNM. There are modest depletion voltages (a few Volts) in the initial electrical tests as well as good leakage currents (1pA/column) and breakdown voltages of more than 60V [159,160]. [161] describes the functional features of pixels detectors bump-bonded to Medipix2 readout. X-ray surveys revealed a low depletion voltage of ~2V for lateral depletion and ~9V for complete depletion. The charge-sharing mechanism in planar detectors, on the other hand, is significantly decreased in a spectroscopic test employing monochromatic 15-keV synchrotron X-ray photons. The CNM 3D-DDTC sensors performed exceptionally well despite being irradiated up to extremely high fluences because of an optimized column overlap. After irradiation up to 2×10^{16} n_{eq} cm^{-2}, sensors in the strip arrangement were fully tested with an Alibava read-out system [162,163]. It was discovered that sensors with an electrode distance of 56 µm between the negative pole and the positive pole were superior to those with an electrode distance of less than that. Fig. 4.13 shows the charge accumulated under various irradiation settings as a function of reverse voltage. As can be observed, sensors reach their maximum efficiency around 2×10^{15} $n_{eq}.cm^{-2}$. Furthermore, the signal efficiency reaches 100% for accumulating 2×10^{15} $n_{eq}.cm^{-2}$ fluence owing to a charge multiplication effect at high voltage and may still achieve 70% at 350 V after 2×10^{16} $n_{eq}.cm^{-2}$ [163]. The highest signal observed was restricted to 15 Ke^{-} only by higher induced trappings in the p-substrate from the 2×10^{16} $n_{eq}.cm^{-2}$ campaign.

4.3.4 3D-DDTC for Insertable B-Layer, A State of the Art Production

The ATLAS 3D Sensor Collaboration has worked tirelessly for more than a decade to create 3D sensors, and this manufacturing maturity has been attained in the last several years. Since 2009, the major focus has been on the ATLAS pixel Insertable B-Layer (IBL), a new pixel layer that was placed as near as 3.4 cm from the proton beams inside the existing ATLAS pixel layers to increase physics performance [165]. A two-year halt for IBL installation was implemented in 2011, during which time sensor technology was examined using built-in module prototypes with planar and 3D sensors. Before and after irradiation, the measured performance of the 3D

module prototypes was convincing, thus they were included in IBL. With a mixed-sensor IBL architecture with planar sensors in the center and 3D in the forward/backward section, the goal was to take advantage of a more consistent charge collection across the sensor depth when tracking an object.

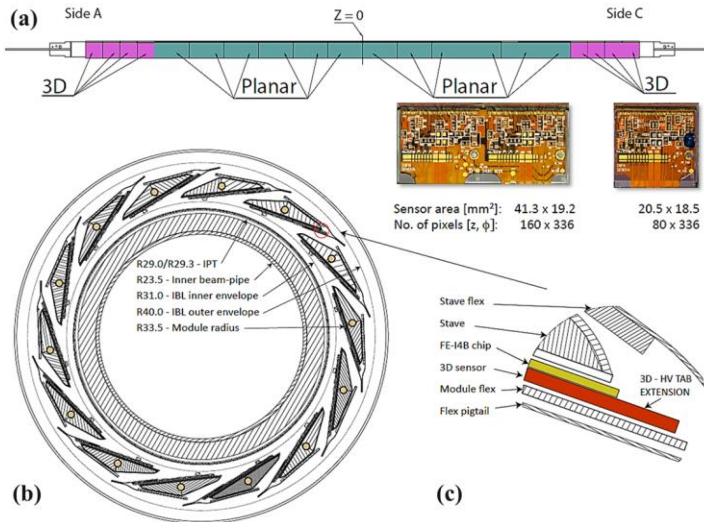


Fig 4.14: (a) Planar and 3D sensor modules organization with Stave layout. (b) The arrangement of the IBL detector with the 14 staves over the IBL positioning tube (IPT) and (c) magnification of one stave side where a 3D sensor module is visible [91].

Fig. 4.14 depicts the IBL system layout. For each stave, there are 12 modules with double-chip planar sensors in the middle and 4 forward single-chip 3D sensors at the two ends. Each stave has 14 blades. The four 3D silicon processing facilities of the ATLAS 3D Sensor Collaboration (SNF, SINTEF, CNM, and FBK) have decided to combine their efforts to manufacture the needed amount of 3D sensors for ATLAS IBL. While retaining the distinct flavors of the various technologies, a common design and collaborative processing effort established during this cooperation provided many advantages: full mechanical compatibility and equal functional performance of the 3D sensors [166]. At FBK, improved 3D-DDTC processing for passing-through

columns was developed [32]. One-quarter of the front ATLAS IBL staves (112 modules) are dedicated to the manufacture of 3D pixel sensors [170].

A 130 nm CMOS readout was used for all sensor designs to meet the FEI4 pixel requirement. It has a resolution of 80 × 336 pixels and a pitch of 50 × 250 μm^2. Because of the processing in this 3D technology, the huge sensor size was a key problem for the manufacturing yield, and so the single sensor tiles were attached in pairs in the modules. The active sensor thickness is 230 μm, which is a reasonable compromise between signal/noise and mechanical robustness for double-side processing [167].

In comparison to CNM and FBK sensors, which used a slim edge design, SNF/SINTEF sensors used an active edge design [169]. While CNM used 3D electrodes for its guard ring, FBK's concept has an ohmic column fence that surrounds the active area. All foundries opted for a narrow edge design in consideration of the IBL specification, which calls for a dead zone of 200 μm between sensors in the direction parallel to the beam (Z).

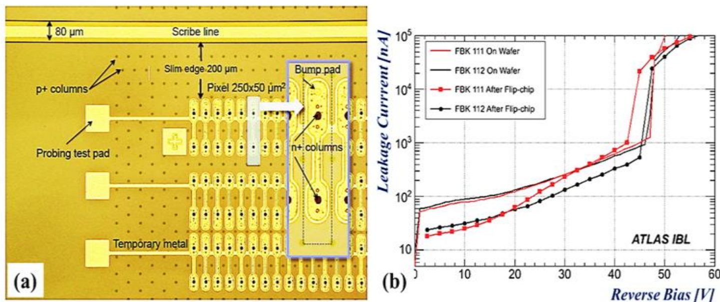


Fig 4.15: (a) Selection process of the working pixel row at wafer-level investigation with temporary metal at FBK and (b) comparison of total current versus voltage curves from an FBK sensor measured on-wafer with temporary and after bump bonding [169].

Bump bonding of the sensor to the readout has always been a difficult and expensive operation, thus originally detecting defective pixel sensors was necessary.

Both SNF/SINTEF and FBK employed a thin aluminum sheet to temporarily short a pixel array while conducting current-voltage measurements in each tile. As a result, the overall current may be calculated. Fig. 4.15 compares, as an example, the I-V curves measured on a wafer with a temporary metal to the assembly after bump bonding and flip-chip. There's a good agreement about the quality. After the front-end installation, the leakage current remained lower as predicted due to the increasing contribution of the temporary metal to the surface current (MOS effect) [171].

The temporary metal pattern of the CNM sensors was not entirely compatible with the test equipment provided. These sensors were only qualified by a guard ring current test. However, in this situation the approach used was not precise, because it is impossible to determine the real current drawn by the sensor [170]. The certification phase of these sensors was restricted to the installation program, which was established in 2013-2014 for the first long shutdown of the LHC. Thus, the certification of SNF/SINTEF sensors could not be completely exploited, and towards the conclusion of the production, the IBL 3D ATLAS Collaboration chose FBK and CNM. The sensors had an electrical characterization of V_{depl} less than 15V, V_{bd} more than 25 V with a complete sensor leakage of 2 μA [166], and V_{depl} with less than 15 V with a decommissioning V_{bd} voltage. At about 20 V at -15°C, operating power was determined. With the bump bond costs in mind, processed wafers with a functional pixel sensor of at least three were delivered solely for final bump bonding. Several FBK and CNM sensor assemblies, including the FEI4 read-out chip, were tested both before and after irradiation in the laboratory and test beams, reporting a maximum leakage current of 100 nA/pixel, maximum dissipation of power of 200 $mW.cm^{-2}$, and in-time hits of >97 percents at a 15° track inclination angle of -15°C after a 5×10^{15} $n_{eq}.cm^{-2}$ benchmark [170].

Many assemblies were irradiated during IBL ratings with 25 MeV protons at KIT, Germany, and with neutrons up to 6×10^{15} $n_{eq}.cm^{-2}$ in Ljubljana, Slovenia. The TID of the proton-campaign sensors was retrieved at ~750 Mrad(Si), far greater than the IBL requirement (250 Mrad). Before testing, all assemblies had been annealed at 60°C for 120 minutes. Beam testing was also performed with CERN SPS 120 GeV pions and DESY 4 GeV positrons. In separate stray tests, irradiated and non-

irradiated assemblies, a planar sensor was maintained as a reference. Data were taken for both the beam incident perpendicular to the module and a ϵ rotation of ±15° [170].

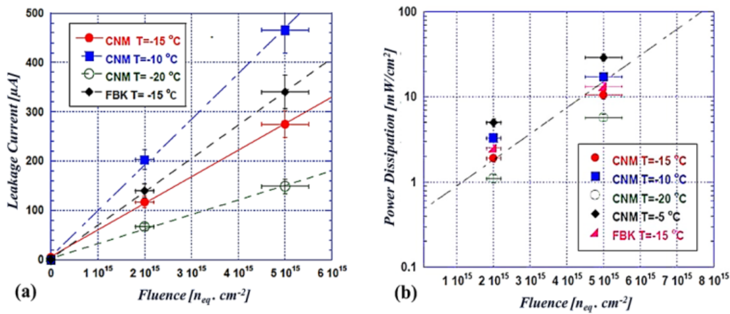


Fig 4.16: Data at various temperatures from CNM and FBK of fluence vs (a) Leakage current and (b) power dissipation of pixel sensor assemblies irradiated with 25 MeV protons -15°C [172].

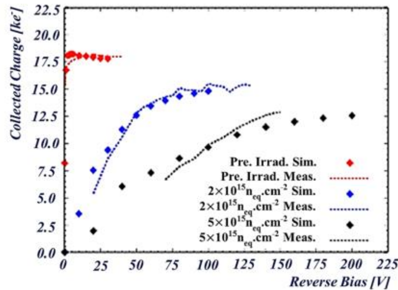


Fig 4.17: Comparison between measured and simulated collected charge as a function of reverse bias voltage for IBL pixel sensors from FBK before irradiation and after 25 MeV proton irradiation at 2×10^{15} $n_{eq}.cm^{-2}$ and 5×10^{15} $n_{eq}.cm^{-2}$ [173].

Fig. 4.16 shows the flow-based leakage current and dissipation of power, which is measured for proton-irradiated CNM and FBK sensor modules at various temperatures [172]. The power dissipation (~15 $mW.cm^{-2}$) and the leakage current (~10 nA/pixel) were 10 times less than the criteria for IBL certification to 5×10^{15} n_{eq} cm^{-2} fluence. Though 3D sensor modules have a higher pixel capacitance of 200 fF, a larger noise level is seen in planar sensor systems (from 150 to 200 e^{-}), regardless

of the irradiation conditions of test beam and laboratory measurements[169] has been recorded. Various IBL FBK sensors have been subjected to a beta source of ^{90}Sr and the corrective charges collected are shown in fig. 4.17 as a function of the bias voltage. The accumulated charges that reach the whole saturation plateau at less than 10 V are seen (fully depleted). After irradiation (5×10^{15} cm^{-2}), it was possible to still collect 60% of the charge, as could be shown in the same figure, in good accordance with the TCAD predictions [173]. Simulations incorporating radiation damage to the specified fluence, inter-electrode spacing, and effective drift lengths [174,175], were carried out with the "Perugia" trap model. Data simulated in the same figure are secondary to the validity and, compared with the results of experiments, account for every conceivable uncertainty: calibration errors, beam homogeneity, and annealing conditions [169-173].

Table 4.1: The key outcomes of the 2011 CERN beam experiments were summarised. In April 2012, the result of a DESY Beam Test for the FBK87 sensor was derived. With a setting of 10 ToT at 20 ke-signal, all results were reached.

Sensor ID	Bias (V)	Tilt Angle (^{0})	Irradiation	Fluence ($n_{eq}cm^{-2}$)	Threshold (e^-)	Hit Efficiency (%)
CNM55	20	0	No	-	1600	99.6
FBK13	20	0	No	-	1500	98.8
CNM34	140	0	25 MeV Protons	5×10^{15}	1500	97.6
CNM34	160	0	25 MeV Protons	5×10^{15}	1500	98.1
CNM97	140	15	25 MeV Protons	5×10^{15}	1800	96.6
CNM34	160	15	25 MeV Protons	5×10^{15}	1500	99.0
CNM81	160	0	Reactor Nutrons	5×10^{15}	1500	97.5
FBK90	60	15	25 MeV	2×10^{15}	3200	99.2

			Protons			
FBK11	140	15	25 MeV Protons	5×10^{15}	2000	95.6
FBK87	160	15	25 MeV Protons	5×10^{15}	1500	98.2

The most relevant findings of the beam testing at CERN in 2011 were reported in table 4.1 in several installation arrangements during the qualifying stage of the module. Non-irradiated samples have been detected on perpendicular tracks, where high efficiency was already achieved at low voltage because of a short inter-electrode distance from the planar sensor. It should nevertheless be noted that FBK 3D sensors do not operate properly when particles hit perpendicularly to the systems since the whole column passage is a dead area. CNM is capable of collecting charges from areas between the tips of the column, thereby performing better than FBK. After irradiation and compatibly with IBL standard, hit efficiency remains excellent. Inclined ±(10-25) degrees enhance the efficiency of the hits. As seen in table 4.1, improved efficiency is obtained by increasing the bias voltage from 140 V to 160 V and reducing the threshold to 1500 e^-.

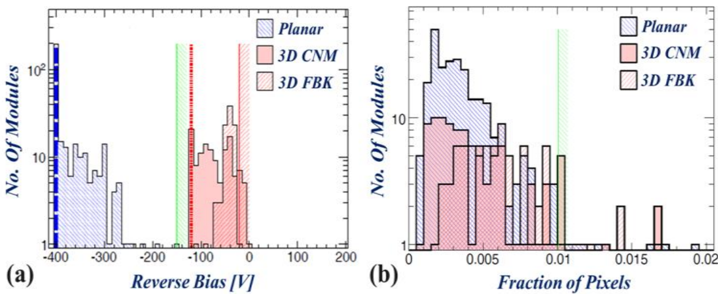


Fig. 4.18: a) Distribution, during the qualifying phase, of the modules breakdown voltage for various types of IBL sensors detected by the FE chip. The vertical blue dashed line specifies the maximum measuring bias set for the flat sensor (-400 V), and the red marked line specifies the maximum measuring bias set for the FBK and CNM 3D sensors. Installed in the flat sensor (V_{bd} more than 120V) the acceptation margin was indicated as a green combo line, whereas (30V) was for red Combo line denoted 3D sensors[165]. (b) The distribution of the fraction of pixels failing in any test of breakdown or ^{241}Am source scan.

The sensor breakdown voltage was selected as a qualification factor during the qualification process. The distribution of the breakdown voltage and the specified thresholds for all the constructed modules is reported in fig. 4.18 (a), ultimately qualifying it for IBL installation. Measurements were conducted to maintain current compliance with FE-I4 readings at 10 µA. Because the IBL 3D sensor working power set was 20V, all bump-bonded modules with a breakdown voltage of less than 30V were dismissed. However, because the CNM sensor qualification was not precise enough without a temporary metal test, the dispersion of the approved CNM 3D sensor module was quite low as seen in fig. 4.18 (a). Alongside this CNM sensor, the leakage caused by increased surface current made the procedure of determining the failure voltage more difficult [165]. A larger CNM sensor distribution in comparison with FBK may thus be noticed in fig. 4.18(a). This impact can be reduced by the accumulated TIDs and bulk damage during the lengthy LHC cycle. A functional test utilizing the ^{241}Am source validated the bump bonding output on the sensor module. A pixel was deemed to be missing when it had an average pixel occupancy of less than 5% or more than 450%. In fig 4.18(b), the failed test statistical information is reported according to the sensor kinds. The V_{bd} test and functional testing by ^{241}Am are taken into consideration in this release. The fault number was eventually decided for IBL installation in this instance below 1 percent per module.

Chapter 5
Advancement in Small Pitch 3D Sensor Using Stepper Lithography

Part of this chapter has been published in:

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In the mid-1990s, 3D pixel sensors were first proposed by S. Parker and his collaborators [110], and they are currently regarded in high-energy physics (HEP) as the radiation-hardest solution for charged particle tracking [3]. 3D pixels have progressively evolved in design and manufacturing technology with a considerable downscaling in their geometrical dimensions to meet the increasingly difficult special requirements of HEP experiments. In the earliest prototypes, column electrodes had a diameter of <20 μm and a distance of >100 μm [116]; these values have decreased roughly by half for the ATLAS Insertable B-Layer (IBL) [166] in 2010, eventually becoming as small as ~5 and ~30 μm, respectively, for the latest appliances for the ATLAS and CMS detectors at the high luminosity LHC upgrade [176]. Moreover, recently modified 3D designs with small pixel cells using trenched electrodes, which are essential ingredients for the timing performance optimization required by the future LHCb detector upgrade, were proposed to improve electric field distribution and weighting field distributions in the active volume [177].

As a result, the production of 3D pixels has become increasingly difficult, with relatively dense layouts that need minimal feature sizes and a high level of precision, not only for grafting of vertical electrodes that depend on the Deep Reaction Ion Etching (DRIE) process. In these circumstances, mask aligners, the workhouse of the radiation sensor manufacture in most laboratories for decades, demonstrate apparent performance constraints with adverse impacts on device quality and manufacturing output. The decision was therefore driven for the Foundation Bruno Kessler (FBK), Trento, Italy to change to new lithographic equipment (named Stepper) for the production of the current generation of the 3D pixel [178].

5.1 Technological overview

3D pixels from the previous generation, e.g., those placed in the ATLAS IBL, are 50×250 μm^2 and the active substrate thickness is 230 µm [166]. In comparison, the new ones geared to upgrades at HL-LHC must meet significantly more demanding criteria in terms of occupancy, with a planned event stack of ~200 events/bunch crossing and radiation hardness, with the highest projected fluence of ~2×10^{16} n_{eq}/cm^2 for the most internal pixel layers. Smaller pitches and thinner active substrates are necessary to deal with these problems.

The active thickness was decreased to 150 µm, especially for ATLAS and CMS tracker improvements. Processing thin wafers with double-sided technology, that was the case for the IBL [124], would pose significant issues in wafer fragility, affecting the mechanical yield, and in the high bow, hindering the bump bonding process. The production line at FBK was particularly updated in 2014 to process 6-inch wafers with a minimum processable thickness of 300 µm. An alternative single-sided technology using a handle wafer to improve mechanical stability was thus necessary [176].

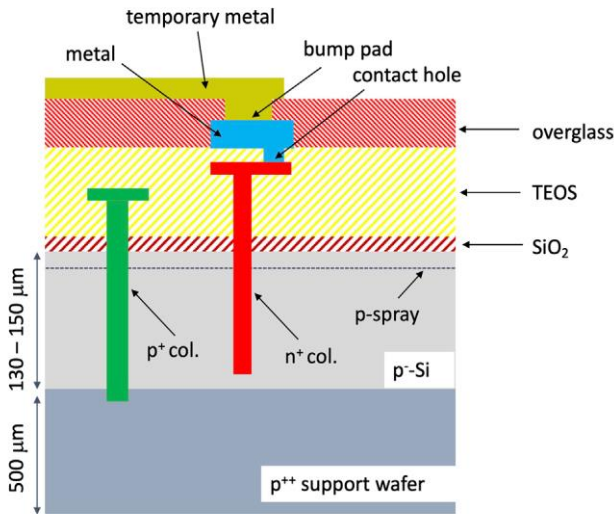

Fig. 5.1: Graphical cross-section of FBK made 3D small-pitch pixels on silicon substrates with a single-sided technology (not to scale). A similar method is also utilized for 3D trenched electrodes.

The scheme of a 3D pixel created with such an approach is shown in Fig. 5.1. A p-type, high-resistivity (Float Zone) wafer of the required thickness (130 and 150 µm for the batches described in this document were utilized) is the starting material, directly attached to a p-type, low-resistivity, 500-µm thick handle wafer. In the R&D phase, Silicon On Insulator (SOI) substrates, with a 200nm thick bonding oxide, were also utilized as an alternative to these so-known Si-Si substrates.

The devices are completely processed from the front side. After initial oxidation and p-spray implantation, the p+ columns (bias) are etched with a depth that allows penetration into the support wafer (passing through the bonding oxide in the case of the SOI wafers) [8]. This allows bias to be applied from the rear. The n+ columns (readout) are then etched, stopping around 25 µm from the support wafer at a safety distance, to prevent early breakdown [9]. Both column types are doped by thermal diffusion and filled (at least partially) with poly-Si, leaving the column openings also with tiny poly-Si extrusions. To protect the apertures of the pillars, several layers of tetra-ethyl-ortho-silicate (TEOS) oxide are applied. The contact holes are grafted into

the top TEOS layer to create a contact on the poly-Si caps between the metal and the readout columns (this is not required for the bias columns that are biased from the backside). A passivation layer of oxide-nitride is placed above the metal and holes are formed for the bump bonding pads. Finally, a temporary metal layer is placed on the pixels to enable electrical testing and is then removed. In the manufacture of 3D pixels with the trenched electrode on Si-Si substrates, with correct tailored recipes, FBK followed the same technological method as the various geometries of trenched electrodes required.

5.2 Layout of small-pitch 3D pixels

A new read-out (ROC) chip (CERN RD53 Collaboration) was created in 65 nm CMOS technology with the view of the improvements to the HL-LHC ATLAS and CMS detectors [179]. The RD53A is the first ROC prototype with 400 × 192 pixels and a total active area of 1,92 cm^2. For ATLAS and CMS applications the final files are roughly double the size. The R&D phases of all 3D processing plants (CNM in Barcelona, Spain; FBK in Trento, Italy; SINTEF in Oslo, Norway) have considered two small-pitch pixels compatible with the RD53A chip, namely 50 × 50 μm^2 and 25 × 100 μm^2 and qualified for production [11]. Both pixel geometries will be eventually utilized to instrument the new ATLAS Tracking System's innermost pixel layer (Layer 0) for the various areas (50 × 50 μm^2 in the barrel and 25 × 100 μm^2 in the ring) (ITk). These 3D pixels remain among the considered possibilities for the update of the CMS tracker, and a final decision will be taken in April 2022.

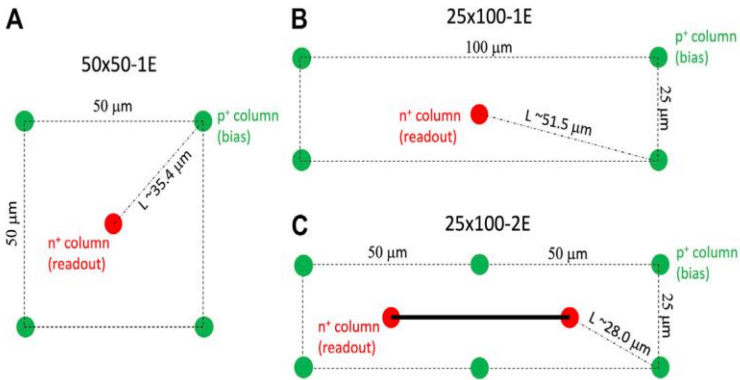

Fig 5.2: Conceptual layout of small-pitch 3D pixels for the ATLAS and CMS upgrades at HL-LHC, also representing the measurements of the inter-electrode distance L. (A) 50 × 50 1E; (B) 25 × 100 1E; (C) 25 × 100 2E.

Fig 5.2 shows the drawings of several pixels and electrodes. In Fig. 5.2A are 50 × 50 µm^2 3D pixels that were only created in a single read electrode form in the middle of a cell (50 × 50 1E). In fact, the inter-electrode spacing (L) is around 35.4 µm, short enough to avoid effective load-trapping effects [52] to provide high tolerance to radiation even after the highest fluences predicted in applications using HL-LHC. On the contrary, two versions of the 25 × 100 µm^2 pixels were designed, having one (25 × 100 1E) or two (25 ×100 2E) readout electrodes: the former (Fig. 5.2B) has L~51.5 µm, a relatively large value that was initially not considered safe from a radiation resistance standpoint (but was later demonstrated to be adequate); the latter (Fig 5.2C), with L~28 µm, would undoubtedly be more radiation hard, but at the cost of increased capacitance and technological complication.

The transition from Fig. 5.2's conceptual ideas to actual layouts imposes various limitations. Because geometrical features (minimum size, minimum distance, minimum overlap, etc.) of all layers should be patterned on the front side alone, the single-sided manufacturing technique is less flexible than the double-sided fabrication approach in this regard. The pixel layout might become crucially dependent on the layout criteria, which are mostly influenced by the lithography equipment.

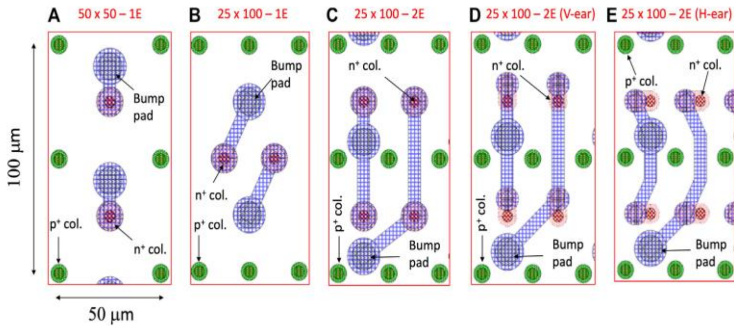

Fig 5.3: Design of small-pitch 3D pixels for the ATLAS and CMS upgrades at HL-LHC (two neighboring pixels are displayed in every single cut). (A) 50 × 50 1E; (B) 25 × 100 1E; (C) 25 × 100 2E (D) 25 × 100 2E (V-ear); (E) 25 × 100 2E (H-ear).

Fig 5.3 depicts layouts optimized for stepper lithography, i.e., using more aggressive layout rules. The configuration for the 50 × 50 1E pixels in Fig. 5.3A is fairly simple, especially since the RD53A has precisely a 50 × 50 μm^2 footprint for the bump bonding pads. If the column diameter (5 µm for readout columns, 6 µm for bias columns, indicative of FBK technology) is small enough, the architecture is not crowded. Despite its size (12 µm diameter in the passivation hole), the bump bonding pad, in particular, may be readily positioned on any side of the readout column. The alternative option of placing bumps merely on top of the readout columns, which would be appealing in numerous ways, was also successfully tested, but owing to the non-flat surface roughness at the column aperture, it was not judged safe enough for the bump bonding process yield. The arrangement for the 25 × 100 1E pixels (Fig. 5.3B) is slightly more complicated since the bump bonding pads must be arranged on a 50 × 50 μm^2 grid that matches the ROC's footprint. Even if there is an imbalance between even and odd pixel rows, the layout density is low enough. The arrangement of the 25 ×100 2E pixels (Fig. 5.3C), on the other hand, is more critical, as seen by its increased density. The extremely close distance between the bump pad and the poly-Si cap of bias columns, in particular, can be a substantial source of micro-discharges and early breakdown. The contact between metal and poly-Si on the readout column is formed in a ring shape around the column aperture in the layouts of Figs. 5.3A–B–C. The 25 × 100 2E pixels with the so-called "ears"

were also subjected to a variety of layout options. Metal and poly-Si connections are offset from the readout columns in "ear" configurations. A vertical (Fig. 5.3D), as well as a horizontal (Fig. 5.3E) offset, were applied.

It should be noted that a slim-edge (150 μm wide, compliant with the ATLAS ITk specification) termination was designed for all pixel types, based on multiple rows of bias columns that ensure the confinement of the depletion region spreading from the outermost junction columns within a short distance, so that it does not reach the highly damaged cut region [166].

5.3 Design of Trenched 3D Pixel

Many R&D efforts have been directed in recent years to the development of high-resolution timing detectors as a solution to the challenge of high-track density in future particle collider detectors. While specialized timing layers, based on LGAD sensors, will be added to the ATLAS and CMS detectors for HL-LHC applications [180], for experiments in the future, such as the LHCb and FCC, space and time measurements should be integrated into a single device [176]. Although small-pitch 3D pixels have been demonstrated to provide high timing resolution, their ultimate performance is restricted by the spatial non-uniformity of the electric and weighting fields within a pixel, which limits timing resolution [181].

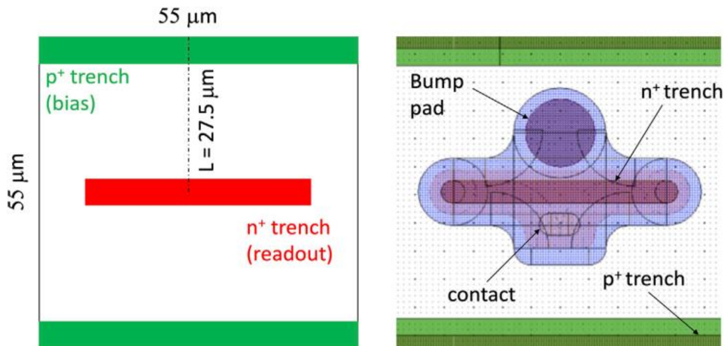

Fig 5.4: A 3D pixel with trenched electrodes: conceptual design (left) and physical layout (right).

To address this issue, the development of 3D pixel sensors with trenched electrodes was begun in Trento, which promises to give exceptional timing performance while preserving the other advantages of 3D sensors, such as radiation hardness [182–184]. With the LHCb upgrade as an application in mind, a pixel size of 55 × 55 μm was chosen for the initial testing to be compatible with the readout chips of the MEDIPIX/TIMEPIX family [185]. Fig 5.4 depicts a pixel's conceptual design as well as its matching layout.

The pixel size is somewhat larger than in fig 5.3A, but the arrangement is much denser. The requirement for the bump pad not to overlap the readout trench, where the surface is not flat so that the gap between the pad and the poly-Si cap along the bias trench is short, is a key aspect. This prompted the adoption of stepper lithography from the beginning. It is worth noting that active-edge termination is accessible in these trenched 3D pixels [3].

5.4 Batches of 3D Sensors Made at FBK

Three batches of 3D pixel sensors geared to the HL-LHC upgrades have been manufactured by FBK, all on 6-inch diameter wafers, with two more batches in the works. The first batch, produced in 2015, provided a positive assessment of the manufacturing process: while the RD53A chip was not yet available, the wafer layout contained sensors compatible with the ATLAS FEI4 and CMS PSI46dig ROCs, as well as several test structures [186]. For the first time, 3D pixel sensors compatible with the RD53A readout chip were manufactured in the second batch, with a wafer configuration that still included some ATLAS FEI4 and CMS PSI46dig compatible sensors [187]. The first two batches were created via mask aligner lithography. Because the electrical yield for the 25 × 100 2E pixels produced in batch 2 was insufficient, it was decided to employ stepper lithography in batch 3, with a wafer layout fully dedicated to 3D pixels compatible with the RD53A ROC and test structures.

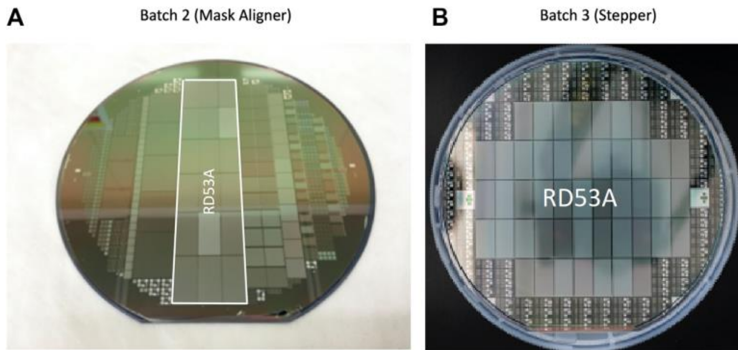

Fig 5.5: Images of batch 2 (left) and batch 3 (right) processed wafers: A wafer from batch 2 has 18 RD53A compatible sensors, whereas a wafer from batch 3 contains 47.

Photographs of two processed wafers from batches 2 and 3 are shown in Fig. 5.5, while Table 5.1 summarizes the key information for the two batches. Batch 2 utilized both Si-Si and SOI wafers with active thicknesses of 130 µm, whereas batch 3 used Si-Si wafers with active thicknesses of 150 µm (the substrate of choice for the innermost layers of both the ATLAS and CMS trackers at HL-LHC).

Table 5.1: Summary of FBK 3D small-pitch pixel batches 2 and 3 aimed at ATLAS and CMS upgrades at HL-LHC.

Batch No	Lithography Equipment	Wafer Type	Number of Wafers	Active Thickness (µm)	Number of RD53A compatible sensors per wafer			
					50 × 50 1E	25 × 100 1E	25 × 100 2E	Total
2	Mask Aligner	Si-Si	5	130	8	3	7	18
		SOI	5	130				
3	Stepper	Si-Si	8	150	13	10	24	47

FBK produced one batch of trenched 3D pixels in 2019 as part of the INFN TIMESPOT project [177], drawing on its experience with small-pitch 3D pixels and planar active-edge sensors [188, 189]. The batch was produced using wafers with a

6-inch diameter and a 150 μm active layer thickness, similar to those utilized in batch 3 previously stated. Because this was the first prototype batch, a variety of pixel layouts were developed, with differences in trench dimensions and surface layer design, as well as several processes splits to test the most essential process steps. The reticle in this example comprised complete buildings that could be exposed with a single shot. Because trenched electrodes cause the wafers to bow more than columnar electrodes, it was also chosen to limit the number of dies, with vast areas of non-etched silicon in between, to optimize mechanical yield [184].

5.5 Stepper Lithography Vs. Mask Aligner Lithography

In the field of radiation detector technologies, mask aligners are the most basic and commonly used lithography equipment. Wafer layouts are exposed in a single shot on a wafer, and the associated masks comprise full wafer layouts. When using proximity mode lithography, the mask is usually kept at a distance (proximity gap, g) of a few tens of micrometers from the wafer. The minimal resolution that may be reached is $W_{min} = \sqrt{\lambda \cdot g}$, where λ is the wavelength of the UV or deep-UV lamp, and W_{min} is typically a few micrometers [24]. By having the mask in close contact with the wafer, better resolution can be attained at the cost of a higher risk of introducing flaws from wafer to wafer due to the direct contact with the mask. The precision of the alignment is on the order of a few micrometers. These numbers are usually sufficient for most radiation sensor systems with somewhat large minimum feature sizes. Since 2005, FBK has utilized a mask aligner for 3D sensor production, making use of the double-sided alignment system for double-sided 3D sensor technologies.

Nonetheless, as seen in Figs. 5.3C–E, the architecture of the new 25 × 100 2E 3D pixels is extremely packed, with very small feature sizes, particularly for the minimum distance between the bump bonding pad and the bias columns. Its production necessitates a resolution and alignment accuracy that a mask aligner cannot accomplish while maintaining process dependability, necessitating the use of superior lithography equipment. At FBK, a stepper with a minimum feature size of

350 nm and an alignment precision of 80 nm is available, which is sufficient for the geometries under consideration.

The device dimensions are amplified (e.g., 5X) in a stepper mask called reticle, and a sophisticated optical focusing mechanism is utilized to project the reticle image to the wafer level [190]. The large space between the reticle and the wafer prevents flaws produced by a tiny gap or direct contact between the mask and the wafer in a mask aligner. A related advantage is that steppers substantially simplify the optical inspection of wafers after each lithography, which is typically a highly critical and time-consuming process for operators using mask aligners.

One unusual element of 3D sensor technology is the employment of thick photoresist layers to function as a masking material (on top of the oxide) during the Deep Reactive Ion Etching process. A thick photoresist reduces lithography resolution when using a mask aligner. The depth of focus may be adjusted with a stepper to provide the required resolution at the interface between photoresist and oxide, allowing for a clearer definition of the columnar electrode holes.

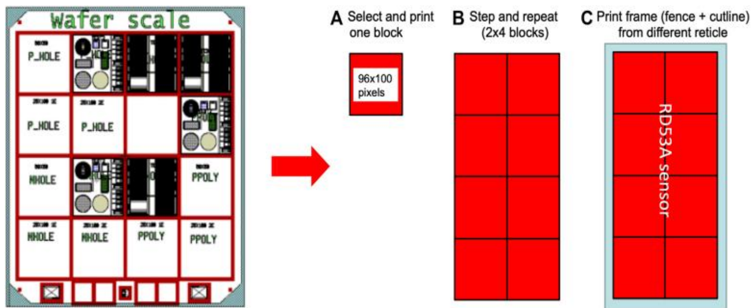

Fig 5.6: An example of reticle arrangement and exposure approach applied with stepper in batch 3.

A unique disadvantage of stepper lithography is the limited maximum exposure area, which is on the order of 4 cm^2 for FBK equipment and necessitates stitching if bigger detectors are required. Stitching was successfully tested in batch 3 at FBK, even though it was not technically essential. Although two RD53A-compatible sensors would fit into a reticle, the objective was to create all of the different pixel shapes illustrated in Fig. 5.3. This might have been accomplished by employing a variety of

reticles, each with two RD53A-compatible sensor designs. The method depicted in Fig. 5.6 was utilized as an alternative. Reticle layouts were separated into 16 tiny blocks of the same size (at wafer-level, ~5 × 5mm^2), each corresponding to one specific layer relevant to either an array of 96 × 100 pixels (i.e., one-eighth of an RD53A-compatible sensor) or a set of test structures. Each block was manually chosen using blades and printed on a wafer in a regular grid footprint. To create a full-size RD53A sensor (step and repeat operation), each layer of a block of 96 × 100 pixels was printed 2 × 4 times; moreover, a frame structure comprising a slim-edge termination and the cut lines, included in a separate reticle, was printed around it. The stepper was configured to create a wafer layout with 47 pixel sensors and numerous test structure blocks on the wafer periphery (as seen in Fig. 5.5B). The number of reticles decreased significantly as a result of this, but the stepper programming became more complicated due to the high number of "step and repeat" operations. During batch 3, this occasionally resulted in a stepper failure, requiring the lithography of some layers to be redone many times.

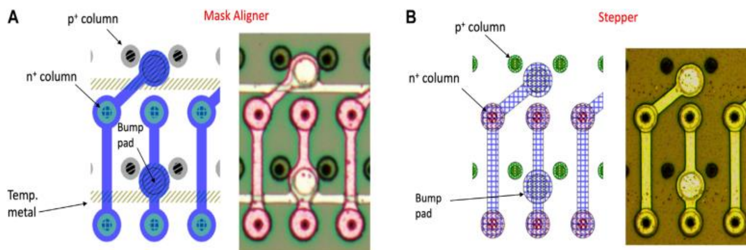

Fig 5.7: 25 × 100 2E 3D pixels produced at FBK with (A) mask aligner (also displaying temporary metal strips) and (B) stepper lithography, including layout details and micrographs.

For that, batch 3's quality was not as high as it might have been with a stepper. Nonetheless, the benefits in terms of resolution and alignment precision were obvious. In comparison to the mask aligner, stepper lithography achieves a considerably greater control of the 25 × 100 2E pixel geometry (as seen in Fig. 5.7). The metal is not properly aligned concerning the columnar electrodes using the mask aligner (Fig. 5.7A, also displaying temporary metal). The metal is too near to and occasionally overlaps the poly-Si cap of the p+ column in the region of the bump

pads, thus the whole bias voltage drops on a relatively thin TEOS layer, with a high danger of shorts owing to the non-ideal step coverage of the TEOS layer at the edge of the poly-Si cap. Stepper (fig. 5.7B) allows for more aggressive layout rules to be applied and retained in the real device implementation: notice how the metal of the bump pad is kept at a safe distance from the poly-Si cap of the p+ columns.

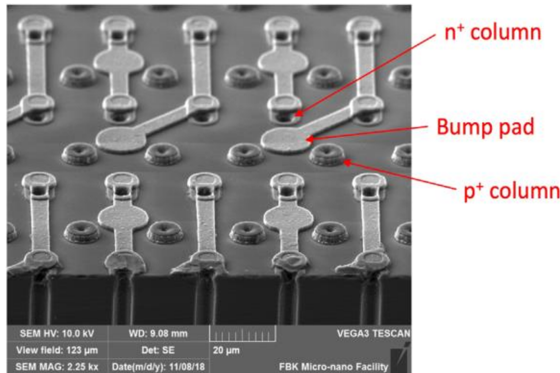

Fig 5.8: SEM image of a 25 × 100 2E 3D pixel produced at FBK using stepper lithography (layout version of Fig. 5.3D).

Fig. 5.8 shows a Scanning Electron Microscope (SEM) picture of the 25 ×100 2E pixels of Fig. 5.3D (variant with vertical ear), demonstrating the excellent pattern definition and alignment accuracy achieved using stepper lithography. All layout details are retained, and all structures are properly separated in the important zone of bump pads. The higher quality of stepper lithography was also critical to fabricating trenched 3D pixels on the first try. Fig. 5.9 shows an SEM micrograph of a set of pixels of the kind seen in Fig. 5.4, revealing details of the trenches and surface topography: in particular, the bump pads (shorted by temporary metal in the image) are well separated from the poly-Si cap at the bias trench opening.

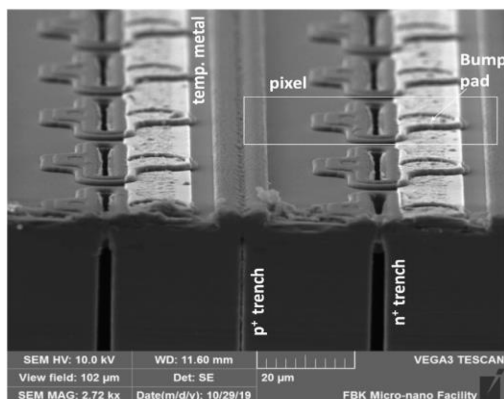

Fig 5.9: An SEM micrograph of a set of trenched 3D pixels from the first batch of stepper lithography-fabricated pixels (see the arrangement in Fig. 5.4).

5.6 Setup for Electrical Measurement at Wafer Level

Using an automated probe station with specialized probe cards, pixel sensors were electrically tested at the wafer level, at room temperature, and under dark conditions. The testing technique initially established for the IBL 3D pixels [124, 166] was utilized for this purpose. Over the passivation, a layer of temporary metal is placed and patterned in strips; each strip connects several pixels through the bump pad holes, shorting them to a common probe pad.

Strips are routed in groups to the same probe pad, and their current-voltage (I-V) curves are monitored in parallel up to 50 V reverse bias. In batch 2, 8 strips (160 columns) of 192 pixels (192 rows) (1,536 pixels, 3.84 mm^2 area) were measured in parallel; in batch 3, where the number of RD53A sensors is considerably higher, 20 strips (400 columns) of 192 pixels (192 rows) (3,840 pixels, 9.60 mm^2 area) were tested in parallel to minimize overall measurement time. Because of the extra surface current contribution (MOS effect) generated by the temporary metal, the measured currents exceed the real pixel currents [124].

The total current of a sensor is then calculated by adding all of the strip currents, and sensors are classified according to the ITk 3D pixels' leakage current requirements, which are:

- depletion voltage V_{depl}<10 V
- breakdown voltage larger than the operation voltage $V_{op} = V_{depl}$+20 V
- leakage current at operation voltage $I(V_{op})$ < 2.5 μA/cm^2.

The depletion voltage, which is calculated from the capacitance-voltage curves of test diodes, is relatively low (around 3 V). However, the top limit for depletion voltage was evaluated as a worst-case scenario, with V_{op} set to 30 V (in practical which should not be more than 23 V) and the relative leakage current compared to the specified threshold set by Itk requirements at 30 V. It's worth noting that, by doing so, if the leakage current meets the specifications at 30 V, the breakdown voltage situation is also evaluated to see whether it meets the specification or not.

5.7 Experimental Outcome from Small-pitch 3D Pixels

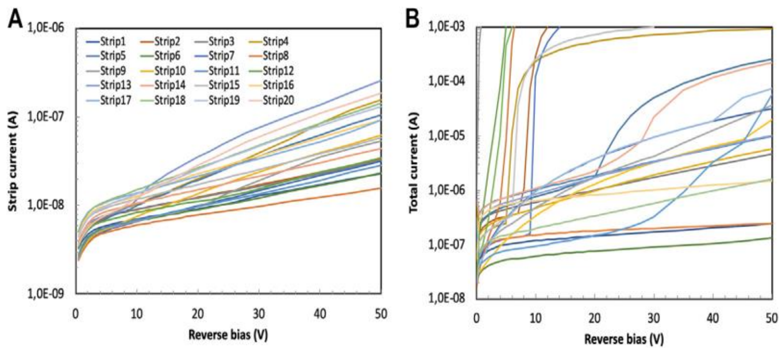

Fig 5.10: Batch 3 I–V curves of 25 x 100 2E 3D pixels: (A) currents of all strips (3,840 pixels each) in one sensor, and. (B) total currents of all sensors in Wafer 38, where each curve corresponds to each sensor.

Fig. 5.10A shows an example of the I-V curves recorded with temporary metal on the 20 strips connecting the corresponding pixels (3,840 pixels in each strip) in a 25 × 100 2E sensor from batch 3 wafer 38. While this sensor is good, with a total current of less than 600 nA at 30 V, there is a non-negligible dispersion of the strip current of around 10 nA, which is often assessed for 3D technologies [124, 166]. For all of the 25 × 100 2E sensors on the proposed wafer, the sum of the 20 strips I-V curves

yields the total sensor I-V curves, as illustrated in Fig. 5.10B. About half of these sensors (specifically 13 out of 24) are functional, with low leakage currents and a breakdown voltage greater than 50 V (the highest bias used in the test), whereas the rest either exhibit early breakdown or a smooth rise in the curves, eventually leading to significant leakage values in the orders of micro amperes.

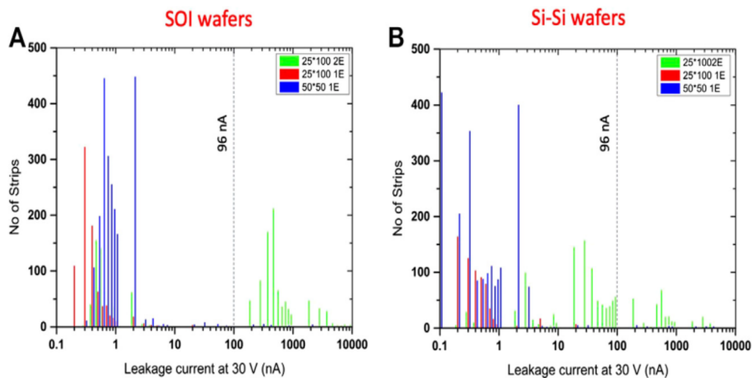

Fig 5.11: Leakage current distributions at 30 V reverse bias in all 3D strips (1,540 pixels each) from batch 2 SOI wafers (left) and batch 2 Si-Si wafers (right).

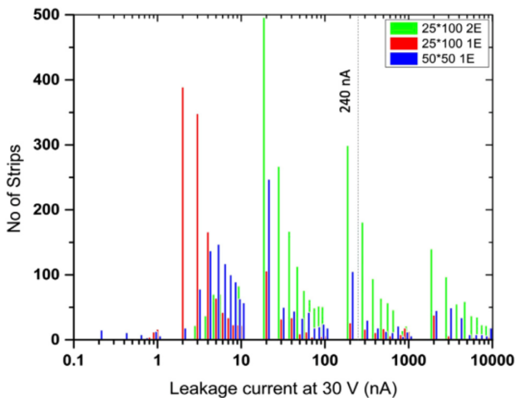

Fig 5.12: Leakage current distributions at 30 V reverse bias in all 3D strips (3,840 pixels each) from batch 3 wafers.

Fig 5.11 (for batch 2, distinguishing between the two types of wafers) and Fig. 5.12 (for batch 3) show the distributions of all the strip currents measured at a reverse bias of 30 V to provide a thorough overview of the data. The distributions reveal

numerous peaks at different leakage current values: the peaks at low leakage currents (less than 96 nA for batch 2, 240 nA for batch 3)are mostly due to wafer-to-wafer variations, and occasionally even within single sensors, whereas the peaks at high leakage currents (more than 96 nA for batch 2, 240 nA for batch 3) are attributable to process flaws. When scaled to the area covered by each strip, the specification on the leakage current at the operating voltage $I(V_{op})<2.5$ A/cm^2 translates to an upper limit of 96 nA for batch 2 and 240 nA for batch 3. Fig. 5.11 and 5.12 show these values as vertical dashed lines. Most of the strips of 50 × 50 1E and 25 × 100 1E pixels had leakage currents far below the specification, both in batch 2 and batch 3, with astonishingly low values ranging from a fraction of 1 pA to a few tens of pA per pixel after normalization to the number of pixels. As a consequence, the yield of these two geometries for complete sensors is high enough (more than 60%). On the other hand, it can be shown that the strips of 25 × 100 2E pixels had larger leakage currents on average. This is consistent with the higher electric fields caused by the shorter inter-electrode spacing reported by CNM [191].

Table 5.2: Wafer electrical yield summary for all RD53A-compatible 3D pixel sensors from batches 2 and 3.

Batch No	Lithography Equipment	Wafer Type	Wafer yield (%) for RD53A-compatible sensors Average/Minimum/Maximum		
			50 × 50 1E	25 × 100 1E	25 × 100 2E
2	Mask Aligner	Si-Si	60.0/12.5/100.0	60.0/0.0/100.0	11.4/0.0/28.6
		SOI	67.5/50.0/75.0	60.0/33.3/100.0	25.7/14.3/42.9
		All	63.7/12.5/100.0	60.0/0.0/100.0	18.6/0.0/42.9
3	Stepper	Si-Si	58.2/38.5/84.6	62.9/30.0/80.0	38.1/8.33/66.7

Most importantly, a large proportion of the 25 × 100 2E strips had currents over-specification in batch 2 and, to a lesser extent, in batch 3, with clear implications for yield for this design. Table 5.1 summarizes the wafer electrical yield of all RD53A compatible sensors from both batch 2 (for different wafer types and overall) and

batch 3. The statistics for each sensor shape relate to the proportion of sensors satisfying the leakage current criteria on the total number of sensors present on a wafer, as shown in Table 5.1. The average, minimum, and maximum values are provided, indicating rather broad wafer-to-wafer non-uniformities. On the one hand, comparable yield values with mask aligner and stepper are obtained for the two non-critical geometries (50 × 50 1E and 25 × 100 1E), on the order of 60% on average. This outcome, which is identical to that produced from chosen wafers in the ATLAS IBL 3D pixel manufacturing at FBK [166], is adequate given the high technological complexity. While remaining lower than for the other two geometries, the production of 25 × 100 2E pixels nearly quadrupled in batch 3 compared to batch 2, reaching about 40% on average, with small variations across the three layouts illustrated in Fig. 5.3C–E. While this finding confirms that the 25 × 100 2E geometry is the most critical, it is also hopeful and suggests that, in the case of an improved reticle design, manufacturing of this pixel geometry might be achievable at FBK with an acceptable yield.

5.8 Experimental Outcome from Trenched 3D Pixels

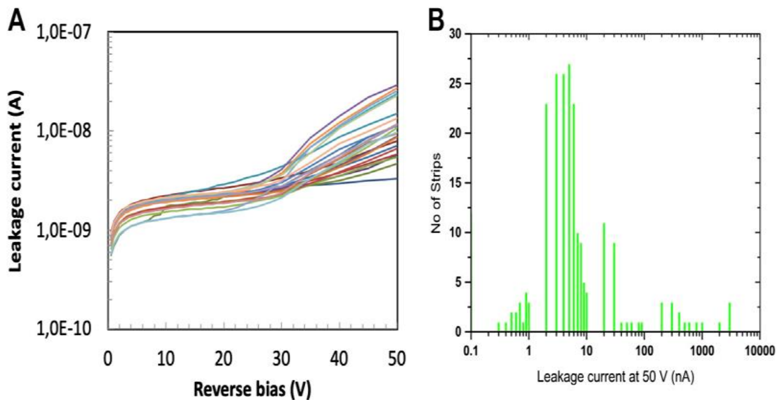

Fig. 5.14: (A) I–V curves of all 3D Trenched-Electrode pixel sensors in a die, and (B) Distribution of total leakage current at 50 V. Wafer 2,249 from the first batch contains arrays of 18×18 pixels.

The earliest prototypes of trenched 3D pixels have good electrical properties. Fig. 5.14 A shows the I-V curves of all pixel sensors (18-pixel arrays) in a die from Wafer 2,249, whereas Fig. 5.14 B shows the leakage current distribution at 50 V bias for all pixel sensors on the considered wafer. Most sensors have a leakage current of a few nA, which equates to roughly 10 pA per pixel, which is a surprisingly low figure. The depletion voltage is only a few Volts (2~3 V), while the breakdown voltage is over 200 V [183], allowing a large operating margin to run the pixels with carrier velocity saturation, which reduces the time to reach electrodes, thus improving timing performance. The initial beam tests on these devices connected to separate readout circuits yielded extremely promising results, with a timing resolution of around 20 ps [177].

5.9 3D SS Batch 4

After successful completion of the stepper batch, another batch of 3D single-sided wafers was fabricated with a simplified stepper lithography process. The process started in July 2019 and was completed by June 2020.

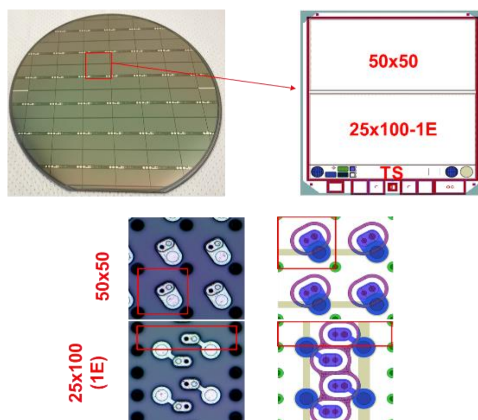

Fig. 5.15: (Top) A real-time picture of a wafer from 3D-SS Batch-4, and the design of each step block. (Bottom) Real-time picture from the top and layout of both geometries.

This batch was also made with 2 cm × 1 cm sensors, compatible with RD53a RoC. Each reticle of the wafer has one 50 × 50 and one 25 × 100 1-E sensor, as well as test structures, as can be seen from Fig. 5.15 (top). This reticle was stepped 44 times to cover a 6-inch wafer. The design of the pixels was made targeting the production design, as can be seen in Fig. 5.15 (bottom), also trying p-stop around n columns, to estimate the yield for the production phase. 12μm bump pads were created for bump bonding with the RoC and were connected with metal to an n-column. For smooth connection, a contact surface was also etched with an n-column (Fig. 5.16).

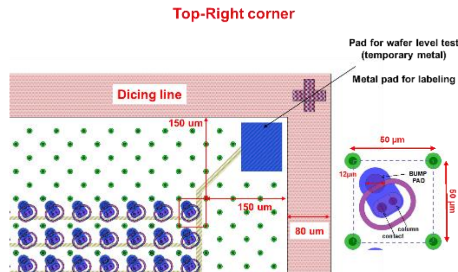

Fig. 5.16: Design of 50 × 50 μm^2 sensor geometry, seen from the top right corner. All the n-columns were shorted by temporary metal and connected with a pad to allow wafer-level tests.

For wafer-level electrical tests, all the n columns were shorted with temporary metals and were connected to two large metal pads on two upper corners, as can be seen from Fig. 5.16. The right pad was also used for labeling the name and position of the sensor.

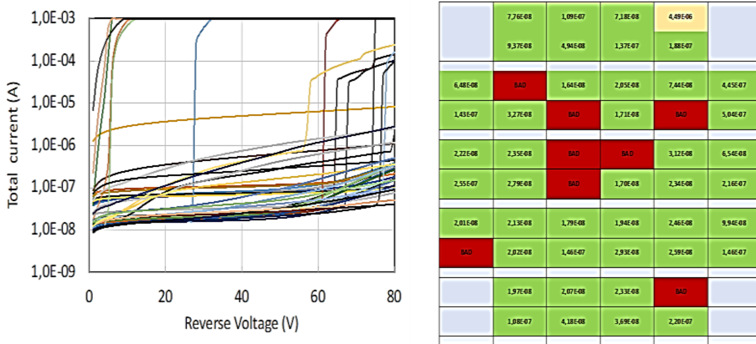

Fig. 5.17: (Left) IV characteristics curve from one wafer of the 4th batch and (right) wafer map depending on leakage current of the same wafer.

Fig. 5.17 (left) shows the IV characteristics from one wafer of the 4th batch of 3D-SS fabrication. Most of the sensors have fare leakage current between 10 nA and 100 nA at 30V, which is the operating voltage, with a breakdown voltage of more than 80 V. The wafer map (Fig. 5.17(right)) depending on leakage current shows only a few bad sensors, which shows a high yield for this wafer of batch 4.

5.10 Pre-Production Batch

The 5th batch of the 3D single-sided technology was made according to the final production plan, considering 10% of the whole production. The batch was completed by the summer of 2021. This batch was made with 2cm × 2cm size sensors, compatible with RD53b or ItkPixV1 RoC, only with 50 × 50 μm^2 geometry, as per the ATLAS requirements. Each 6-inch wafer has 24 sensors with the above dimensions, and the periphery is covered with test structures or Process Control Monitors (PCM) blocks, as can be seen in Fig. 5.18. The sensor design is similar to the fourth batch, but with twice the active area (384 rows and 400 columns).

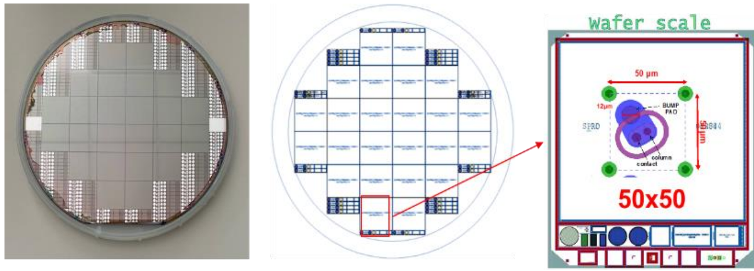

Fig. 5.18: (Left) Real-time picture of pre-production wafer, and (right) design of the wafer with a zoom of one reticle.

Seven wafers were produced in this batch, all having temporary metals to connect all the n columns with two metal pads on two upper corners of each sensor, to perform electrical tests at the wafer level. The ATLAS collaboration has set specific criteria to be met for this batch, which is given in Table 5.3.

Table 5.3: ITk criteria for produced wafers from all vendors and value from FBK Pre-Production batch.

Quantity	*Value set*	*Pre-production batch of FBK*
Depletion voltage	<10 V	<=3V
Breakdown voltage	$>V_{depl} + 20$ V	>80 V
Leakage current at RT	<2.5 µA/cm^2 at $V_{depl} + 20$ V	~0.05 µA
Leakage current slope	$I(V_{depl} + 10\text{ V})/I(V_{depl} + 5\text{ V})<2$	~1.06
Number of good sensors/wafer	5	Yes, for all of the wafers
Yield over a delivered batch	>50%	59.5%
Optical Inpection	No strains, residues or scratches, or damage to the sensor area	Yes

IV tests were performed on all the seven wafers of this batch. The current was limited to 1 mA and voltage to 80 V. Fig 5.19 (left) shows a distribution of the leakage currents at 30 V, which is the operating voltage for ATLAS. It shows that the maximum number of sensors has a leakage current of around 200 nA, which makes around 0.05 μA/cm^2 current density, much lower than ITk specifications. Fig 5.19 (right) shows a distribution of the breakdown voltages for all wafers. It shows that most of the sensors' breakdown voltages are concentrated at 80V because the voltage limit was set to 80 V for the automatic probe station so that it doesn't stress the wafers. It means most of the sensors have a breakdown voltage of more than 80 V, which is much higher than ITk specifications.

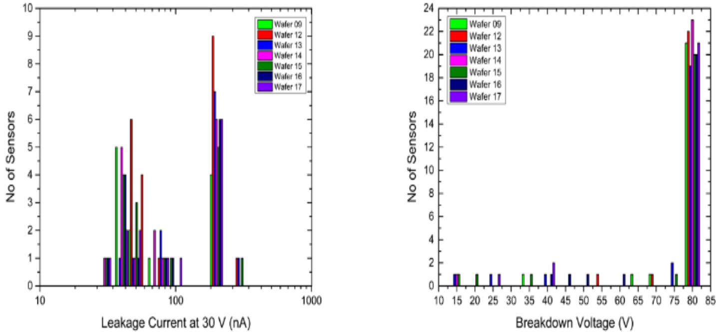

Fig. 5.19: (Left) Distribution of leakage current at 30 V (operating voltage) at log scale for all wafers, and (right) distribution of breakdown voltage for all wafers. Voltage was limited to 80V, sensors showing at 80 V may have higher breakdown voltages.

5.11 Conclusion

FBK has begun to employ stepper lithography rather than mask alignment for the process of complex 3D pixel sensors to benefit from the considerably better definition of crucial layout features it can give. Despite the difficulties encountered during the manufacturing of the first stepper batch (batch 3), the overall results are good. This is owing to the decision to accommodate various design variants and the

resulting difficulty in the exposure strategy. The yield for the crucial 25 × 100 2E geometry was significantly increased (approximately doubled) compared to the prior batch utilizing the mask aligner (batch 2), reaching almost 40% on average. The yields for the other non-critical geometries 50 × 50 1E and 25 × 100 1E, on the other hand, remained relatively constant, around 60% on average, which is acceptable given the complex fabrication technology of 3D sensors and the very high density of columnar electrodes involved in small-pitch designs. These findings show that a stepper may be used to make complex small-pitch 3D sensors. The last two batches of small-pitch 3D sensors manufactured at FBK, including pre-production for ATLAS ITk, employing a simplified technique to expose the sensors and test structures included in a reticle in a single shot, have increased yield and wafer-to-wafer consistency. FBK has also successfully manufactured 3D Trenched Electrode pixel sensors using the stepper for the first time, with a very low leakage current and high breakdown voltage.

Chapter 6
Characterization of 3D pixel sensor modules based on RD53A readout chip

Part of this chapter has been published in:

Stefano Terzo, Maurizio Boscardin, Juan Carlotto, Gian-Franco Dalla Betta, Giovanni Darbo, Ole Dorholt, Francesco Ficorella, Giuseppe Gariano, Claudia Gemme, Giulia Giannini, Sebastian Grinstein, Andreas Heggelund, Simon Huiberts, Angela Kok, Ozhan Koybasi, Alessandro Lapertosa, Magne Elk Lauritzen, Maria Manna, Roberto Mendicino, Hideyuki Oide, Giulio Pellegrini, Marco Povoli, David Quirion, Ole Myren Rohne, Sabina Ronchin, Heidi Sandaker, Abdulla Samy, Md Arif, Bjarne Stugu, Leonardo Vannoli,

"Novel 3D pixel sensors for the upgrade of the ATLAS inner tracker",

Frontiers in Physics,(2021) pages: 2

Md AA Samy, A Lapertosa, L Vannoli, C Gemme, G-F Dalla Betta,

"Characterization of FBK 3D pixel sensor modules based on RD53A readout chip for the ATLAS ITk",

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In its evolution to the High Luminosity phase (HL-LHC), which is foreseen to start in 2029, the Large Hadron Collider will be upgraded to reach about seven times its current nominal instantaneous luminosity, predicted to reach up to an astonishing threshold of 3000 fb^{-1}. Like other major experiments, ATLAS will upgrade its sub-systems to cope with higher particle rates, hit occupancy, and radiation damage. The entire tracker system will be replaced by an all-silicon detector, namely the Inner Tracker (ITk), made of a pixel detector core with five Barrel layers and several End-cap rings, surrounded by a micro-strip system with four Barrel layers and six End-cap disks. Due to its proximity to the proton-proton beam collisions, the silicon pixel detector will have to sustain unprecedented radiation levels, surpassing 1×10^{16} n_{eq}/cm^2 during its lifetime [192].

In the twenty-five years since their invention, 3D pixel sensors have gradually progressed in their design and fabrication technology and are currently accepted as the most radiation-hard solution for charged particle tracking in High Energy Physics [193]. For this reason, they were chosen to equip the innermost layer (L0) of the ITk pixel detector. For this purpose, a new generation of 3D pixels has been developed [176], compatible with the new ATLAS readout chip (ROC), the ITkPix, and its precursor designed by the RD53 Collaboration, the RD53A [194]. The new 3D pixels have higher granularity (50×50 μm^2 or 25×100 μm^2) and smaller active thickness (150 μm) as compared to the state-of-the-art 3D pixels installed in the ATLAS Insertable B Layer (IBL) [166]. With these downscaled geometries, the ITk 3D pixels will maintain the occupancy at the ~% level despite the expected event pile-up of∼200 events/bunch crossing and ensure a good spatial resolution; moreover, owing to the 3D design, the small pixel size corresponds to a small inter-electrode distance, that enhances the radiation hardness [52].

6.1 Characterization at Wafer Level

At the wafer level, pixel sensors are electrically verified by measuring current-voltage (I-V) curves at room temperature and in darkness with a probe station. A temporary metal layer is placed over the passivation and patterned in strips to shortcircuit rows of pixels to probe pads for this test [166]. Summing the I-V curves of all strips yields the total current. Capacitance-voltage (C-V) curves are also measured on some samples.

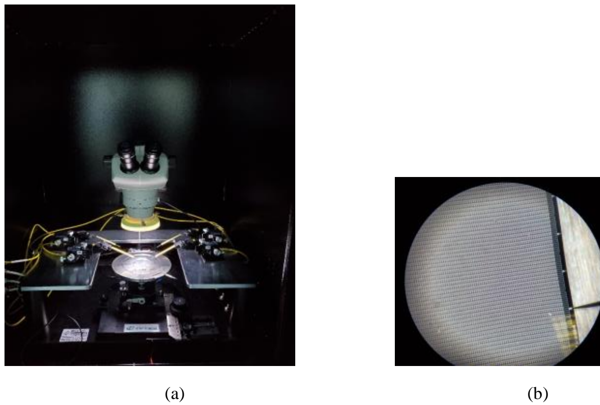


Fig. 6.1: (a) Electrical characteristics set up in University of Trento. (b) Columns, metal pad, and probe connection under the microscope.

Before dicing, all the sensors were tested and characterized using a 4-point probe station as seen in Fig. 6.1. Wafers were biased from the backside using the probe station's chuck. All the 20 n^+ electrodes in a column were shorted using a temporary metal strip, which is visible in fig. 6.1 (b). Again, every strip was connected with a metal pad, which can be read by a probe. 400 columns of one sensor were divided into 20 strips of columns, current and capacitance could be read from each strip and added to estimate the current and capacitance of the whole sensor.

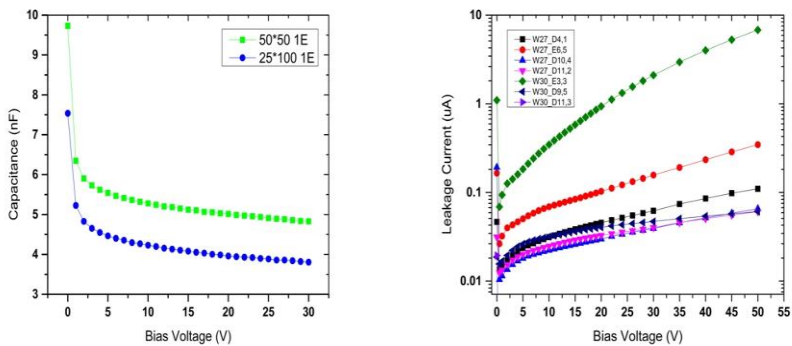


Fig. 6.2: (Left) C-V and (Right) I-V characteristics of selected sensors of the two geometries.

Fig. 6.2(left) shows the C-V curves of sensors of two geometries, 50 × 50 1E and 25 × 100 1E sensors: from the initial knee in the curves, it can be inferred that depletion is achieved at a very low voltage (~2 V) in both cases, well below specifications. The total I-V curves of a few selected sensors of both geometries are shown in Figure 6.2 (right). Most sensors have very low leakage currents: after normalization to the full sensor active area (1.92 cm^2), values of ~0.1 $\mu A/cm^2$ are found at 30 V. Despite its higher current, which reaches ~1.8 $\mu A/cm^2$ at 30 V, also sensor E3.3 is within specifications.

It should be noted that the measured currents overestimate the true pixel currents, because of the additional surface current contributions (MOS effect) caused by the temporary metal [178]. This same problem affects the measured capacitances: the normalized values at 25 V for the 25×100-1E and 50×50-1E pixels are ~50 fF and ~65 fF, to be compared to ~20 fF and ~50 fF, respectively, as measured on the test diodes [192]. All the values are listed in Table 6.1 for better understanding.

Table 6.1: Electrical characteristics of the selected sensors.

Geometry	Wafer	Sensor name	Leakage current at 30V nA	Capacitance at 30 V nF	Full depletion voltage V
50×50 1E	27	E6.5	157	4.83	~1.2
	30	E3.3	210		
25×100 1E	27	D4.1	62.1	3.81	~1
	27	D10.4	39.2		
	27	D11.2	40.1		
	30	D9.5	47		
	30	D11.3	3.38		

6.2 Characterization at Module Level

To read from these new small pitch sensors, a new Readout Chip (RoC) was developed by the RD53 Collaboration, to be used for the ATLAS and CMS Phase II pixel detector upgrade, named RD53A RoC. The RD53A chip is produced in 65 nm CMOS technology, and the size is 20.0 mm by 11.8 mm and the pixel matrix is 400 pixels wide by 192 pixels tall, where a pixel cell is 50 × 50 μm^2. The main specifications of the RD53A are derived from HL-LHC conditions: pixel hit rate 3 GHz/cm, trigger rate 1 MHz, total power per pixel less than 10 μW with low noise, and low in-time threshold. The RD53A pixel matrix is built up of 50×30 identical cores with 8×8 pixels each. Within one core the 64 front ends are placed as 16 analog islands with 4 front ends each, which are embedded in a flat digital synthesized "sea" [195]. One pixel core contains multiple pixel regions with shared logic and triggers latency buffering. The RD53A contains three different front-end designs which are identified as synchronous, linear, and differential. The synchronous front end uses a baseline "auto-zeroing" scheme that requires the periodic acquisition of a baseline instead of pixel-by-pixel threshold trimming. The linear front end implements a linear pulse amplification in front of the discriminator, which compares the pulse to a threshold voltage. The differential front end uses a differential gain stage in front of the discriminator and implements a threshold by unbalancing the two branches. The front-end designs share the pixel matrix area as shown in Fig. 6.3. The synchronous front end is 16 core width while linear and differential are 17 core width.

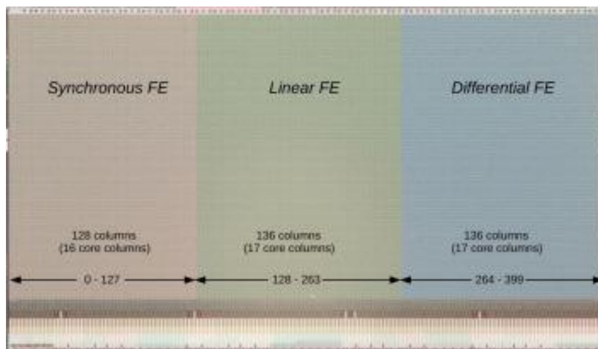


Fig. 6.3: Arrangement of front-end flavors in RD53A with indicated digital readout architecture. The pixel column number range of each flavor is shown along the bottom.

Among these three FEs, ATLAS experiments have chosen differential and CMS experiments have chosen linear front end.

Several sensors of different geometries from wafers 27 and 30 of Batch 3 were bump bonded to RD53A readout chips at Leonardo (Rome, Italy) and connected with Single-Chip Card (SCC) at INFN Genova for further tests. Selected modules were irradiated with protons at fluences of 5×10^{15} n_{eq}/cm^2 and 1×10^{16} n_{eq}/cm^2 at Birmingham. Leakage currents were measured in Genova after irradiation at -25^0 C, which is the foreseen operating temperature of the ATLAS ITk. The working modules were then sent to DESY (Hamburg, Germany) to be tested under a 6 GeV electron beam. The I-V characteristics were re-measured there at -45^0 C by cooling with dry ice.

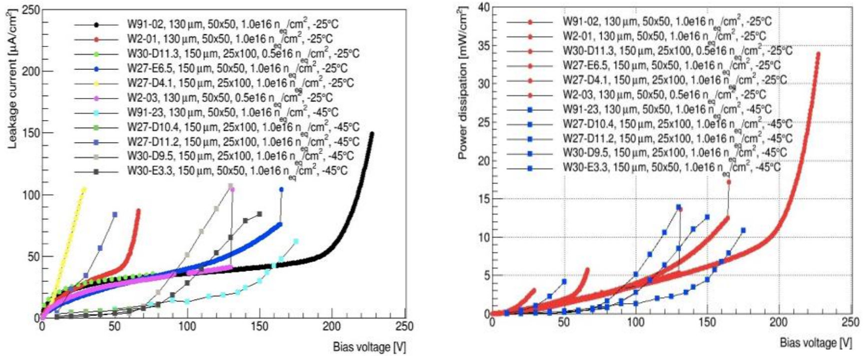
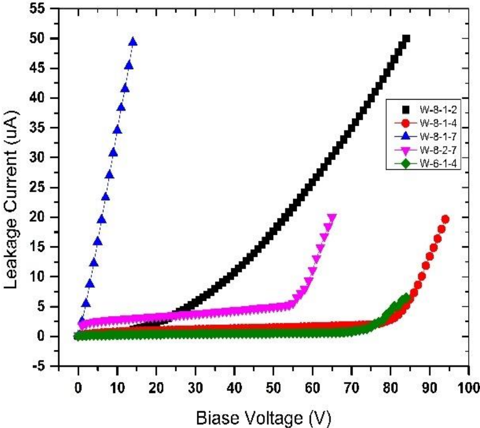


Fig. 6.4: (Left) I-V characteristics of the modules tested at -25^0C (bold lines) and -45^0C (thin lines); (Right) corresponding power dissipation estimate of the same modules, where -25^0C corresponds to bold red and -45^0C corresponds to thin blue lines.

Fig. 6.4 shows the I-V and power dissipation curves of several modules made from sensors of Batch 2 and Batch 3 at the two different temperatures, -25^0C in a climate chamber and -45^0C with dry ice. Most modules could be safely operated up to a voltage of 100 V, which is expected to ensure a hit efficiency >97% at the considered fluences, with a power dissipation lower than the ITk specification value of 10 mW/cm^2 at a fluence of 1×10^{16} n_{eq}/cm^2.

Some more modules were tested at the Institute de Fisica d'Altes Energies (IFAE), Barcelona before sending them to Los Alamos National Laboratory (USA) (LANL) to irradiate up to 1.6 × 10^{16} n_{eq}/cm^2 fluence. A total of 5 modules were checked, and all of them were integrated with sensors made in CNM with a mask aligner lithographic process.



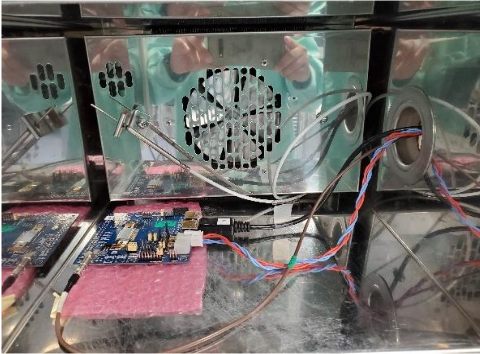


Fig. 6.5: (Top) I-V characteristics of the modules of IFAE tested at -25⁰C; (bottom) test setup inside a climate chamber for testing RD53A single-chip card at cold temperature.

Table 6.2: Electrical characteristics of the selected modules.

Wafer No	Sensor No	Geometry	Breakdown Voltage (V)	Leakage current at 30 V (μA)
W8	1-2	50 × 50 1E	-	5.62
W8	1-4	50 × 50 1E	80	1.15
W8	1-7	50 × 50 1E	-	-
W8	2-7	25 × 100 2E	55	3.80
W6	1-4	50 × 50 1E	75	0.41

Modules were tested inside a climate chamber as can be seen in Fig. 6.5 (bottom) at -25^{0}C, with a dry air supply. I-V curves were measured using automated scripts. Fig 6.5 (top) shows a comparative view based on the I-V of the modules, which is more elaborately recorded in Table 6.2. Depending on breakdown voltage and lowest leakage current, modules W8-1-4, W8-2-7, and W6-1-4 were selected for the irradiation campaign.

6.3 Data Acquisition Setup

The data acquisition (DAQ) setup for RD53A RoC is mainly built depending on the Yet Another Rapid Readout (YARR) system. The YARR system is a data acquisition system developed for the current generation of Pixel detector readout chips and scalable to the next generation. It allows for a stronger emphasis on data processing in software as opposed to traditional processing in FPGAs, which reduces reliance on the utilized hardware and allows for the usage of current multi-core CPU architectures. The PCIe bus, which permits the high bandwidth (~30 GB/s) and low latency transmission (300 ns) of raw Pixel module data into the host system's memory, is an important element of this readout system. Compared to traditional architectures, this provides several advantages. The high-level software, which is a more familiar area for the scientists utilizing these devices, contains the majority of the readout system's important functionality. Furthermore, because the hardware, especially the FPGA, is primarily utilized as a reconfigurable I/O interface, there is very little overlap between firmware and software [195]. This is important to use the same software in the laboratory for testing as well as for the final detector.

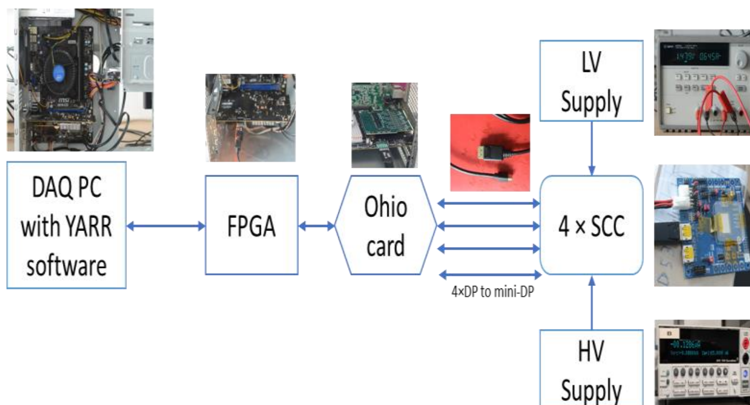


Fig 6.6: DAQ setup for a single-chip card with YARR system.

Fig. 6.6 shows a schematic diagram of the YARR setup. The first key component of the setup is the DAQ PC, as the pc will obtain all the raw data, process it, and analyze it with the YARR software. It is always better to have a high-end processor to increase the processing speed. In Trento, we have two DAQ computers, one with an Intel Core i7 and another with a Core i9 processor. It is also very crucial to select the motherboard for the pc as it has been seen a lot of motherboards don't work with the required FPGAs, due to mismatching in data rate and communication channel. Both the DAQ pc's in Trento have MSI motherboards with two PCIe card slots. Another crucial thing about selecting the pc is that it needs to have a power supply of more than 500 W, as it is required to supply adequate power to the FPGA to work. The pc should have Centos 7 operating system installed in it, as YARR software only runs in this environment.

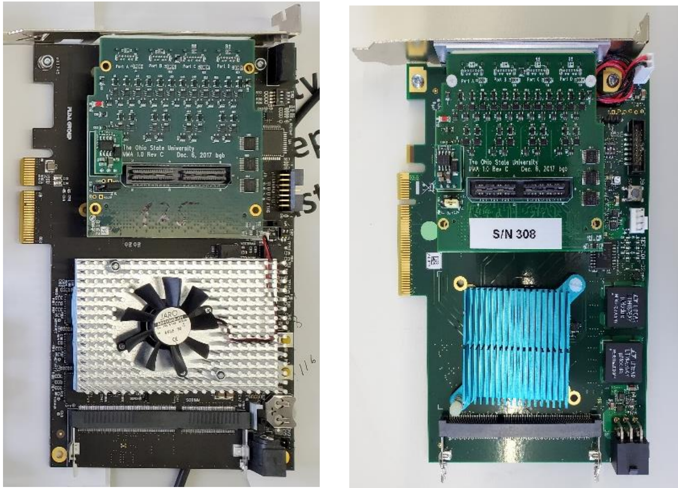


Fig. 6.7: Left is an XpressK7 card with an Ohio card attached and right is a TrenzR 002 card.

An FPGA has to be attached to the PCIe port of the motherboard to acquire data from the module. The recent upgrade of the YARR suggests using XpressK7 and TrenzR 002 card for that [196]. The XpressK7 uses a Kintex7 FPGA with four connections, each having a 12 Gb/s bandwidth. PCI-e v2.1, with a maximum bandwidth of 20 Gb/s, is used by the XpressK7. Because the new RD53A readout chip can attain a bandwidth of 5 Gb/s, it was necessary to replace the YARR FPGA board to improve the bandwidth of the DAQ system. The PCI-e endpoint is likewise implemented in the FPGA by the XpressK7. This allows the firmware to work with a broader selection of PCI-e FPGA boards at the expense of having to deal with PCI-e in firmware. Trenz card comes with all the same qualifications, but with a more cost-effective solution. In Trento, both of the cards are being used, as in Fig. 6.7. The FPGA needed to be connected with pc via a JTEG cable for uploading firmware into it. The firmware needs to be of accurate configuration for specific functions, i.e for single-chip readout or multiple chip readout, and specific speed, otherwise there will be a communication error.

The Ohio card is a multi-module adapter card, which enables one FPGA to communicate with 4 modules at the same time. It has to be mounted on FPGA and enabled by a jumper. It has 4 mini-DP ports to connect with modules with Display

Port to mini-DP cable. Each port is designed to communicate with one single RD53A chip, but to read the HitORs, two ports can be modified by replacing capacitors with 0Ω resistors. In such a case, two ports are connected with one module to read HitORs. ‘HitOR’ is a function where if the FE gets a ‘Hit’, The comparator output is fed to the digital pixel region through logic gates which allows to gate it off or combine (logic OR) with a digital test signal. Additionally, the comparator output is fed to a column-parallel wired-OR circuit.

A Single-Chip Card (SCC) is a PCB board made to mount an RD53A sensor bonded with a 3D or planar sensor and hold all the readout electronics and interface. It was designed at the University of Bonn, that’s why it is also called the Bonn card. An SCC has two power inputs, one is the main input, and another is the auxiliary input. It also has two DP inputs, 1 and 2.

Fig. 6.9: Left is a full Single-chip card with a 3D sensor of geometry 50 × 50 μm^2 1E attached with RD53A ROC and right is an SCC with a bare module, i.e ROC without sensor attached.

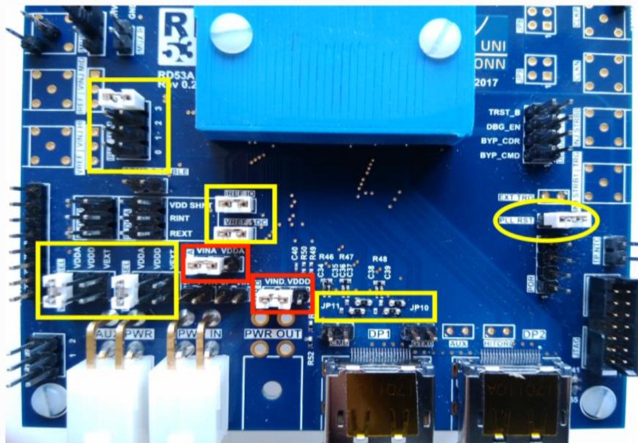


Fig. 6.10: Jumper configuration to activate SCC on SLD0 mode.

Fig. 6.9 shows two different configurations of SCC. An SCC has a lot of open pins for different purposes, some of them have to be jumpered to activate the chip. Fig 6.10 shows the jumper configuration to activate the card in SLD0 mode. In this mode, the PWR_IN should be supplied with 1.8 V from a low voltage power supply. The current compliance should be 1A. The card can also be operated in Shunt mode, by shifting the jumpers to the right shown in the red boxes. In this mode, the voltage should be 1.2 V. To communicate with the DAQ pc, a DP cable should be connected to the DP1 port. DP2 port is used for HitOr operation. The lemo connector in the top left part of the card is to be connected with a high voltage source to bias the sensor. It is also possible to do an I-V test through this connector. The current and voltage can vary, but the current limit should not exceed 100 µA, or it may burn the sensor. Fig. 6.11 displays a full setup for SCC inside the cleanroom of the University of Trento.

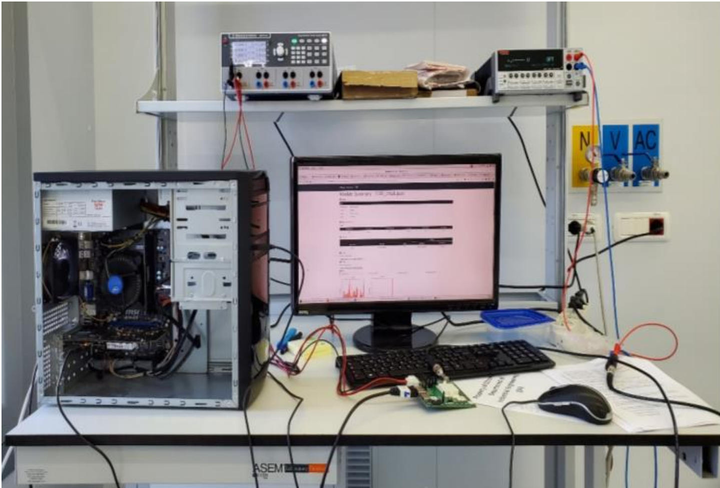


Fig. 6.11: A full data acquisition setup for a single chip card, containing DAQ pc with FPGA connected with a single-chip card, HV, and LV power supply.

6.4 Visual Inspection

After receiving an SCC, the first thing is to do a visual inspection. The card should be visually checked for any damage and a picture should be taken for record. Then the chip and the wire bonds should be checked thoroughly with the help of a microscope as seen in Fig. 6.12. If there is any wire bond seen as damaged, it has to be immediately reported and fixed if possible, otherwise, the SCC should be sent back to do wire bonding again.

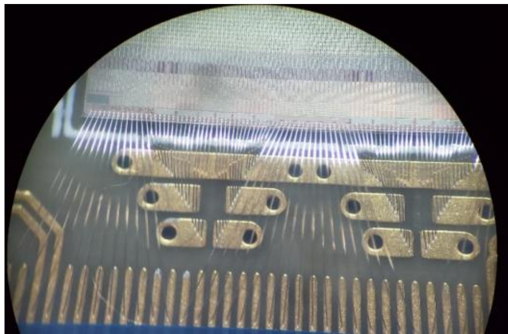


Fig. 6.12: Wire bond inspection under a microscope, showing that all the wire bonds are well connected.

6.5 IREF Trimming

Every single chip card comes with four-bit IREF_TRIM pins on the left side of the chip. 'IREF' stands for Internal current Reference, which is a bias generator reference current selection. The idea of these pins is to set them in such a manner so that the chip gets 4 µA current constantly. To determine the bits, the IREF_IO pin needs to be connected with a current meter, in this case, a Keithley 2470 was used. Then the card has to be turned on in SLD0 mode. The bits need to be changed in different configurations to find when the current becomes 4 µA. This can differ from card to card. Fig 6.13 shows a setup for finding the trim configurations. After setting the bits, the IREF_IO pin should be jumpered again. Also, the AdcRefTrim value in the configuration file was set to 14 to get 0.9 V in the VREF_ADC pin, which is a voltage reference generation for on-chip ADC.

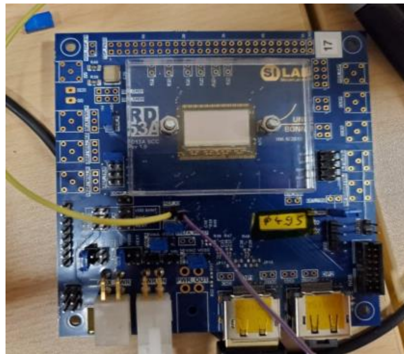


Fig. 6.13: Finding IREF trimming.

6.6 Internal Voltage (VDD) Trimming

There are two important internal voltage pins in the single-chip card, VDDD, and VDDA. These two pins regulate the digital and analog power supplies in the Front Ends (FE). Two parameters and module configuration files, SldoDigital and SldoAnalog govern these two voltages respectively. Values of these two parameters have to be changed to see when both VDDD and VDDA ports give 1.2 V. However, sometimes depending on the module FEs, it might be needed to increase the values a little bit.

6.7 Basic communication

For first and basic communication, the SCC has to be powered up by a low voltage power supply, also it should be connected with the Ohio card. If it is in SLD0 mode, the voltage should be 1.8V. If the current is in the range of 500-600 mA or some slightly up and down, it's normal. If it's too high or too low, it is better to power cycle once or twice. After it, a digital scan can be done to check whether it's communicating or not. If the scan is done and the histogrammer is plotting, the communication is done. If it shows a communication error, a few things have to be checked:

I. Power cycle once and try to scan again.

II. If still having the same error, check the connectivity file, whether it is referring to the exact configuration file or not

III. Check the configuration file. Check 'CdrSelSerClk', whether it matches with firmware speed or not. Values for different speeds are:

- 0 : 1280Mbps
- 1 : 640Mbps
- 2 : 320Mbps
- 3 : 160Mbps

IV. If there are multiple FPGAs connecting with the PC, check the controller file and the spec no for the correct FPGA

V. If nothing works, check the firmware again whether is it the correct one or not

6.8 Bare Module 046C

A bare module means a single chip card without any sensor attached to the readout chip. These SCCs are useful to understand chip characteristics, and also to train DAQ setup and laboratory individuals. A bare module was received named 046C for such purposes.

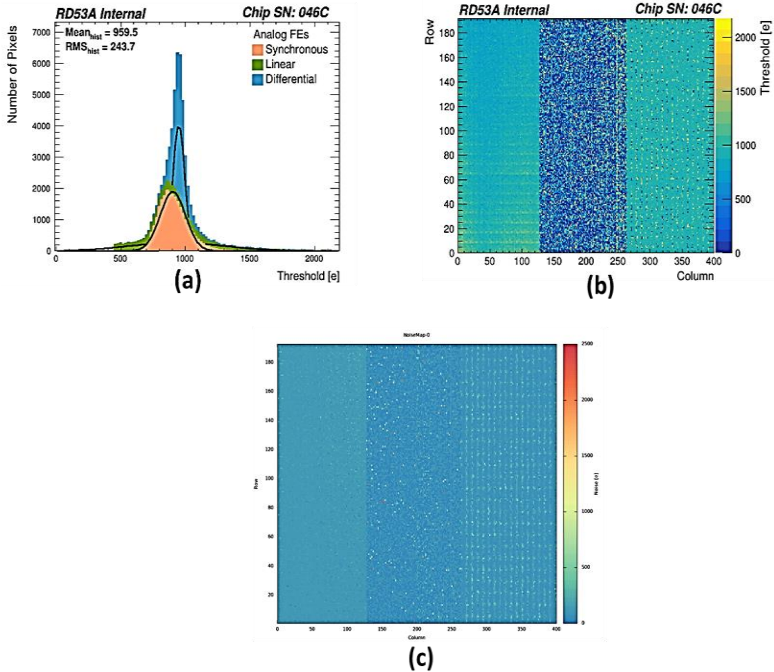


Fig 6.14: (a) Threshold Distribution, (b) threshold map, and (c) noise map of module 046C for the Synchronous, Differential and Linear FEs .

Fig 6.14 shows different characteristics of bare module 046C. All the front ends were tuned to 1000 electrons. Differential FE was tuned perfectly, as can be seen from both Fig. 6.14 (a) and (b). The linear and synchronous are however slightly deviated and more flattened. A lot of pixels in linear FE is not responding to tuning, thus going to zero, reducing the number of pixels tuned in linear FE. This is not usual for all chips normally, but was seen for a lot of other chips also in other sites. The mean distribution of all FEs are in 959.5 electrons, with an RMS value of 243.7, which is still acceptable. The noise of all FEs are comparatively low as the chip doesn't have any sensor attached to them.

6.9 Module 1039

Module 1039 contains a 50 × 50 1E sensor made in FBK, Trento, Italy. It was bump bonded and flip chipped with RD53A chip in Leonardo, Rome, and wire-bonded in INFN Milan.

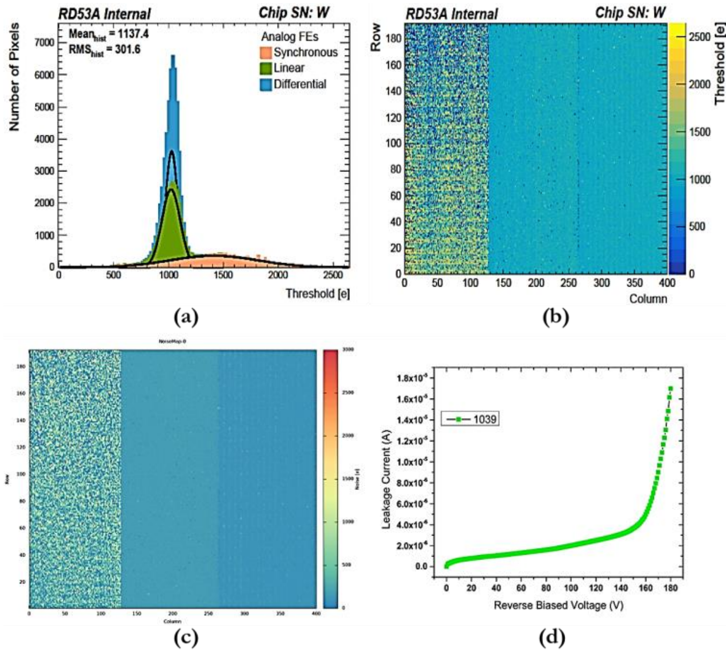


Fig. 6.15: (a) Threshold distribution, (b) threshold map, (c) noise map, and, (d) I-V curve of module 1039.

Fig. 6.15 shows different scan results and characteristics of the module. All of the three front ends, differential, linear, and synchronous were tuned to 1000 electrons for threshold. This threshold was set to see the performance of all three FEs at such a low value. It was also seen before by other sites that performance in a lower threshold than 1000 electrons is not acceptable. The distribution looks very good for linear and differential FE, while the synchronous FE is a bit flattened which means it is not responding (Fig. 6.15 (a)). The noise map estimates lower noise levels for the module. IV characteristics as seen in Fig. 6.15 (d) look good in terms of leakage current.

6.10 Module W8-2-7

Module W8-2-7 contains a 25 × 100 2E sensor made in CNM, Barcelona. It was bump bonded and flip chipped with RD53A chip and wire bonded and mounted on SCC in IFAE, Barcelona.

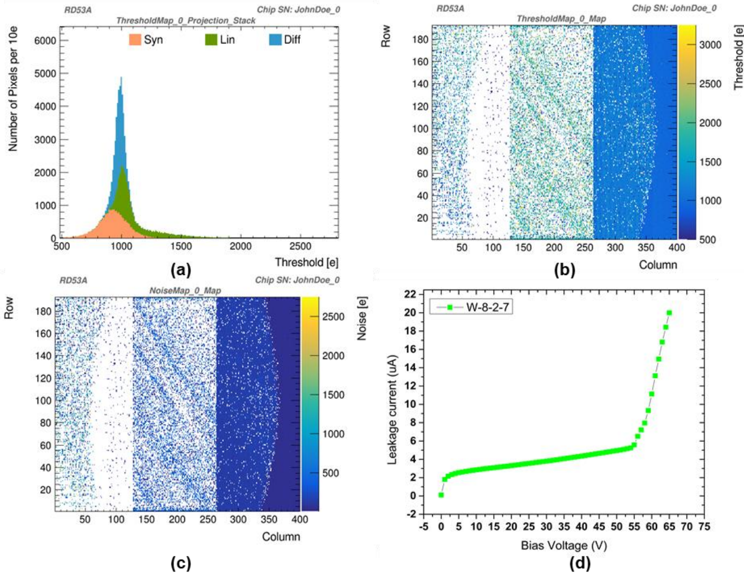


Fig 6.16: (a) Threshold distribution, (b) threshold map, (c) noise map, and, (d) I-V curve of module W8-2-7.

Fig. 6.15 shows different scan results and characteristics of the module. All of the three front ends, differential, linear, and synchronous were tuned to 1000 electrons, the distribution looks very good for linear and differential FE, while the synchronous FE is a little bit flattened (Fig. 6.16 (a)). From the threshold map and noise map (Figs. 6.16 (b) and (c)), it is evident that some large bump disconnections are giving a conical shape to the edges. The noise map estimates low noise levels for the module. IV characteristics as seen in Fig. 6.16 (d) look good, with lower breakdown voltage but a wider operating voltage range with a low leakage current as compared to module 1039. Due to good scan results and characteristics, this module was sent for irradiation at Los Alamos National Laboratories, New Mexico, USA.

6.11 Module W8-1-4

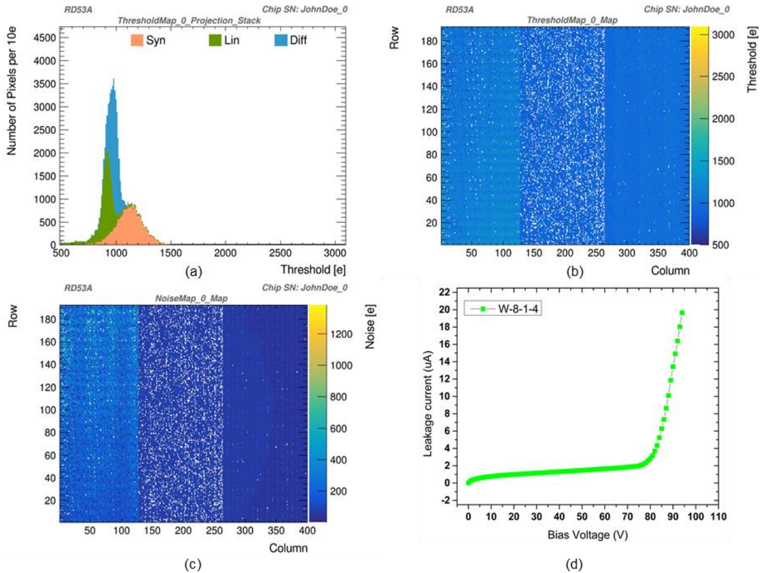


Fig 6.17: (a) Threshold distribution, (b) threshold map, (c) noise map, and, (d) I-V curve of module W8-1-4.

This module is based on a 50 × 50 1E sensor made by CNM, Barcelona, and bump bonded and assembled in IFAE Barcelona. This module was tuned to 1000 electrons threshold for all three FE. The threshold distribution as seen in Fig. 6.17 (a) shows a good agreement with that for linear and differential FEs, but the synchronous FE is a little bit deviated from the mean, which is normal. The threshold map in Fig. 6.17 (b) also matches the distribution. The noise map in Fig. 6.17 (c) shows a low noise level of the module for all FEs. The IV in Fig. 6.17 (d) looks good, with a moderate breakdown voltage at 80 V and a low leakage current at 30 V, which is the operating voltage. Due to good characteristics and scan results, this module was sent for irradiation up to a fluence of 1.6×10^{16} n_{eq}/cm^2 at Los Alamos National Laboratories, New Mexico, USA.

6.12 Module W8-1-2

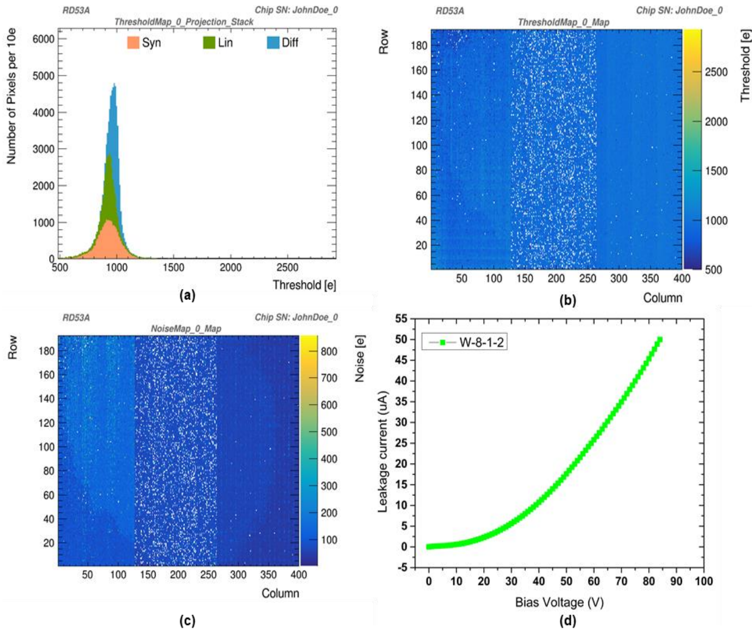


Fig 6.18: (a) Threshold distribution, (b) threshold map, (c) noise map, and, (d) I-V curve of module W8-1-2.

This module has also a 50 × 50 1E sensor fabricated at CNM and assembled in IFAE, Barcelona. This module was also tuned to 1000 electrons, and the threshold distribution in Fig. 6.18 shows a very good agreement with that for all three FEs. Threshold map and noise map in Figs. 6.18 (b) and (c) show a hint of bump disconnection at the edges having lower threshold values which are represented by dark colors, also with a lower noise level for all FEs. The IV curve in Fig. 6.18 (d) shows strange behavior, with current increases exponentially with reverse-bias voltage. Though this module has good scan results, it was rejected for irradiation due to increasing current.

6.13 Module W8-1-7

This module was also made with a 50 × 50 one electrode readout sensor from the same wafer, W8, fabricated in CNM and assembled in IFAE, Barcelona. Like the others, it was also tuned to 1000 electrons. Threshold distribution in Fig. 6.19 (a) shows a very narrow Gaussian profile for linear and differential FE with a mean of around 1000 electrons, whereas synchronous FE has a more flattened distribution. The threshold map in Fig. 6.19 (b) also has a good agreement with the distribution. The noise map in Fig. 6.19 (c) shows a low noise in all the FEs, but it also gives a hint of bump disconnections at the edges. The IV curve in Fig. 6.19 (d) shows a resistive behavior, with current increases linearly with the increase of voltage. Because of this, it was rejected for the irradiation campaign.

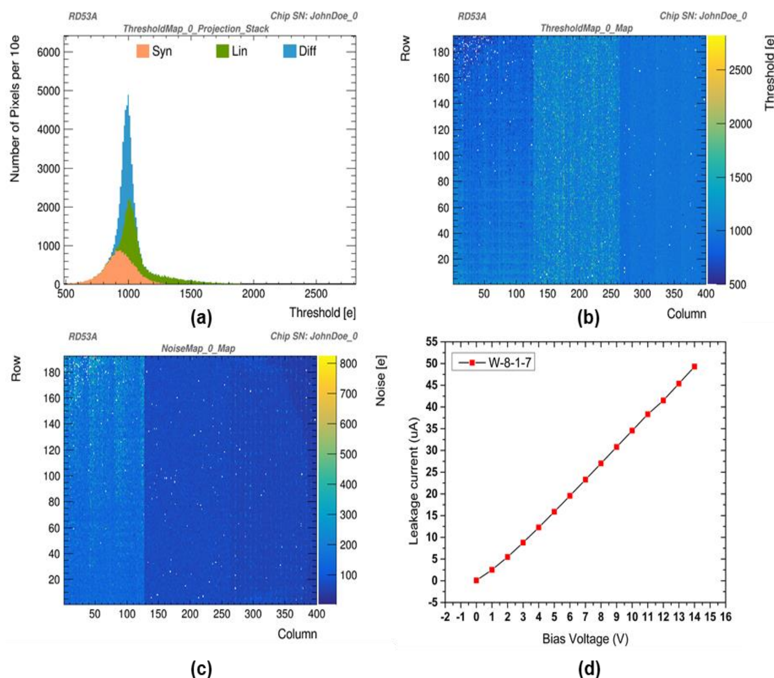


Fig 6.19: (a) Threshold distribution, (b) threshold map, (c) noise map, and, (d) I-V curve of module W8-1-7.

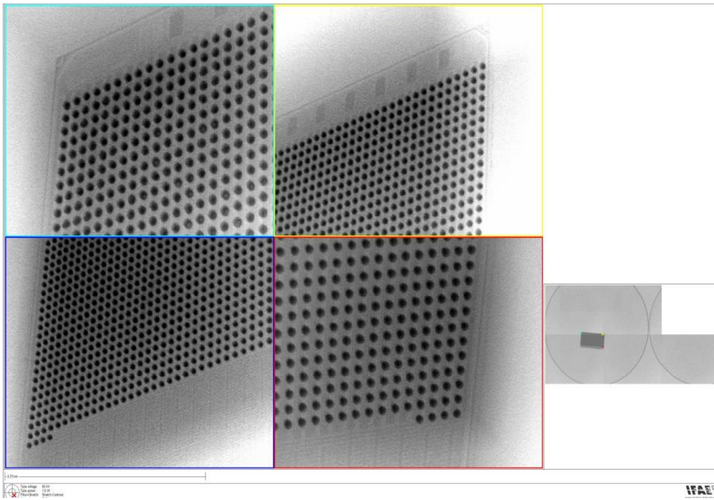


Fig. 6.20: X-ray scan at the edges to see the bump connections.

To understand the bump disconnection hints seen in the noise map, the module was scanned with X-rays to see the edges, as can be seen in Fig. 6.20. The edges were checked carefully, but due to the PCB board and aluminum, it was not possible to understand very clearly. To investigate more, two scans were done. At first, a source scan was done with a random trigger which is a noise scan. The SCC was kept in a dark environment and some noise scan was done to map all noisy pixels. Then a ^{90}Sr source was attached on top of the sensor, and a noise scan was done for five minutes. Fig 6.21 (a) shows the result of the noise scan. Then a disconnected bump scan was done, as seen in Fig. 6.21 (b). Both of the scans confirmed that there are disconnected bumps at the edges of the sensor, which also confirms that the hints got from the noise map are true.

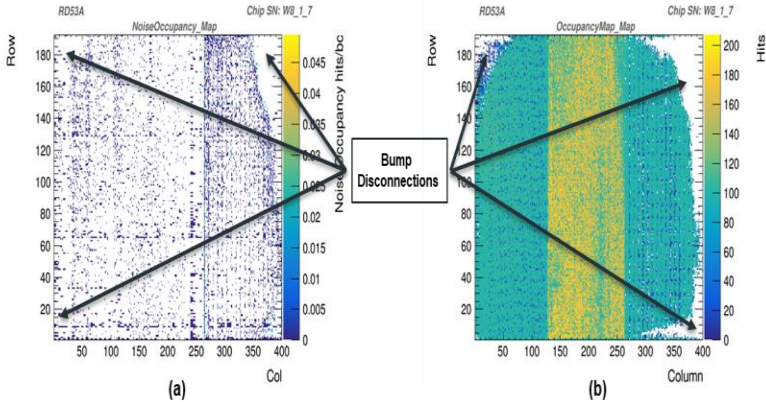


Fig. 6.21: (a) Noise scan with a ^{90}Sr source on top and (b) disconnected bump scan of module W8-1-7.

6.14 Test Beam Results

Module D11.3 (25×100-1E) from wafer 30 of Batch 3 from FBK was irradiated at the Medical Physics cyclotron of the University of Birmingham in the UK with 27 MeV protons up to 5×10^{15} n_{eq}/cm^2 fluence. It was tested at DESY using EUDET telescope [194], and keeping it cold with dry ice at a temperature of -45^{0}C. Fig. 6.22 shows the threshold scan after tuning. The RD53A chip includes three sections with different analog front-end (FE) designs, i.e., synchronous, linear, and differential FE [195]. In this study, only the differential and linear FE were considered. The former was tuned to a threshold of 1000 electrons, the latter to 1500 electrons, since at the 1000 electrons threshold a lot of pixels were noisy. Still, in linear FE, a lot of pixels remained untuned, so they were masked and discarded from the calculation. After tuning, all the noisy pixels were masked. The module was kept perpendicular to the particle beam for data taking, as can be seen in Fig. 6.23.

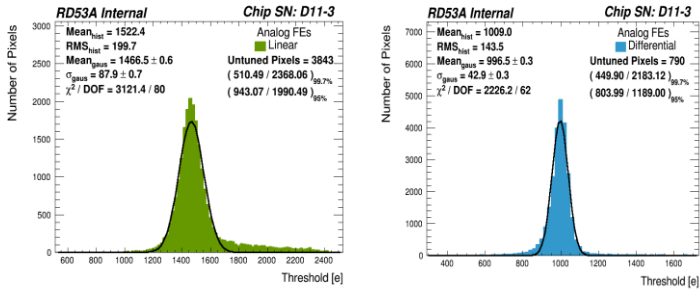


Fig. 6.22: Threshold scans of module D11.3: (Left) linear FE after tuning to 1500 electrons; (Right) differential FE after tuning to 1000 electrons.

Fig. 6.23: Experimental setup in DESY with DUT in the middle of six MIMOSA EUDET telescope planes.

Fig. 6.24 (Left) shows the hit map for the linear FE in a single-pixel area at 20 V bias. At such a low voltage, hits are efficiently detected only in the middle of the pixel around the readout column. The efficiency improves as the voltage is increased, and at 80 V bias (Fig. 6.24 (Right)) most of the pixel area becomes fully efficient.

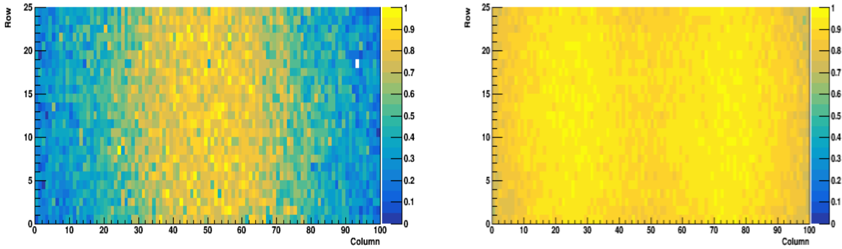


Fig 6.24: Pixel hit efficiency maps of module D11.3 for linear FE: (Left) 20 V bias; (Right) 80 V bias. All geometrical dimensions are in micrometers.

Fig. 6.25 shows the efficiency vs voltage plot of module D11.3 for the two FEs: 96% efficiency is reached at 40 V for the differential FE and 80 V for the linear FE section. This difference is likely due to the different threshold tuning of the two FE sections.

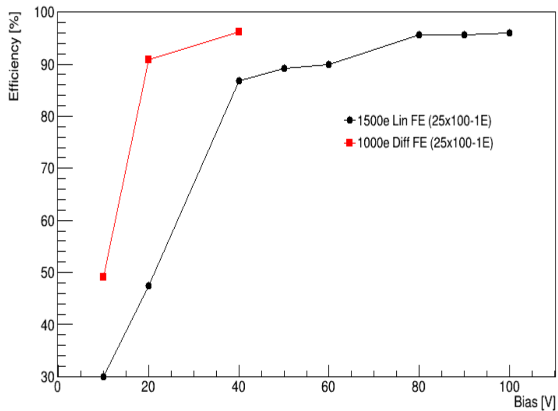
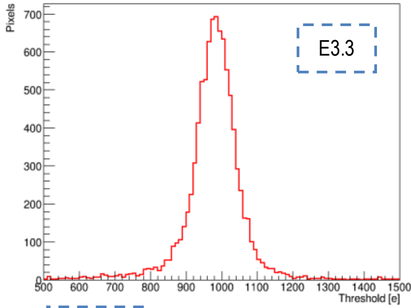
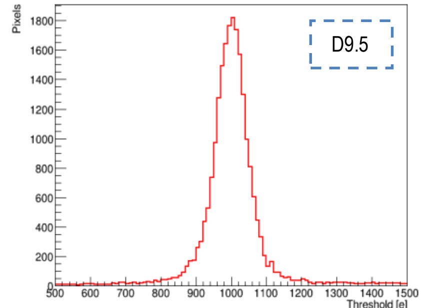
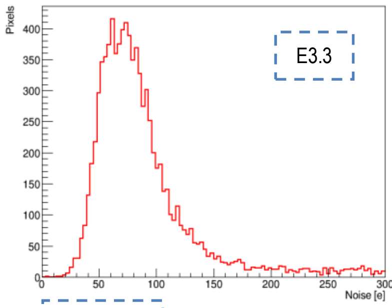


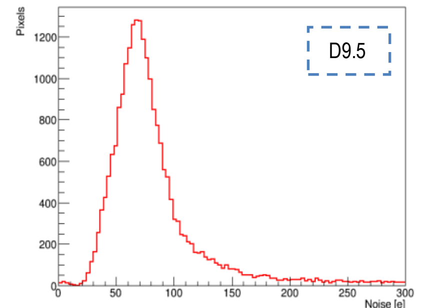
Fig 6.25: Efficiency vs bias voltage plot for linear and differential FE of Module D11.3.



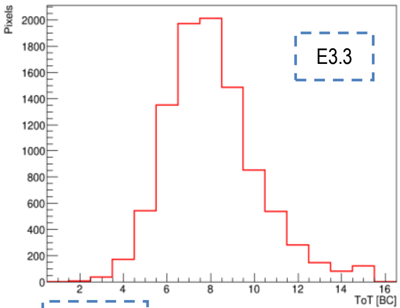


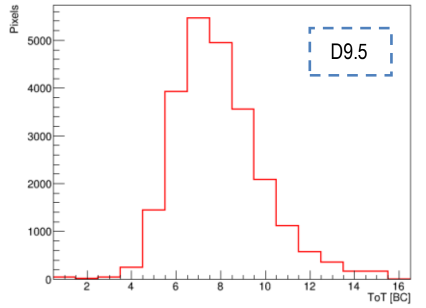
1st Row





2nd Row





3rd Row

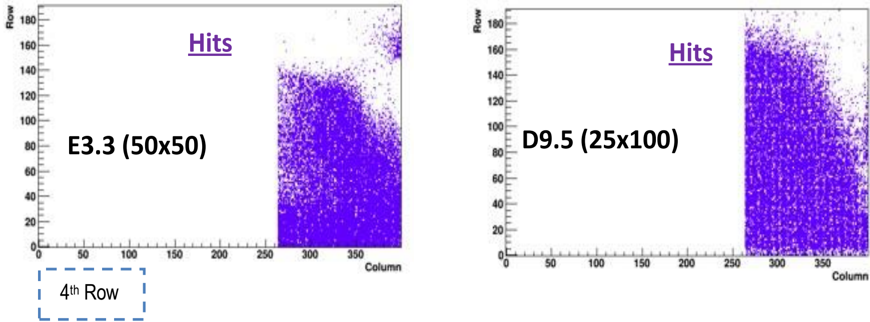


Fig. 6.26: Tuning of two modules E3.3 (left) and D9.5 (right): (1st row) Threshold distribution, (2nd row) noise distribution, (3rd row) ToT signal distribution with 10000 electrons at 7 BC. Hits from data taking under 6 GeV electron beam at DESY are shown in the bottom row.

The other two modules based on sensors from wafer 30 of Batch 3, E3.3 (50×50-1E) and D9.5 (25×100-1E), were tested under a beam in a different campaign at DESY. Both modules were irradiated up to 1×10^{16} n_{eq}/cm^2 fluence at the Cyclotron Radio Isotope Center (CYRIC) of the Tohoku University in Japan using 70 MeV protons. Only the differential FE was considered since it was selected by the ATLAS Collaboration for the development of the final ITkPix chip. The FE was tuned to 1000 electrons as the threshold, and with 10000 electrons @7BC for Time over Threshold (ToT), as can be seen in Fig. 6.26. Also, shown in Fig. 6.26, the noise for both the modules was quite low, ~70 electrons. All the noisy pixels were masked with noise scans. The modules were kept perpendicular to the beam for data taking. It should be noted that the top right corners of both the modules had some problems with disconnected bumps and did not record any hits. Those portions were excluded from data analysis.

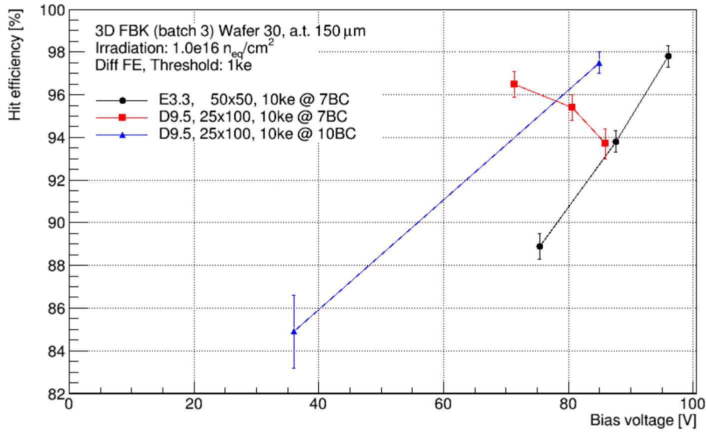


Fig 6.27: Efficiency vs bias voltage plot for the modules E3.3 and D9.5

Fig. 6.27 shows the efficiency vs voltage plot for the two modules. Module E3.3 with a 50×50 1E sensor reached an efficiency of 98% (higher than the 97% ITk target value) at ~95 V bias. For module D9.5 with a 25×100 1E sensor, the efficiency was higher than 96% at 70 V but then dropped with increased bias. This behavior could be explained by a calibration problem when tuning the Time Over Threshold signal with 10000 electrons at 7 Bunch Crossing, which caused the ToT to decrease when increasing the bias [196]. After recalibration by tuning the ToT signal with 10000 electrons at 10 BC, the problem was solved, and the module reached an efficiency >97% efficiency at ~80 V. These results are slightly better in terms of operating voltage than those obtained by the CMS Collaboration on FBK modules made from sensors of Batch 2, where efficiency of ~ 97% was reached for both 50×50 1E and 25×100 1E geometries at 150 and 120 V, respectively. The difference is likely to be ascribed to the thinner active layer of sensors from Batch 2 (130 µm) as compared to Batch 3 (150 µm),

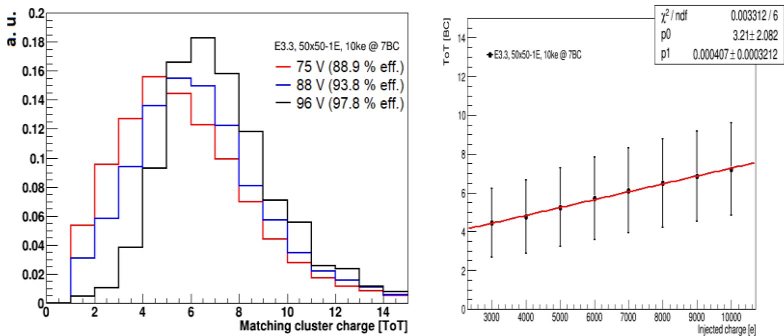


Fig. 6.28: (Left) Charge calibration and (right) ToT vs injection charge for module E3.3.

which, due to charge trapping, requires a higher bias voltage to reach the same signal amplitude [196]. The charge collection efficiency was estimated for both E3.3 and D9.5 modules: it was found to be ~70% while reaching 97% hit efficiency. The value is calculated by exploiting the ToT vs charge calibration (Fig. 6.28 (left) for the E3.3 module calibration plot), obtained by injecting different charges and checking the corresponding ToT distribution. The charge collected at different bias voltages was evaluated as the MPV obtained by fitting with Landau function the cluster ToT distribution from test beam data (Fig. 6.28 (right)) for module E3.3 cluster ToT distribution. Increasing the bias voltage more charge is collected: the peak of the cluster ToT distribution shift towards higher ToT values. In particular, at a bias voltage of 96 V, the collected charge is ~7500 electrons, corresponding to about 70% of the expected amount of charge released in 150 µm (11000 electrons).

6.15 Conclusion

FBK has already proved to reach the benchmark to fabricate small pitch 3D sensors for HL-LHC, with figuratively good yield with their new lithography process. The process of bump bonding with the chip and wire bonding with a single-chip card has been also established well, for all groups and vendors. However there are still some problems with the bump disconnections at the edges, investigations have been done to understand more and steps are being taken to improve them. The data acquisition

system for the SCC has been established well, and more and more investigations are being done to get more and more efficient on that.

Characterization of FBK 3D pixel sensor modules irradiated with protons up to a fluence of 1×10^{16} n_{eq}/cm^2 was reported here. After irradiation, the I-V curves were found to be acceptable in most of the cases, with sufficiently high breakdown voltage and power dissipation lower than the ITk target value of 10 mW/cm^2 at a fluence of 1×10^{16} n_{eq}/cm^2. After such a fluence, modules based on sensors of both relevant geometries could reach 97% hit efficiency in the beam test within 100 V voltage range, which fits very well the ITk requirements. An irradiation campaign aimed at reaching the maximum fluence expected for the ITk ($\sim1.7\times10^{16}$ n_{eq}/cm^2) and further beam tests of the irradiated modules are underway, some modules sent for the campaign are also reported here. In parallel, the pre-production phase has started, and FBK has successfully completed and delivered a batch of 50×50 1E sensors compatible with ITkPix ROC.

Chapter 7
Assembly and Characterization of 3D Triplet modules based on RD53A readout chip

As the sensor production is approaching its pre-production phase, it is also important to work on the actual module shapes to be mounted on Innermost Tracker (ITk). All pixel modules are bare modules, which are made up of a sensor and a readout chip coupled with bump bonds. A flexible PCB, called flex hybrid or flex, is put on top of the sensor. The readout chips and sensor of the module are connected to the off-detector electronics, such as the readout system or the bias voltage supply, through wire bonds to the flex. The wire bonds are enclosed for mechanical stability and corrosion resistance; see Fig. 7.1 for a design of the Hybrid module.

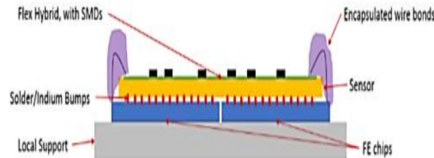


Fig. 7.1: A design of the proposed Hybrid Module showing different layers.

Triplets and quad chip modules house the 3D and planar modules, respectively. Three single bare modules are integrated into one module with one flex for the triplets. In the quad chip module, four readout chips are bump bonded to one big sensor. To make manufacturing easier, a single flex is employed in all barrel layers and endcaps for quad chip modules. Locally, the connection between the flex and the detector's support structure is tailored to the layout requirements [197].

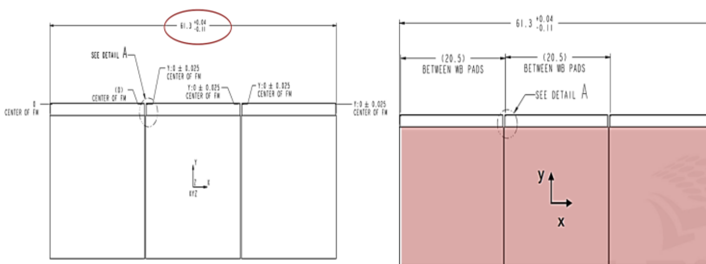
From the Final Design Review of November 2019, it was decided that the whole innermost layer (L0) will be made with 3D sensors. The Endcap part (ring part) will be made with 50 × 50 1E sensors, which will be jointly produced by FBK and SINTEF. To house these sensors, Ring Triplets will be made at the University of Genova, Italy. The Barrel part or the staves will be made with 25 × 100 1E sensors,

which will be produced by CNM. To house these sensors, Linear Triplets will be made by IFAE, Barcelona, Spain.

7.1 Dimensions

As there are two types of triplets, both of them have their own dimensions and design. Fig 7.2 depicts the design of a Linear triplet, where all the dimensions are in mm. The maximum length of a linear triplet can be 61.340 mm and the minimum can be 61.190 mm. To count the edge and position, there is a dot printed on the chip, which is called the Fiducial Mark (FM). The relative position of FM in the front-end chips along the Y-axis should be within ±25 µm. Inter module gap should be min 50 µm. The maximum displacement of the hybrid center concerning the triplet center in the x-axis should be ±35 µm. There are no specifications on the tolerance of the relative placement of the single modules, but it is important to align the PCB with the module. The alignment should be done considering:

- Wire-bondability
- Guarantees that module edge is visible
- It matters for the loading (that uses a module edge to locate the pickup areas)
- It matters for the services (it affects the position of the connectors with respect to the local support)



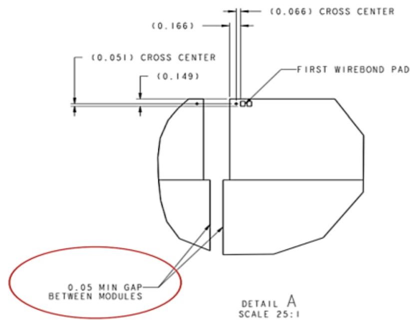


Fig 7.2: (Top) Schematics of Linear triplet with all the dimensions in mm. (Bottom) Detail A, which is the gap between two adjacent flex and module [198].

The sensor dimension is 19.5 mm, whereas PCB maximum dimension is 19.3 mm, which is 200 µm smaller. Wire-bonding pads on PCB are 1 mm away from the edge. The maximum displacement of PCB concerning the nominal position in the Y-axis should be ±50 µm. Modules can be displaced concerning each other by ±25 µm in the Y-axis. The maximum displacement between chip and PCB pad should be ±75 µm corresponding to a maximum rotation of 0.14 degrees. Planarity is currently defined concerning the backside of chip A (datum), as can be seen in Fig. 7.3. All points in the backside of the other two chips are within two planes parallel to surface A, displaced by 25um.

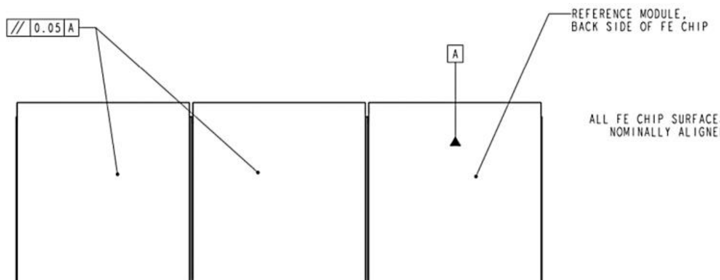


Fig. 7.3: Planarity of a Linear Triplet [198].

Ring triplets are a little bit different, as they have angular displacement, as can be seen in Fig. 7.4. The total displacement for a ring triplet is 80 degrees, whereas the

edge modules have a displacement of 40 degrees from the central one. Relative placement concerning the fiducial marks in the central chip in the Y-axis should be ±35µm. Relative placement in the X-axis concerning the center of the central chip should be ±35µm. The hybrid dimension should be 200 µm smaller than the nominal edge of the sensors. The average distance in the Y-axis concerning nominal should be within ±50 µm, measuring from the first or last wire bonding pad. The maximum difference between the first and last pad of chip to PCB wire-bonding pads should be less than 50 µm corresponding to a maximum rotation of 0.16 degrees. The planarity is as same as linear triplets, where the datum is the central one. All points in the backside of the other two chips are within two planes parallel to the surface of the central one, displaced by 25um.

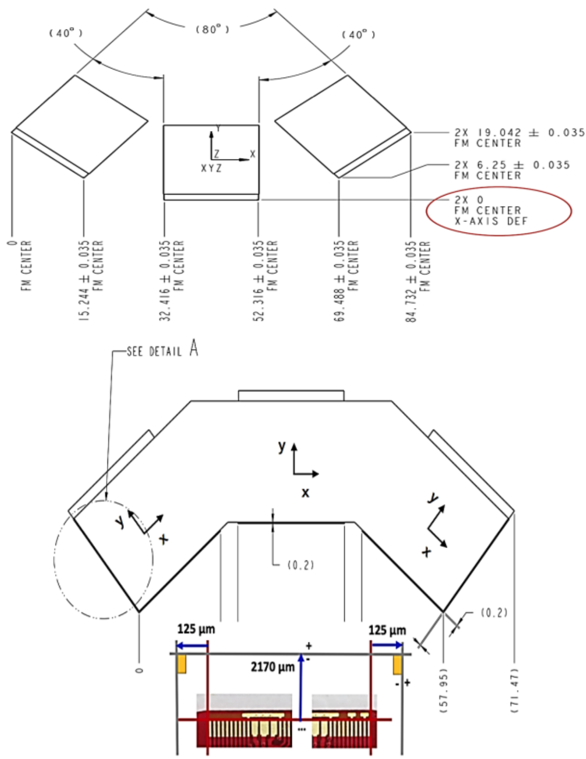


Fig. 7.4 Schematics of Ring Triplet with all dimensions in mm. [198].

7.2 Assembly

The assembly process of a triplet is quite complex and contains different steps and instruments. The whole process needs to be done with maximum care and safety. The setup must be done in a clean room with constant temperature, humidity, and particle count. An overview of the required steps can be obtained from Fig. 7.5.

Fig. 7.5: Different steps of the triplet assembly process.

The process starts with a visual inspection of the chips. The chips are sent from Bonn, Germany in gel packs. After unpacking, all the chips have to be checked using a microscope for any physical damage, especially on the edges, as can be seen in Fig. 7.6. Also, measurements are taken of the chips to match with requirements, which have been already discussed in the previous segment.

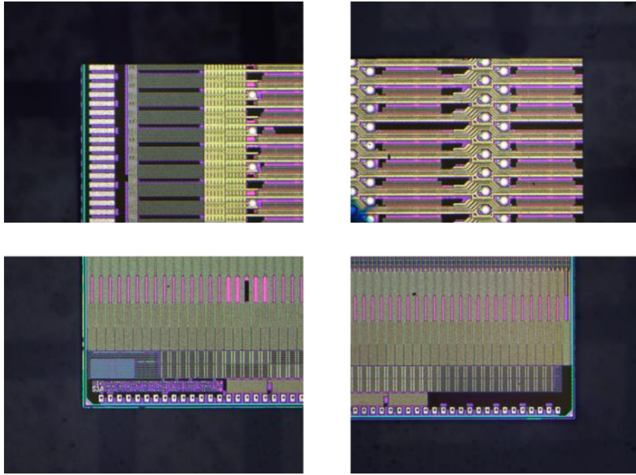


Fig. 7.6: Edge inspection of an RD53A chip. The edges look good and are accepted for assembly.

The next thing is to measure the weight of the flex. Measuring weight in every step of assembly is crucial due to measuring the amount of glue. The expected amount of glue is around 7 to 8 milligrams for each flex or chip. If the amount of glue is less, the shear strength between flex and chip will be lower than expected. If the amount of glue is more, excess glue will cover bump pads. An example of how the glue is measured can be realized in table 7.1.

Table 7.1: Measurement of glue on third flex of linear triplet L1. All the weights are on gram.

ONLY FLEX WEIGHT	AVERAGE FLEX WEIGHT	FLEX+ ONE CHIP	AVERAGE	FLEX+ ONE GLUE WEIGHT	AVERAGE	AMOUNT OF GLUE ON THIRD CHIP	FLEX+ONE CHIP+ONE GLUE	AVERAGE	AMOUNT OF GLUE ON THIRD CHIP AFTER DRYING
6.5733	6.57318	7.355	7.35526667	6.5808	6.5807	0.00752	7.3627	7.3625	0.0075
6.5735		7.3554		6.5806			7.3622		
6.5734		7.3554		6.5807			7.3626		
6.5729									
6.5728									

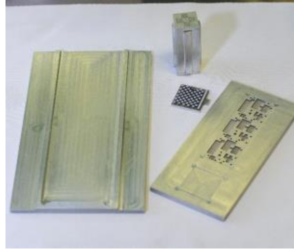


Fig 7.7: Glue stencil, glue stamp, and flex vacuum chuck used for linear triplet assembly in IFAE, Barcelona.

A special kind of glue is used for the triplet assembly, Araldite 2011, which has two components, resin, and hardener. The two components are mixed on the surface of the glue stencil and spread evenly with spatula (Fig. 7.7). The spatula that is being used in IFAE, Barcelona, has four different height segments, 150, 200, 250, and 350 µm. For a desired amount of glue, 250 µm height segment is appropriate, as seen after different trials. A glue stamp also has been designed to glue evenly and effectively the flex as seen in Fig. 7.7. The last component seen in Fig. 7.7 is the flex and chip vacuum chuck. This chuck is specially grooved to house all the electronics on flex, and also to house the chip on one side.

A very important component of the assembly process is a pick and place machine. The one being used in IFAE, Barcelona is a manual one with a three-axis camera to be able to align every object in each step. It has a vacuum bed where the glue stencil and flex stencil are positioned, and the glue stamp is attached to the pickup limb.

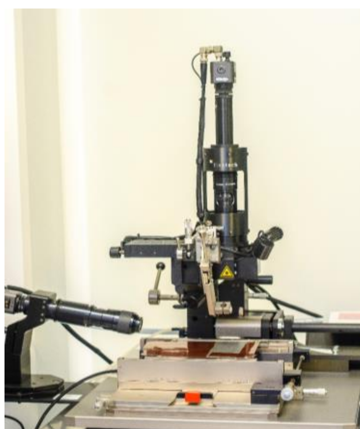


Fig. 7.8: Pick and place machine for linear triplet assembly in IFAE, Barcelona.

The surface of the flex is not planar, also it has a lot of asymmetric electronics on it. So, stamping its back planarly with glue is tricky. In order to be symmetric on all the flexes, the height of the pickup tool has to be adjusted in each step. With different trial and error, a workable measurement was found for the linear triplets as listed in Table 7.2.

The vacuum bed is set to have a 300 mmHg pressure after placing the components on it. At first, a stamp is dipped in the glue and stamped a flex. After that, the flex is weighted. Then a chip is picked and aligned with the flex, and then placed on it, kept on it for the glue to dry, with 7 N weight on top for at least 7 hours, with a vacuum pressure of 80 mmHg. After this period, the flex is weighted again and inspected for any excess glue and bad alignment. If everything is perfect, the procedure is continued in the same way for the other two chips and flex.

Table 7.2: Height setup

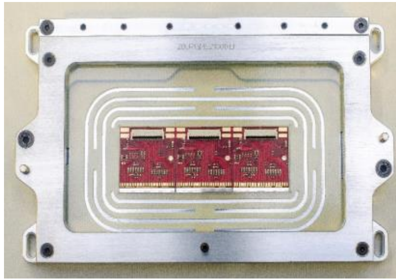
	SOAKING GLUE	**STAMPING GLUE**	**PICKING UP CHIP**	**PLACING CHIP**
OVERALL	8.05 mm		7 mm	
FLEX 1		8.90 mm		7.05 mm
FLEX 2		9.05 mm		7.45 mm
FLEX 3		9.50 mm		7.60 mm

After gluing, the triplet is secured inside the triplet carrier, and placed with vacuum on in the wire bonding machine as can be seen in Fig. 7.9. The configuration file for wire bonding has to be modified depending on the chip numbers for the three chips, as per the design of the RoC wire bonding scheme has been defined, as for chip id 1, only pad no 52 should be wire bonded. For chip id 2, only pad 53 should be bonded. For chip id 3, both pads 52 and 53 should be connected.

The next step is to perform a pull test on the three designated pull wire bonds on every chip. For that triplet is placed on a pull-up machine keeping on the carrier (Fig. 7.10). Usually, the pull-up strength should be around 9 grams. Then the triplet has to be bit trimmed. The trimming information is provided by chip fabricators and can be read from ITk Production Database. Pull-up resistors have to be soldered depending on chip VDDA at bit 16 value, read from the production database. The values are given in Table 7.3.

Table 7.3: Conditions for Pull-up resistor and value.

MEASURED STARTUP VDDA [V]	PULL-UP RESISTOR REQUIRED?	PULL-UP RESISTOR VALUE [KΩ]	THE EXPECTED INCREASE IN START-UP VDDA [V]
≤1.09	Yes	150	0.1
>1.09, AND≤1.14	Yes	300	0.05
>1.14	No	N/A	N/A



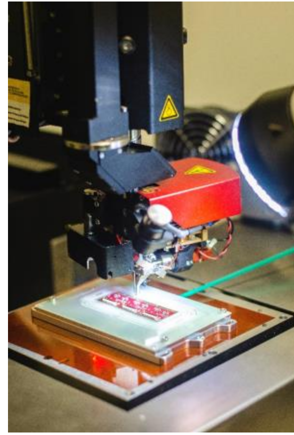


Fig. 7.9: (Left) triplet on the carrier after gluing, (right) wire bonding of the triplet keeping on the carrier.

Fig. 7.10: Pull test on triplet keeping it on the carrier.

7.3 Quality Control and Quality Assurance Setup

In a production lineup, a very important part is to ensure the quality of the production, which can be assured by quality control and quality assurance setup. A strong and organized QC/QA step can improve the production quality to the maximum extent. Like every production setup, Triplet production also has proposed a strong QC/QA process, as can be seen in Fig. 7.11.

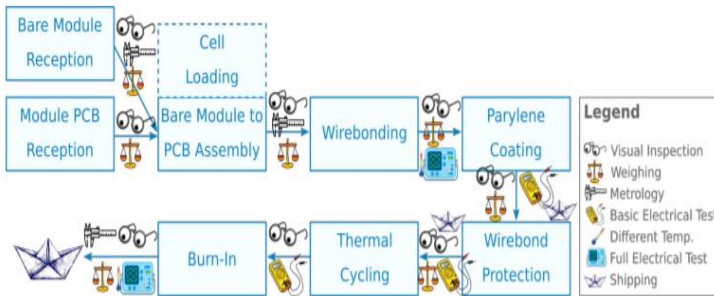


Fig. 7.11: QC/QA process of Triplet production.

As Italy is going to work as a cluster to do the full process, works are divided within the institutes. The University of Genova is going to Receive modules and PCB, assemble ring triplets, wire-bond them, coat them with perylene, and protect wire bonds. Then they will pass the triplet to the University of Bologna where they will do the thermal cycling. After successful thermal cycling from -55^{0}C to +60^{0}C, triplets will be sent to the University of Trento for the Burn-In test.

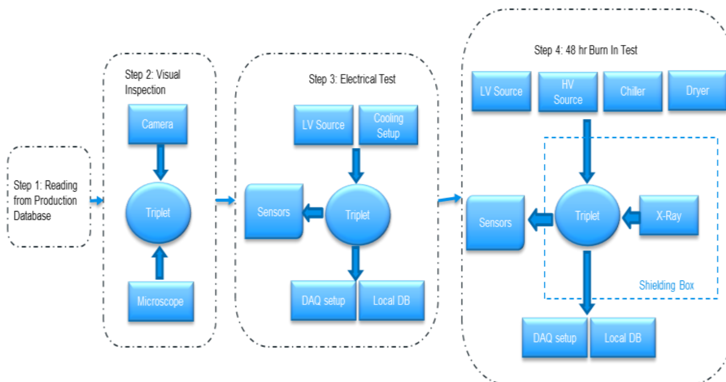


Fig. 7.12: QC/QA process in the University of Trento for Ring Triplets.

Fig 7.12 shows the QC/QA process steps taken at the University of Trento. It starts after receiving a Ring triplet, it also has to be received in the ITk production database. After receiving in production DB, it is possible to read production parameters and previous test results from there, which is useful to understand the condition of the triplet.

7.3.1 Visual Inspection of the Triplet

After unpacking the triplet, the first thing to do is a visual inspection. The Triplet should be carefully checked for any physical damages. To keep a record, and upload it in the production DB, a high-resolution picture has to be taken of the full module. The constraint of the picture is that it has to be fully in focus and all details, but the picture size should be within 30 Mb. To do so, at the University of Trento, a Nikon D7000 camera is used with a 50 mm prime lens. For lighting, a Youngonu TTL flash is used. The camera is mounted on a copy stand as can be seen in Fig. 7.13 (left). The camera was set as ISO 200, f stop 8, and shutter time 1/60. The distance from the stand to the camera was set to 45 cm.

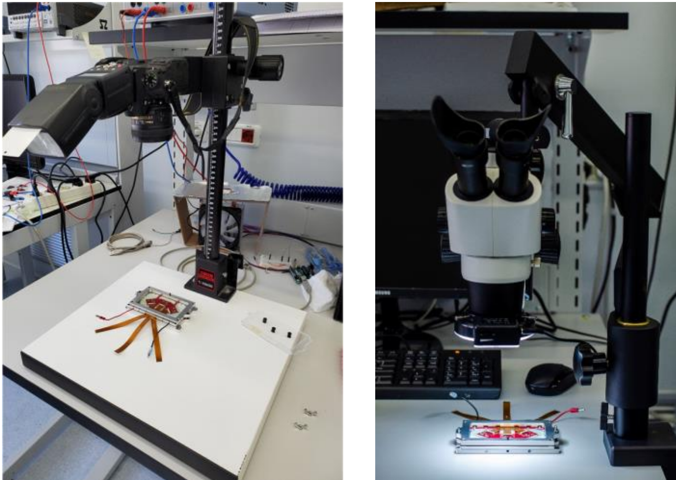


Fig. 7.13: (Left) Camera setup to take picture of the whole triplet. (Right) Microscope was set up to take pictures of the wire bonds.

The wire bonds should be checked very carefully in the triplets. To do so, a Motic SMZ-171 microscope with a camera mounted is used. With the help of this, all the wire bonds are inspected, as well as pictures are taken to upload to production DB.

7.3.2 Electrical Test

After every step in the QA/QC process, an electrical test is necessary to check whether the triplet is functioning well or not. The goal is to turn on the triplet with a low voltage power supply and read from it with the help of a DAQ setup. The process is almost the same as a single chip card, with some modifications for the triplet. The DAQ setup is the same as a single-chip card. An appropriate firmware should be downloaded using *flash.sh* script and flashed to the FPGA using Vivado Lab. As in this case a trenz card was used, and the firmware that was used was:

rd53_ohio_4x4_640Mbps_tef1001_R2.bit

In the controller file, or the *specCfg* file, two parameters have to be modified:

"rxPolarity" : 65535,

"txPolarity" : 15,

This defines that the polarity of chip identification in a triplet is in reverse order. In the chip configuration file, some parameters have to be changed:

"CdrSelSerClk": 1; to match with firmware clock speed, 640 MHz

"ChipId": 1; ID of each chip has to be changed, by default it is set to 0

"Name": "20UPGFC0029031"; name of the chip as given in production DB

Three DP to mini-DP cables attached to the A, B, and C ports of ohio card are connected with chips 1, 2, and 3 correspondingly via connector boards designed for triplets. As a low voltage power source, an HMP 4040 four-channel power source was used. The operation was set to the constant current mode, with the limits of 1.9 V for the whole triplet and 1.1 A per chip. A cooling setup was designed to restrict temperature increase in triplet during initial electrical tests, consisting of a cooling fan and a Peltier on top of it. The whole setup can be realized in Fig. 7.14. To monitor the temperature of the chips of the triplet by reading NTC connected with the chips, a canary board was used. The Canary board is a custom-made board from the ITk community to measure the temperature from NTC, room temperature, humidity, and dust particle inside the room. The board is based on the ESP32 microcontroller. To measure room temperature and humidity, the canary board and also a Sensirion module were used.

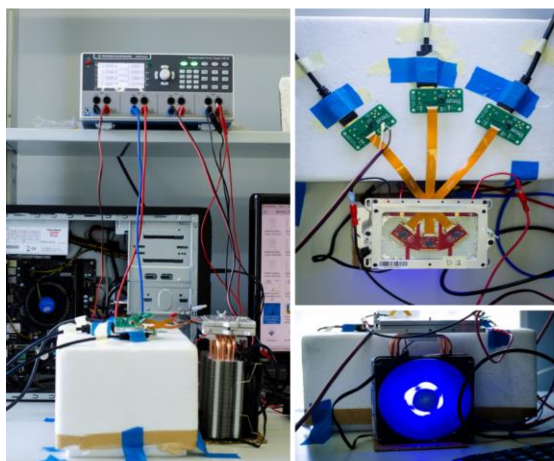


Fig. 7.14: (Left) Electrical test setup for triplet. (Right up) connections to the triplet and (right bottom) cooling system.

7.3.3. Cold Test

The cold test has the following requirements set by the testing community:

- Ability to SLD0 startup at -35⁰C
- Digital scan, analog scan, and threshold scan at the temperatures as specified on the testing document (-25°C), to qualify for the cooling ability and temperature stability.
- Environmental monitoring throughout the operation
- Keep the triplet running for 48 hrs on -25⁰C and monitor the performance
- Readiness for source scan

To cool down the triplet to -35⁰C, a cooling setup has been established. Julabo corio cd-100F cooler has been purchased to supply the cold fluid. With the help of silicon-based bath fluid, this cooler can cool down to -45⁰C. As the bath fluid is silicon-based, a Polytetrafluoroethylene (PTFE) type pipe is used to provide the cold fluid to the cold plate. Considering thermal loss, a Peltier is also connected on top of the cold plate. The cold plate is connected with a vacuum chuck, which holds the triplet. The cold plate, vacuum chuck, and triplet are kept inside a cold box, made out of thermally treated foam, suitable for a cleanroom environment. The chiller is very stable under operating conditions and can fluctuate within ±0.5⁰C when cooling

down to a new temperature. The peltiers can fluctuate within ±1^{0}C. As a whole, in a stable operating condition, the whole system can fluctuate within ±1^{0}C.

Fig. 7.15: (Left) Julabo corio cd-100F cooler, (right) Custom-made cold box.

As the operating temperature for this phase is very low, it essential to keep the dew point on the module atmosphere well below the operational temperature. A Kaeser DC2.0 dryer unit (Fig. 7.16 right) has been used to supply dry air to the triplet and cold box. This unit can supply dry air maintaining a dew point of -70^{0}C (Fig. 7.16 left-up). A flow meter has been added to measure the amount of dry air flushed to the cold box (Fig. 7.16 left-bottom). During the cool down, the average flow of dry air is set to 5 L/min. But when the temperature and humidity become stable, the flow is reduced to 1 L/min.

Fig. 7.16: (Right) Kaeser DC2.0 dryer unit, (left-up) dewpoint set to -70^{0}C, (left-bottom) flow meter.

For the source scan, an X-ray gun, Amptek Mini-X2 was used. The x-ray gun is mounted inside a shielding box, shielded by lead. The box has two curved holes to supply wires and tubes inside as can be seen in Fig. 7.17. The box has a full interlock system for safety. Doors of the box are coupled with magnetic switches, to interrupt the x-ray gun if the door is opened. Also, indication lights are mounted on top of the box to understand the operation state of the box. The x-ray gun was operated with 50kV voltage and 80 µA current (4W power). 250µm Aluminium filter has been used to suppress low-energy photons. The gun is mounted on a fixed mount temporally, but it will be mounted on an automatic XYZ movement system later on.

Fig. 7.17: Mini-X2 x-ray gun inside shielding box showing a source scan setup for a single-chip card.

7.4 Triplet Reception Test

7.4.1 Triplet D1

Triplet D1 is a digital ring triplet, where 'Digital' means it has only readout chips, without any sensor. This was assembled at INFN Genoa in the first batch of assembly and then was sent to Trento for qualification. Upon receiving, a visual inspection was done as seen in Fig. 7.18. There was no physical damage in the module. Only chip1 was found to be connected to the power grid. Wire bonds were checked with the microscope, everything was perfect.

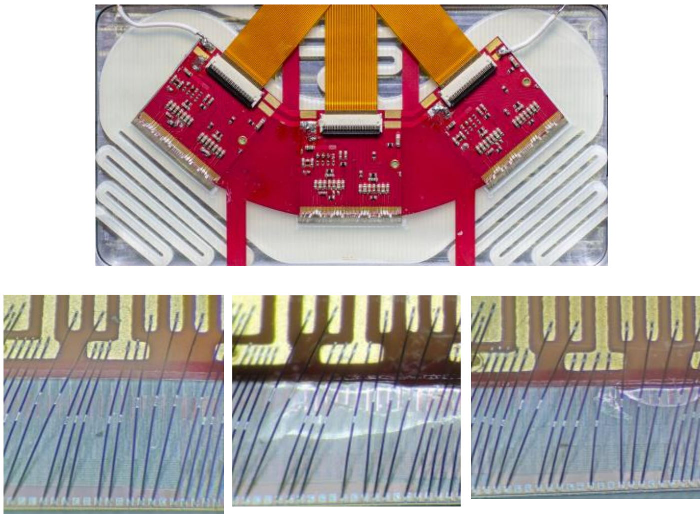
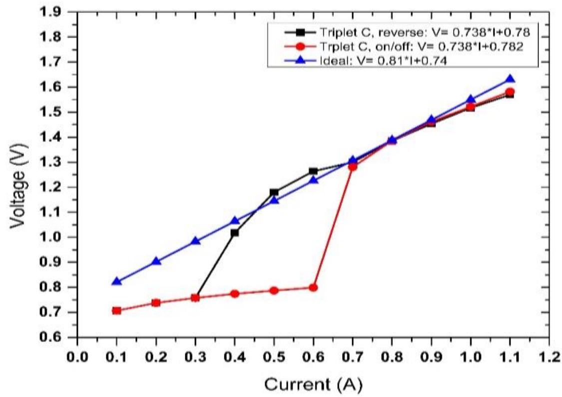


Fig 7.18: (Top) Visual inspection picture of digital triplet D1, (bottom) Microscopic wire-bond inspection pictures.

A VI characterization was made in two ways; firstly, the chip was biased with 1.9 V and 1.1 A current in constant current (CC) mode. Then the current was reduced with the step size of 0.1 A. Secondly, the chip was biased with 1.9 V and 0.1 A current in cc-mode. Then the current was increased with the steps of 0.1 A while switching the chip ON and OFF at every step. Both the curves were also compared with an ideal curve for the digital triplets. The characteristics matched on turned-on phase with different turn-on voltage. After an appropriate VI was obtained, communication and scanning were started. All the tests were done while monitoring the temperature by connecting the NTC of the chip to a microcontroller. The temperature rose to ~27^{0}C maximum during the operation, as can be seen in Fig. 7.19 (bottom).



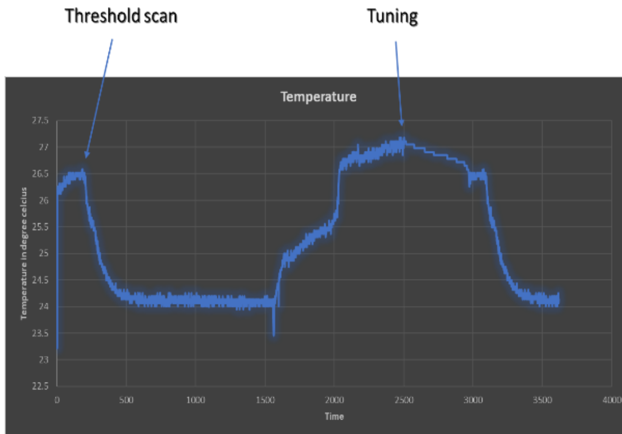


Fig. 7.19: (Top) VI characteristics curve of D1, where the sudden current rise at 0.6 A for the red line shows the FEs are switching ON at that voltage, and for the black, it is a little bit deviated because of residual effect, (bottom) temperature log read from NTC of the chip during the test time.

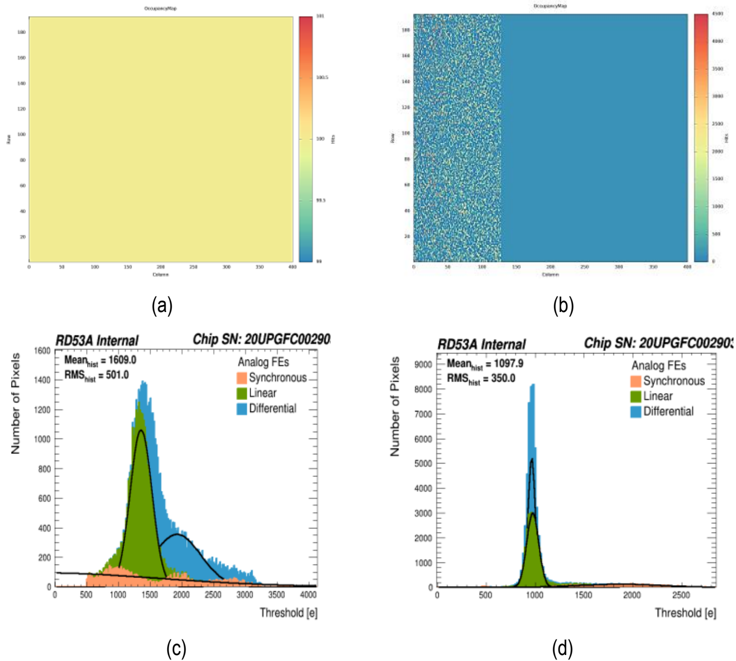


Fig. 7.20: Scan results from digital triplet D1, (a) digital scan, (b) analog scan, (c) threshold scan before tuning, and (d) threshold scan after tuning.

First, a digital scan was done to establish communication. After a successful communication, trimming was done to match VDDA and VDDD to 1.2V, with a good digital and analog scan. Fig. 7.20 (a) shows a good digital scan with 100% occupancy, whereas, in the analog scan (Fig. 7.20 (b)), the synchronous FE had a lot of unresponsiveness. A threshold scan was done before tuning (Fig. 7.20 (c)) and then a tune routine was started to tune the FEs to 1000 electrons threshold and 10000 electrons @ 8BC ToT. The synchronous FE was turned off as it was not responding, but the other two FEs were tuned perfectly (Fig. 7.20 (d)).

7.4.2 Triplet D3

Triplet D3 is also a digital type ring triplet, assembled in INFN Genoa in the first batch of assembly. It was sent to IFAE, Barcelona for qualification, and then was sent to the University of Trento, Italy for further tests. Upon receiving, a visual

inspection was done as seen in Fig. 7.21. There was no physical damage in the module. Wire bonds were checked with the microscope, everything was perfect.

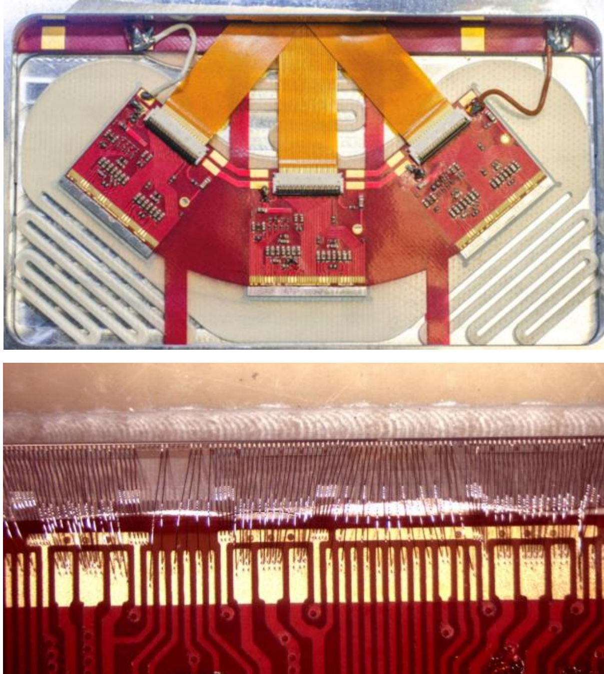


Fig. 7.21: (Top) Visual inspection picture of digital triplet D3, (bottom) Microscopic wire-bond inspection picture.

A VI characterization was made, and the chip was biased with 1.9 V and 0.1 A current in cc-mode. Then the current was increased with the step size of 0.1 A while switching the chip ON and OFF at every step. The characteristics were matched with the expected behavior, where the FEs switch ON with rapid ramp-up at 1.8 A and 2.6 A (Fig. 7.22, left). After an appropriate VI was obtained, communication and scanning were started. All the tests were done while monitoring the temperature by connecting the NTC of the chip to a microcontroller. The temperature rose to 20^{0}C maximum during the operation, as can be seen in Fig. 7.22 (right).

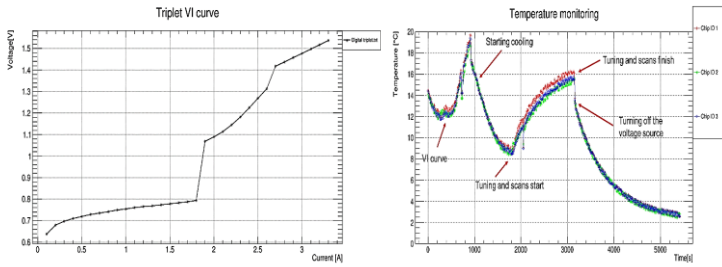
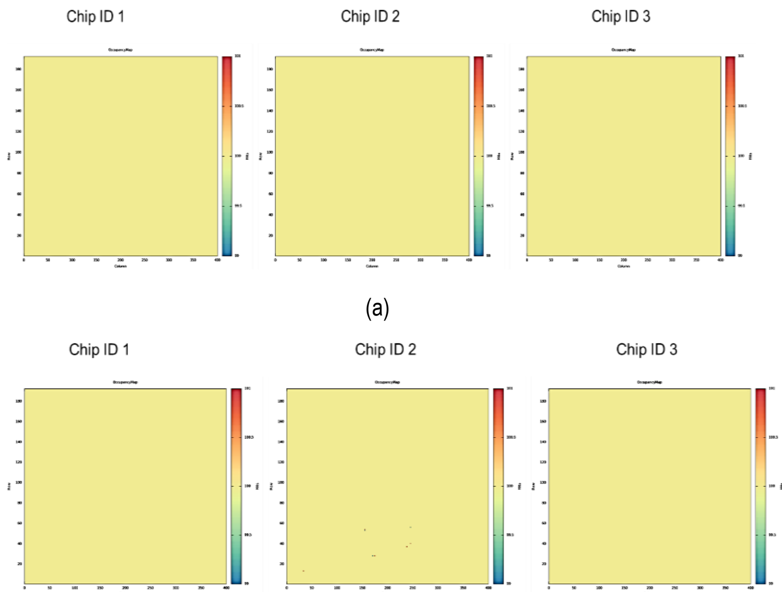


Fig. 7.22: (Left) VI characteristics curve of D3 where the FEs switches ON at 1.8 A and 2.6 A, (right) temperature log read from NTC of the chip during the entire test time with the rise during operation and down of temperature during switching OFF time.

First, a digital scan was done to establish communication. After a successful communication, trimming was done to match VDDA and VDDD to 1.2V, with a good digital and analog scan. Fig. 7.23 (a) shows a good digital scan with 100% occupancy, as well as the analog scan (Fig. 7.23 (b)). A threshold scan was done before tuning (Fig. 7.23 (c)) and then a tune routine was started to tune the FEs to 1000 electrons threshold and 10000 electrons @ 8BC ToT. Only in chip 2, the synchronous FE didn't tune well, even after multiple trials (Fig. 7.23 (d)).



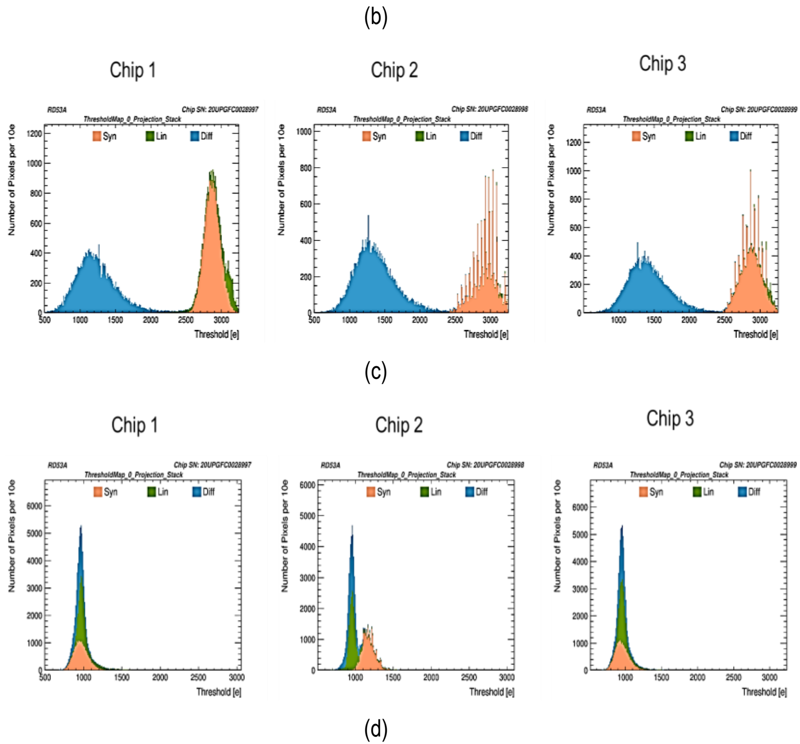


Fig. 7.23: Scan results from digital triplet D3, (a) digital scan, (b) analog scan, (c) threshold scan before tuning, and (d) threshold scan after tuning.

7.4.3 Triplet L1

Triplet L1 is the first linear-type digital triplet, assembled in IFAE, Barcelona. After assembly, it was tested in the same facility. Following the routine, a visual inspection was done as seen in Fig. 7.24. There was no physical damage in the module. Wire bonds were checked with the microscope, everything was perfect.

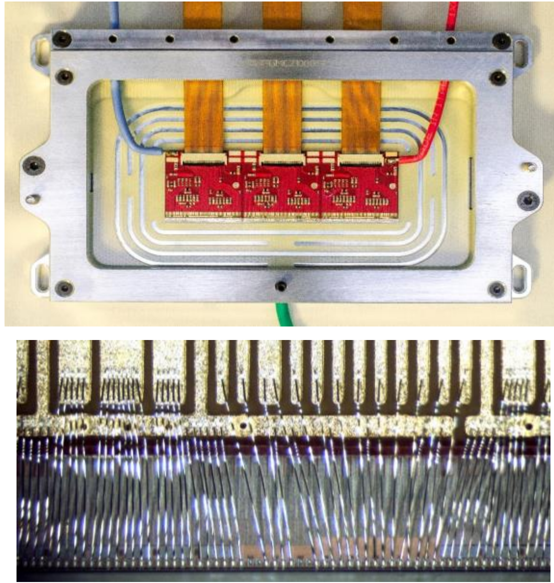


Fig. 7.24: (Top) Visual inspection picture of digital triplet D3, (bottom) Microscopic wire-bond inspection picture.

A VI characterization was made, and the chip was biased with 1.9 V and 0.1 A current in cc-mode. Then the current was increased with the step size of 0.1 A while switching the chip ON and OFF at every step. The characteristics were matched with the expected behavior where FEs switch ON with sudden ramp at 1.4 A and 1.8 A (Fig. 7.25). After an appropriate VI was obtained, communication and scanning were started.

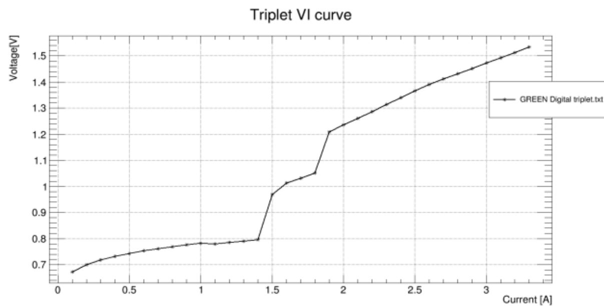
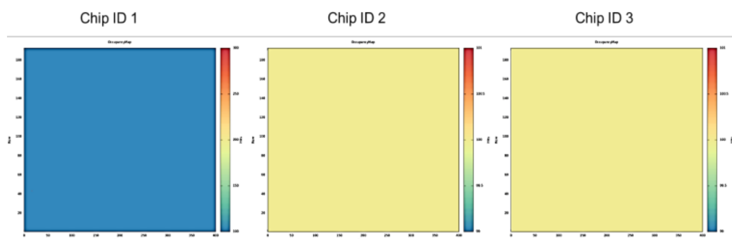
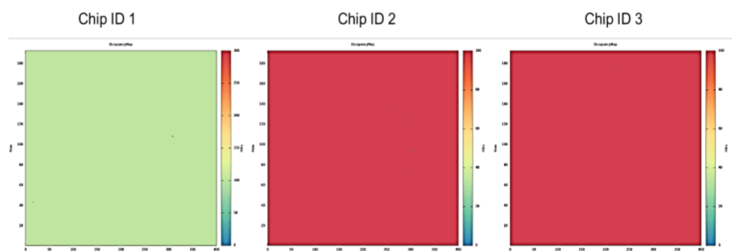


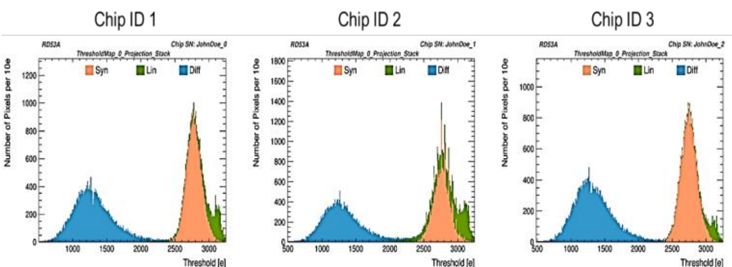
Fig. 7.25: VI characteristics curve of L1.



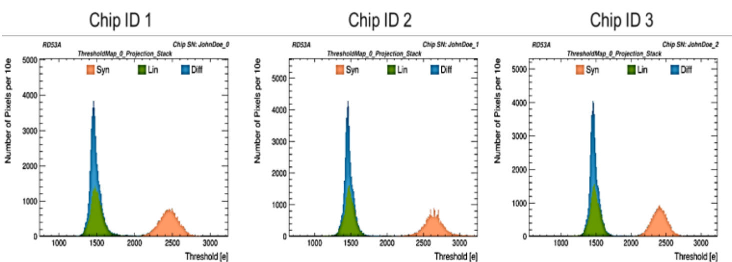
(a)



(b)



(c)



(d)

Fig. 7.26: Scan results from digital triplet D3, (a) digital scan, (b) analog scan, (c) threshold scan before tuning, and (d) threshold scan after tuning.

First, a digital scan was done to establish communication. After a successful communication, trimming was done to match VDDA and VDDD to 1.2V, with a good digital and analog scan. Fig. 7.26 (a) shows a good digital scan with 100% occupancy, with one pixel in chip 1 not responding as well as the analog scan, and some pixels not responding in chip 2 (Fig. 7.26 (b)). A threshold scan was done before tuning (Fig. 7.26 (c)) and then a tune routine was started to tune the differential and linear FEs to 1500 electrons threshold, whereas the synchronous FE to 2500 electrons and 10000 electrons @ 8BC ToT. In chips 2 and 3, the synchronous FE showed a little shift in tuning, even after multiple trials (Fig. 7.26 (d)).

7.4.4 Triplet L2

Triplet L2 is the second linear-type digital triplet, assembled in IFAE, Barcelona. After assembly, it was tested in the same facility. Following the routine, a visual inspection was done as seen in Fig. 7.27. There was no physical damage in the module. Wire bonds were checked with the microscope, everything was perfect.

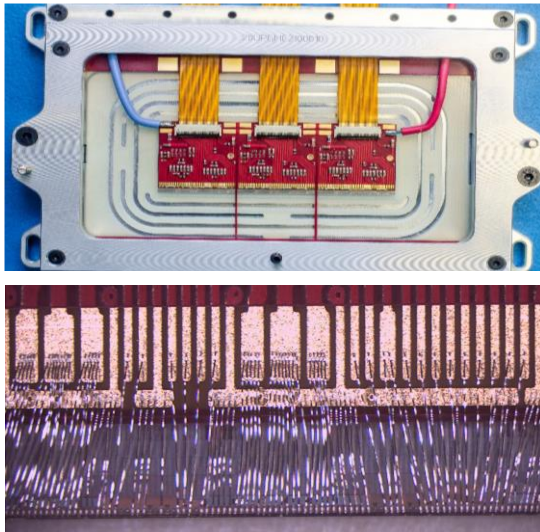


Fig. 7.27: (Top) Visual inspection picture of digital triplet D3, (bottom) Microscopic wire-bond inspection picture.

A VI characterization was made, and the chip was biased with 1.9 V and 0.1 A current in cc-mode. Then the current was increased with the step size of 0.1 A while switching the chip ON and OFF at every step. The characteristics were matched with the expected behavior where the FEs switched ON at 1.5 A and 2.2 A (Fig. 7.28). After an appropriate VI was obtained, communication and scanning were started.

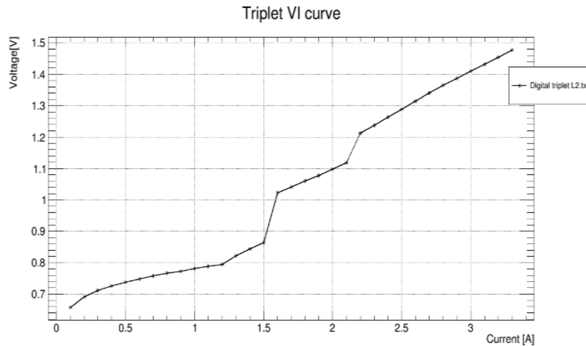
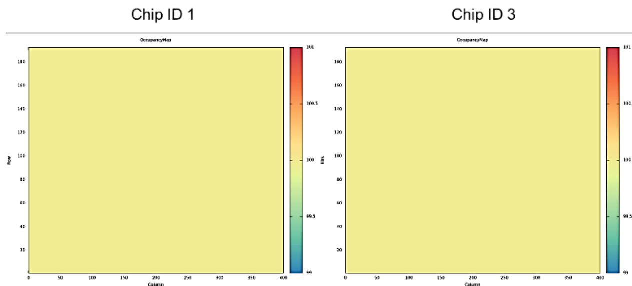
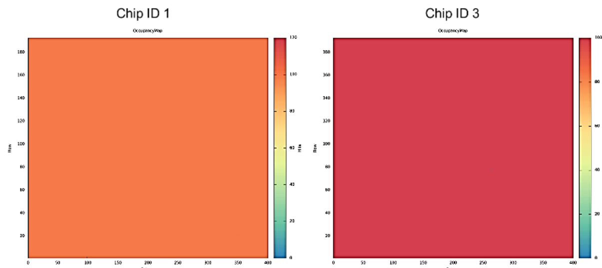


Fig. 7.28: VI characteristics curve of L2.

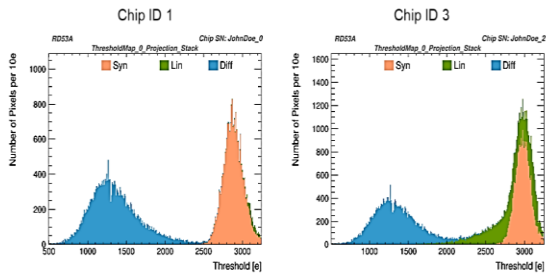
First, a digital scan was done to establish communication. It was observed that chip 2 was not communicating. So trimming was done for chips 1 and 2 to match VDDA and VDDD to 1.2V, with a good digital and analog scan. Fig. 7.29 (a) shows a good digital scan with 100% occupancy, as well as the analog scan (Fig. 7.29 (b)). A threshold scan was done before tuning (Fig. 7.29 (c)) and then a tune routine was started to tune the FEs to 1500 electrons threshold, and 10000 electrons @ 8BC ToT. All the FEs were tuned perfectly (Fig. 7.29 (d)).



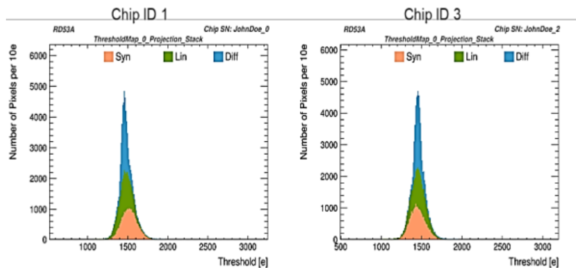
(a)



(b)



(c)



(d)

Fig. 7.29: Scan results from digital triplet D3, (a) digital scan, (b) analog scan, (c) threshold scan before tuning, and (d) threshold scan after tuning.

7.5 Triplet Cold Test

7.5.1 Digital Triplet D3

Digital triplet D3, after the reception test, was tested at the cold temperature. It was crucial, to test the cold setup in Trento, and to qualify for the phase 2 QA/QC test. To perform the test, the triplet was placed on the cold chuck inside the cold box, with a

vacuum on to have good thermal conduction. The thermal chuck was placed on top of two Peltier's, which were connected with a cold plate. The cold plate gets a continuous flow of thermal bath fluid from the chiller. The cold box was placed inside the x-ray cabinet, as can be seen in Fig. 7.30.

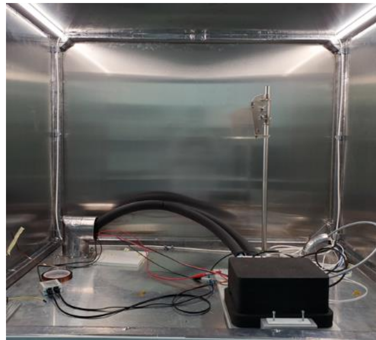


Fig. 7.30: Setup for the cold test of triplets in Trento showing cold box, chiller pipe and wire inlets inside sheilding box.

To measure the temperature and humidity at different levels, sensirion sensors were placed in both cold plate and vacuum chuck. The temperature was also read from chip NTCs of the Triplet. At first, the triplet was cooled down to -35^{0}C, after stabling down, it was switched ON to see whether all the chips communicate it or not. After that, keeping the triplet ON, the temperature was stabilized to -25^{0}C to do further tests, as seen in Fig. 7.31.

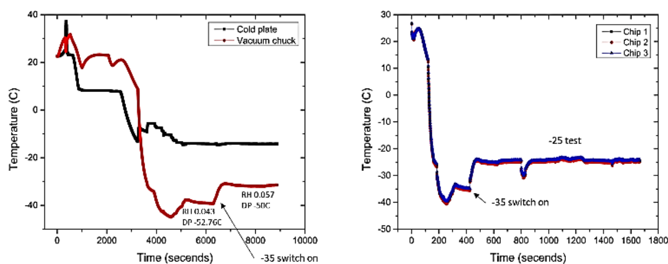


Fig. 7.31: (Left) Temperature log during the cold test, read from sensirion sensors, and (right) temperature log read from 3 NTCs of the three chips of the triplet.

At -35^{0}C temperature, the triplet was powered up with 2V and 4.5 A current, as prescribed from ITk specifications. After switching ON, a digital scan was done to see whether they communicate or not. In this case, all three chips communicated well (Fig. 7.32), otherwise, YARR could not have made any occupancy map, and there would error report. Also, the occupancy is zero all over the map, as it should be.

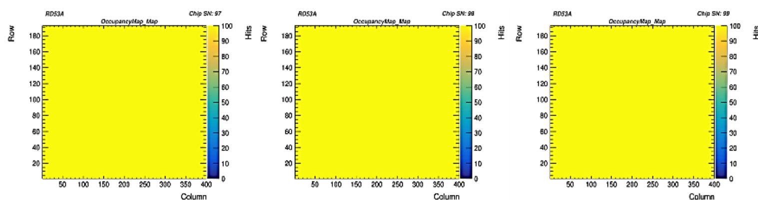


Fig. 7.32: Digital scan results from all the three chips of triplet D3 at -35^{0}C.

At -25^{0}C, the triplet was tuned for cold temperature configuration, differential and linear FE with 1500 electrons, and synchronous FE with 2500 electrons. Differential FE of all the three was tuned with a narrow gaussian profile, having a pick of slightly less than 1500 electrons (Fig. 7.33 (a)). The linear FE showed the second pick of around 1100 electrons (red marked in Fig 7.33(b)), which seems to be a chip property, as it was seen in other sites (Fig. 7.33 (b)). The synchronous FE was tuned with a relatively thicker Gaussian profile (Fig. 7.33(c)).

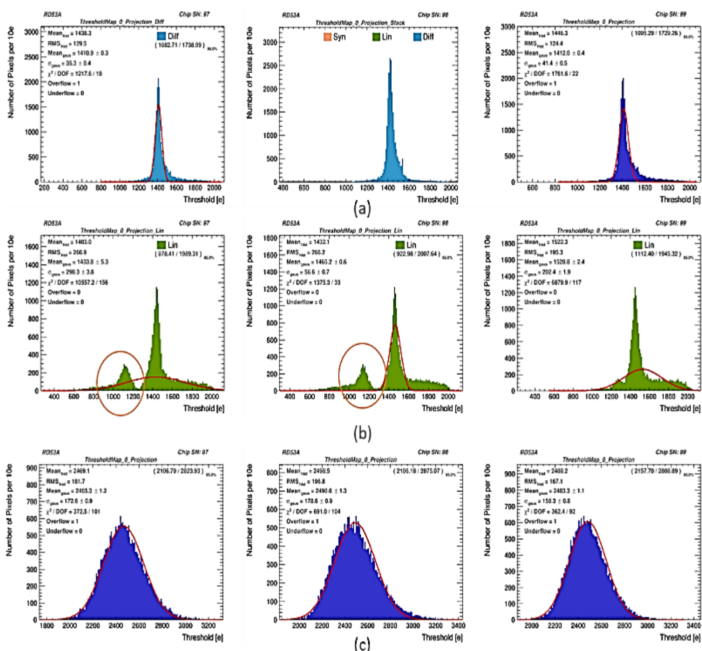


Fig. 7.33: (a) Differential, (b) Liner with a red marking at the second pick, and (c) Synchronous FE threshold scan results of all three chips of triplet D3.

A reduced burn-in test for 8 hours was done triplet D3 at -25⁰C. The goal was to show the possibility of maintaining the temperature and humidity stable during the entire operation time (Fig. 7.34 (left)), engaging the triplet with a continuous noise scan. As this triplet didn't have any sensors on it, and the chip noise was masked during the tuning operation, the noise scan was empty after the burn-in test, as seen in Fig. 7.34 (right).

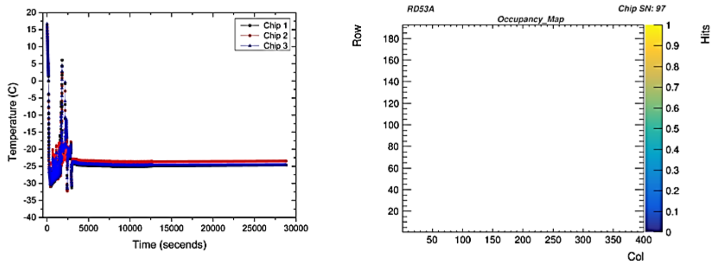


Fig. 7.34: (Left) Temperature log during 8 hours of bur in test, and (right) empty noise scan result due to not having any sensor.

7.5.2 Triplet R4

Triplet R4 was assembled in the first batch of real triplets, i.e. triplet with sensors. R4 was assembled with Rd53a RoC attached with a planar 50 × 50 μm^2 geometry sensor. Though triplets are intended to be with 3D sensors, these triplets were made with planar sensors due to availability at that time. This is the first triplet that underwent the cold test.

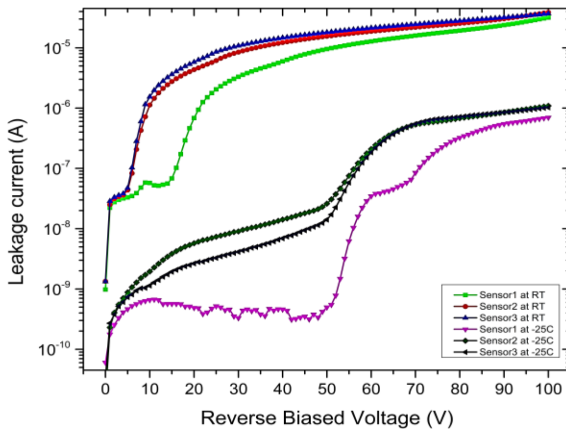


Fig. 7.35: IV characteristic curve of all three sensors of the triplet R4, both at room temperature and -25^{0}C, with lower leakage current at operating voltage (30 V) for cold temperature, and higher breakdown voltage at cold temperature.

Fig. 7.35 shows the IV characteristics curve of the triplet R4, both at room temperature and cold temperature. These are planar sensors, without guard ring. At room temperature, peripheral leakage ads to the sensor leakage current, and it starts to increase rapidly after 10 V reverse bias, where sensor 1 starts after 20 V. The leakage reduces to a very small value at -25^{0}C, as the thermionic generation freezes. The avalanche state also shifts to a higher voltage at cold temperatures, towards around 50 V. After this point, the current steps up rapidly, and bends towards saturation.

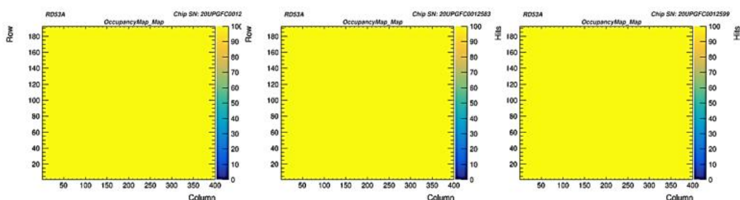


Fig. 7.36: Digital scan results from all the three chips of triplet R4 at -35^{0}C

As the first step, the triplet was cooled down to -35^{0}C, and then powered up. After switching ON, a digital scan was done, and all three chips communicated (Fig. 7.36). After that, the triplet was warmed up to -25^{0}C, trimmed to match VDDD and VDDA valued to 1.2 V, and tuned. The differential and linear FE was tuned to 1500 electrons and synchronous FE was tuned to 2500 electrons, keeping a bias value of -30V at the sensors. The tune results were as expected, as seen also before. The threshold pic a little bit shifts towards 1400 electron, and linear FE shows a second peak (Fig. 7.37).

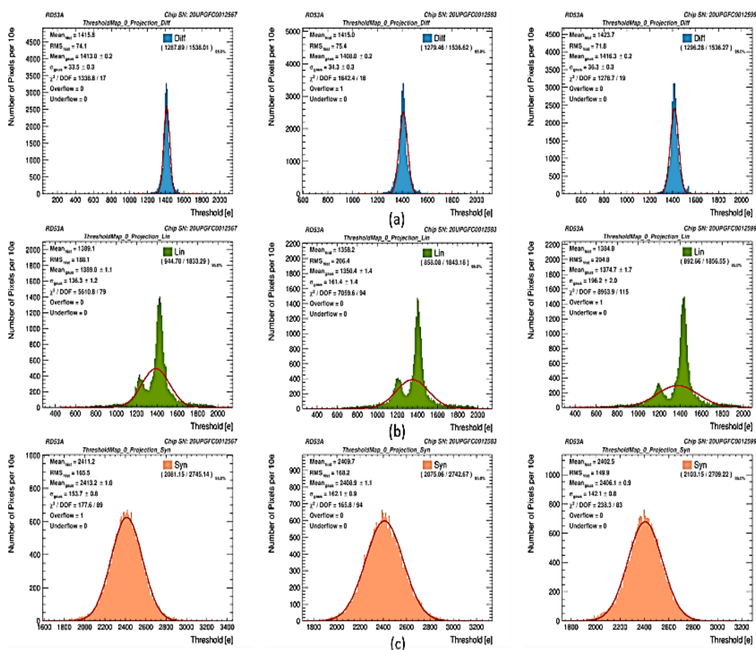


Fig. 7.37: (a) Differential, (b) Liner, and (c) Synchronous FE threshold scan results of all three chips of triplet R4.

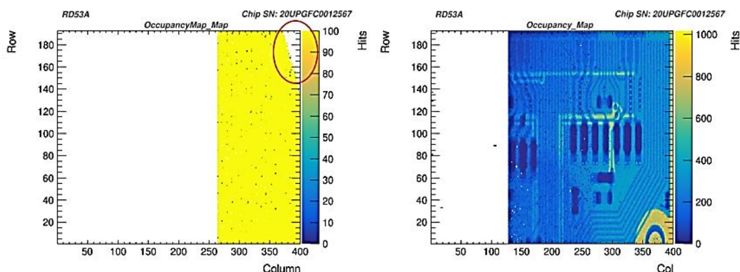


Fig. 7.38: (Left) Differential discbump scan of chip 1 with a red circle on bump disconnection, and (right) X-ray scan of the same chip.

Discbumpscan was done on all the chips, for all the FE individually. 'Discbumpscan' stands for disconnected bump scan. This scan compares the analog scan and crosstalk scan to check pixel response to estimate the bump connection. All of them showed expected results, other than the differential FE of chip 1. It showed a hint of

disconnection in bumps in the upper right corner (Fig 7.38 (left)). To understand this, a source scan was done with a mini X2 X-ray gun. The chip was configured for noise scan with 150 kHz for 60 seconds. But as seen in Fig. 7.38 (right), that corner sees hits like other parts of the sensor. It seems that the corner is not fully disconnected, but rather capacitively connected with the sensor.

7.6 Conclusion

Triplet module assembly is still an ongoing process. Up to this time, six RD53A ring triplets, with planar sensors have been assembled in Genova, among which, three were tested in Trento. ITkpixV1 is just has been made available for assembling actual 3D triplets, one triplet is under process. Phase 1 electrical tests of two ring triplets and two linear triplets have been reported here, with one digital triplet and one real triplet successful cold test.

Chapter 8
Conclusion

Research and development in Trento for 3D sensors aimed at the ATLAS Inner Tracker (ITk) at HL-LHC is an ongoing process. It started in 2014 and has a projection to finish by 2028 after installing and commissioning the final sensors and modules in ITk. This time frame has been slightly delayed because of the covid pandemic. However, despite this unavoidable situation, everyone is increasing efforts to speed up the process and accomplish the goal.

The most important conclusions of the work reported in this thesis are the following:

Section 5.9 has conclusive results of the third or stepper batch of FBK for 3D single-sided sensors. The yield for the crucial 25 × 100 2E geometry was significantly increased (approximately doubled) compared to the prior batch utilizing the mask aligner (batch 2), reaching almost 40% on average. The yields for the other non-critical geometries 50 × 50 1E and 25 × 100 1E, on the other hand, remained relatively constant, around 60% on average, which is acceptable given the complex fabrication technology of 3D sensors and the very high density of columnar electrodes involved in small-pitch designs. These findings show that a stepper may be used to make sophisticated small-pitch 3D sensors. Based on this result, FBK completed the R&D phase and processed the pre-production batch for the ITk, which is 10% of the whole production, using a stepper. These sensors are of 2cm × 2cm dimension to match the ITkPixV1 chip, which is the final RoC for ATLAS ITk. Also, another batch of small pitch 3D sensors was produced to match the CROC readout chip for the CMS detector. Tests are yet to be done to come up with new results.

Section 6.16 has conclusive results from the single-chip card module tests. Till now, results have been published after irradiating the SCCs up to $1×10^{16}$ n_{eq}/cm^2. The electrical characteristics have satisfied the requirements by having less power dissipation than the specification in maximum efficiency voltage. The hit efficiency was recorded to be 97%, which was also expected. Efforts are being made to improve the bump bonding scheme. Two SCCs from IFAE containing sensor geometries of 50 × 50 1E and 25 × 100 1E have been tested under an electron test beam of 5.2 GeV in DESY after irradiation up to a fluence of $1.6×10^{16}$ n_{eq}/cm^2. The

IV characteristics of both modules look satisfactory, with a smooth breakdown trend as can be seen in Fig. 8.1. Beam reconstruction is yet to be done, so as the come up with final results. Four more SCCs containing sensors of FBK from INFN Genoa and three more containing sensors of CNM from IFAE, Barcelona have been sent to Los Alamos for proton irradiation up to ~1.7×10^{16} n_{eq}/cm^2 fluence. After irradiation, they are planned to be tested at the next available test beam campaign.

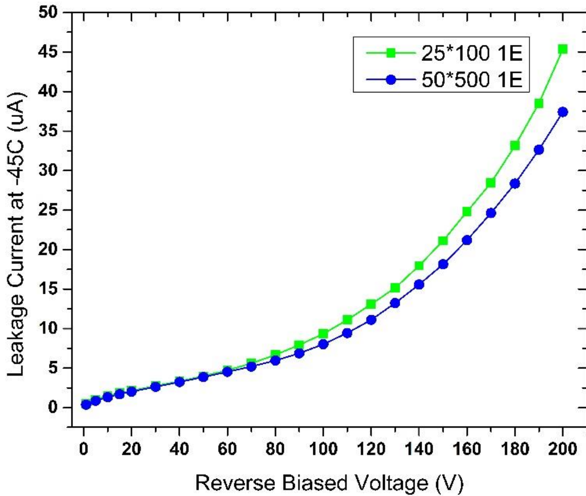


Fig. 8.1: IV characteristics of two Single-Chip cards after irradiating up to 1.6×10^{16} n_{eq}/cm^2 fluence tested at DESY test beam in December 2021, after cooling down with dry ice.

Section 7.5 has a conclusive discussion on the ongoing activities of Triplet modules. As Italian groups have agreed to work as a cluster, assembly and testing activities have been divided within institutions. In such a framework, INFN Genoa will assemble the ring triplets, with the sensors from FBK, do a preliminary electrical test and pass it to INFN Bologna. Thermal cycling will be done there and then modules will be passed to Trento. The final electrical characterization will be done here including a burn-in test and source test using an X-ray gun. Phase 1 electrical test setup has already been done. Two digital ring triplets have also been tested using that setup. Phase 2 qualification setup for burn-in test and cold test is also being

developed. The X-ray shielding box and setup have already been commissioned. Soon the real triplets will arrive, and the full testing will start. Also, the assembly process of linear triplets and testing of the first two linear triplets has been discussed in the thesis, as an outcome of the internship time at IFAE, Barcelona.

Appendix

Scans and Tuning

YARR system has its scan console with special syntaxes and different scans. It also has a prescribed tune routine to be followed to tune an RD53A chip [192]. The syntaxes to be used to do a scan can be described as:

- -r : Specifies the controller file in .json format
- -c : Specifies the connectivity file containing chip type, chip no, and path to the configuration file in .json format
- -s : Specifies the scan file
- -p : Enables the plotting option
- -W : Uploads the scan data to the Local Database
- -t : Sets the no of electrons to inject or to be tuned with
- -m : Sets a mask. With option setting to 1, it resets all masks.

Several scans are there in YARR software to understand the different characteristics of RD53A chip and sensor. Some of them can be listed as follows [193]:

Digital Scan: Shows the occupancy map and enable map of digital outputs. Can be initiated by the following command inside the YARR directory:

bin/scanConsole -r configs/controller/specCfg-rd53a.json -c configs/connectivity/example_rd53a_setup.json -s configs/scan/rd53a/std_digitalscan.json -p

Where, in connectivity, *example_rd53a_setup.json* should be changed by the connectivity file of the individual SCC.

Analog scan: Shows the occupancy map and enable map of analog outputs. Can be initiated by the following command inside the YARR directory:

bin/scanConsole -r configs/controller/specCfg-rd53a.json -c configs/connectivity/example_rd53a_setup.json -s configs/scan/rd53a/std_analogscan.json -p

Where, in connectivity, *example_rd53a_setup.json* should be changed by the connectivity file of the individual SCC.

Threshold scan: This scan gives an estimation of threshold distribution, S-curve, and noise distribution. Can be initiated by the following command:

bin/scanConsole -r configs/controller/specCfg-rd53a.json -c configs/connectivity/example_rd53a_setup.json -s configs/scan/rd53a/std_thresholdscan.json -p

ToT scan: This scan gives an estimation of the distribution of Time over Threshold and its mean value. Can be initiated by the following command:

bin/scanConsole -r configs/controller/specCfg-rd53a.json -c configs/connectivity/example_rd53a_setup.json -s configs/scan/rd53a/std_thresholdscan.json -t 10000 8 -p

Where 10000 is the target charge for ToT 8.

Cross-Talk scan: This scan provides an estimation of probable thresholds at which crosstalks may appear. The cross-talk is evaluated by injecting in the neighboring pixels and checking the occupancy in the central pixel. Can be initiated by the following command:

bin/scanConsole -r configs/controller/specCfg-rd53a.json -c configs/connectivity/example_rd53a_setup.json -s configs/scan/rd53a/std_crosstalkscan.json -p

Disconnected Bump Scan: Crosstalk scan is used to find pixels with no crosstalk, which are most likely caused by unconnected bumps. An analog scan with a crosstalk mask is used. The configuration settings for this scan are the same as those for the crosstalk scan. Can be initiated by the following command:

bin/scanConsole -r configs/controller/specCfg-rd53a.json -c configs/connectivity/example_rd53a_setup.json -s configs/scan/rd53a/std_discbumpscan.json -p

Noise Scan: This scan runs for one minute to find any hot pixel which can provide noise hit, and then mask those pixels. Before running this scan, the SCC should be kept in a dark environment. Can be initiated by the following command:

bin/scanConsole -r configs/controller/specCfg-rd53a.json -c configs/connectivity/example_rd53a_setup.json -s configs/scan/rd53a/std_noisescan.json -p

Source Scan: A second DP-miniDP cable is required to connect to the second DP port in the SCC and port B on the Ohio card, which should have the changes on port B, for the "self-triggering" source scan utilizing Hit-Or as a trigger. The relevant

firmware must be used, which can be found in firmware v0.9.2 as bit files that do not finish with _4chip.bit. Instead of specCfg-rd53a.json, specCfgExtTrigger.json should be used for controller configuration. The Hit-Or lines must be enabled in the chip configuration:

```
"HitOr0MaskDiff0": 65535,
"HitOr0MaskDiff1": 1,
"HitOr0MaskLin0": 65535,
"HitOr0MaskLin1": 1,
"HitOr0MaskSync": 65535,
"HitOr1MaskDiff0": 65535,
"HitOr1MaskDiff1": 1,
"HitOr1MaskLin0": 65535,
"HitOr1MaskLin1": 1,
"HitOr1MaskSync": 65535,
"HitOr2MaskDiff0": 65535,
"HitOr2MaskDiff1": 1,
"HitOr2MaskLin0": 65535,
"HitOr2MaskLin1": 1,
"HitOr2MaskSync": 65535,
"HitOr3MaskDiff0": 65535,
"HitOr3MaskDiff1": 1,
"HitOr3MaskLin0": 65535,
"HitOr3MaskLin1": 1,
"HitOr3MaskSync": 65535,
```

Can be initiated by the following command:

bin/scanConsole -r configs/controller/specCfgExTrigger.json -c configs/connectivity/example_rd53a_setup.json -s configs/scan/rd53a/std_extriggerscan.json -p

All these scan configurations create plots using python and create data files for the plots. Root plots can be made using those data files, to understand more precisely with values. For that, the following command can be used:

bin/ plotFromDir -i data/last_data -P png

Where *last_data* is the data folder created by the scan.

A script can be used to tune RD53A by following this routine:

Pre-tune scans:

- Digital scan, all FE, overwrite masks: -m 1
- Analog scan, all FE
- Threshold scan, all FE, VCAL range 50-300, steps of 5, Mean threshold

Differential Tuning:

- Global threshold tune, 1k e: -t 1000
- Pixel threshold tune, 1k e: -t 1000
- Global preamp tune, 10k e, ToT 8: -t 10000 8
- Pixel threshold tune, 1k e: -t 1000
- Fine pixel threshold tune, 1k e: -t 1000

Linear Tuning:

- Global threshold tune, 2k e: -t 2000
- Pixel threshold tune, 2k e: -t 2000
- Global threshold retune, 1k e: -t 1000
- Global preamp tune, 10k e, ToT 8: -t 10000 8
- Pixel threshold retune, 1k e: -t 1000
- Fine pixel threshold tune, 1k e: -t 1000

Synchronous Tuning:

- Global threshold tune, 1k e: -t 1000
- Global preamp tune, 10k e, ToT 8: -t 10000 8
- Global threshold tune, 1k e: -t 1000

Post-tune scans:

- Threshold scan, all FE, VCAL range 50-300, steps of 5, Mean threshold
- ToT scan, the target of 10k e, Mean ToT

List of Abbreviation and Acronyms

Conseil Européen pour la Recherche Nucléaire	CERN
A Toroidal LHC Apparatus	ATLAS
Large Hadron Collider	LHC
High Luminosity Large Hadron Collider	HL-LHC
Front End	FE
Read out Chip	RoC

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Scientific Production

Journal Publication

1. "Advances in 3D Sensor Technology by Using Stepper Lithography." Frontiers in Physics 8 (2021): 647.
2. "Novel 3D pixel sensors for the upgrade of the ATLAS Inner Tracker." Frontiers in Physics 9 (2021): 2.
3. “Characterization of FBK 3D pixel sensor modules based on RD53A readout chip for the ATLAS ITk.” Journal of Instrumentation (2021)

Conference Publication

1. "Development of Advanced Silicon 3D Sensors at FBK Using Stepper Lithography." 2020 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC). IEEE.

Participation to Congress, Schools, and Workshops

1. Seminar on advanced electron microscopy techniques applied to nanomaterials and nano-objects, 1 hr, January 22, 2019
2. 14th Trento Workshop on Advanced Silicon Radiation Detectors, 3 days, February 27, 2019
3. VIII International Course on Detectors and Electronics for High Energy Physics, Astrophysics, Space Applications and Medical Physics, 5 days, April 5, 2019
4. Seminar on Mechatronic systems based on smart materials, dielectric elastomers & shape memory alloys, 1 hr, May 15, 2019
5. Workshop on Perspectives in Electron Microscopy, 3.5 hrs, June 21, 2019
6. Poster Presentation in autumn career festival
7. 15th Trento Workshop on Advanced Silicon Radiation Detectors, 3 days, February 17, 2020
8. 16th Trento Workshop on Advanced Silicon Radiation Detectors, 3 days, February 16, 2021
9. ACES 2020, 3 days, May 26, 2020
10. 9th Bam Telescope and Test Beam Workshop, 4 days, February 10, 2021

Other Activities

Workshop Talks

1. "Characterization of FBK 3D Pixel Sensor Modules Based on RD53A Readout Chip for the ATLAS ITk", 15th Trento Workshop on Advanced Silicon Radiation Detectors, February 17, 2020
2. "Characterization of 3D Silicon Radiation Detectors using RD53A Readout Chip", ATLAS Italia Young 2021, September 27, 2021

Poster Presented

1. "Development of small-pitch 3D sensors for the High Luminosity LHC" VIII International Course on Detectors and Electronics for High Energy Physics, Astrophysics, Space Applications and Medical Physics, April 5, 2019
2. "Characterization of RD53A modules for ATLAS ITk" Poster Presentation in autumn career festival, November 27, 2019
3. "Development of Advanced Silicon 3D Sensors at FBK Using Stepper Lithography", IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), November, 2020
4. "Characterization of FBK 3D pixel sensor modules based on RD53A readout chip for the ATLAS ITk." 22nd International Workshop on Radiation Imaging Detectors, June 27, 2021

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