Design and TCAD simulation of double-sided pixelated low gain avalanche detectors

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Abstract

We introduce a double-sided variant of low gain avalanche detector, suitable for pixel arrays without dead-area in between the different read-out elements. TCAD simulations were used to validate the device concept and predict its performance. Different design options and selected simulation results are presented, along with the proposed fabrication process.

Keywords: Silicon detectors; avalanche photodiodes; low gain avalanche detector, TCAD simulations.

1. Introduction

Low Gain Avalanche Detectors (LGADs) are attracting wide interest within the HEP community [1]. These devices are similar to avalanche photodiodes (APDs) normally used for light or X-ray detection [2]. Peculiar to LGADs is that the gain layer doping profile is engineered to yield a low gain (from a few units to a few tens, compared to the relatively higher gain of APDs, that can reach ~1000). In fact, LGADs are mainly intended to detect high energy charged particles, so that their gain should compensate loss of signals due to two possible reasons: the use of thin substrates and charge trapping, that is the most severe phenomenon limiting detector performance at very high irradiation fluencies [3]. To this purpose, gain values of just a few units, like those obtained from heavily irradiated n-on-p sensors biased at very high voltage [4], would be sufficient. On the other hand, in order to boost speed properties for timing applications, gain values in the range from 10 to 30 would be desirable and are here considered as a target [5]. With such low gains, standard read-out circuits could be used without risk of signal saturation; moreover, low gain also ensures low excess noise factor [2].

The first LGAD prototypes developed by CNM Barcelona [1] have been characterized by several groups, showing very promising performance. These devices are potentially able to provide concurrent very good position and timing resolution, a fact that could open new opportunities in particle tracking detectors as well as in other fields. Some studies have highlighted a severe gain reduction in LGADs after irradiation [1], [6], so radiation tolerance should be thoroughly addressed in new device developments. In addition, alternative design and fabrication approaches

are necessary to pass from pad detectors to strips and pixels. In fact, existing LGADs are built with a single-sided fabrication process, and feature a blank ohmic contact on the back side and read-out junctions on the front side, embedding an additional doping layer to control the avalanche multiplication mechanism and properly designed terminations to prevent from early breakdown at the edge. This works well for pads, but in case of patterned detectors it would lead to large spatial non uniformities in the signal amplitudes since charge carriers collected at the junction edges would experience reduced (or even null) multiplication. The problem is in fact not new: for fast X-ray imaging applications, arrays of avalanche photodiodes featuring two possible segmentation options (divided cathode and divided anode) have already been proposed, but no details on the detector performance are reported [7].

In this work, we propose a modified, double-sided LGAD structure, having a large multiplication region (n/p junction) on the back side and ohmic read-out pixels on the front side. The device concept has been validated with the aid of TCAD simulations, showing multiplication gains from a few units up to about 30 depending on the doping concentration of the multiplication layer and on the operational conditions. The design options and selected simulation results will be presented, along with the proposed fabrication process to be implemented at FBK (Trento, Italy).

2. Device description and fabrication strategy

In order to obtain charge multiplication at reasonably low voltages, the avalanche process must be initiated by electrons, that have higher ionization coefficient than holes [2]. Therefore, for highly segmented detectors like pixels, the only feasible option consists in using p^- substrates and fabricating a large, uniform multiplication junction ($n^{++}/p^+/p^-$) on one side, and ohmic pixels (p^{++}/p^-) on the opposite side. Since fast timing circuits might be difficult to embed in small pixels, the multiplication region could also be patterned in macro-pixels (~1 mm^2 area, ~1 pF capacitance) with a small reduction of the geometrical efficiency (~5%). By doing so, different functions could be divided between the two sensor sides, using the pixelated ohmic side for position resolution, and the macro-pixelated junction side for timing resolution [8].

The schematic cross section of the proposed device is shown in Fig. 1. The pixel side at the top is simple, since it just requires one boron implantation or diffusion. On the contrary, the gain side is quite complex, since it requires four different patterned doping layers, to be obtained by a combination of ion implantation and thermal diffusion: the gain layer is made by a thin n^{++} region and an overlapping p^+ region, the latter being the most critical for its impact on the device gain and breakdown voltage. In addition, a proper termination able to prevent edge breakdown is necessary. Taking inspiration from power devices, this can be made of a deep n^+ region equipped with a metal field plate, the so called JTE [9]. Moreover, another patterned p^+ region (p-stop) is used to isolate the n^+ regions [10]. In the proposed device, p-stop is preferred to p-spray in order for its doping profile not to be overlapped to the gain layer.

Not shown in Fig. 1, but essential for the device operation, is a multiple guard-ring termination on the gain side, preventing early breakdown at the periphery [11], [12]. To this purpose, existing designs, already tested at FBK and featuring breakdown voltages higher than 1100 V, will be used.
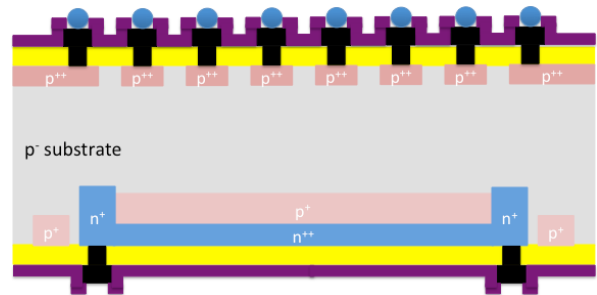

Figure 1 Schematic cross section of proposed double-sided pixelated low gain avalanche detector (not to scale).

The proposed device has some drawbacks: for pixels made on the ohmic side, isolation requires full depletion and inter pixel resistance after irradiation could be an issue; moreover, it is well known that detectors with hole-reading electrodes are less radiation hard than their electron-reading counterparts. Nevertheless, having timing resolution as the main long-term objective of our project, this approach is deemed appropriate for applications calling for moderate radiation hardness.
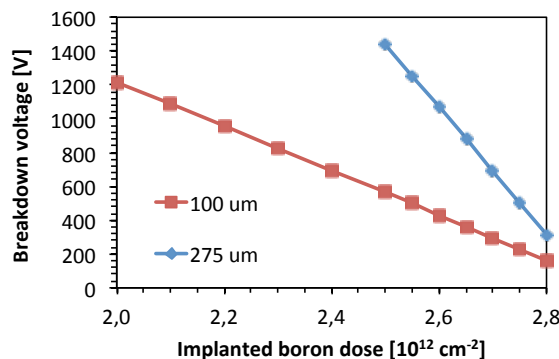
Devices will be fabricated at FBK leveraging on the strong experience with Silicon Photo-Multipliers [13]. To control the multiplication properties and the breakdown voltage, the Boron dose of the p^+ gain layer will be used, hence it is the main process parameter considered in the simulations. The first batch of sensors will be fabricated at FBK on relatively thick (275 μm) 6" wafers, in order to disentangle the issues inherent to LGAD operation from those set by processing thin wafers. However, in order to improve the timing performance, we aim at later work with

148 thinner (~100 μm) substrates. Processing 6" wafers
149 thinner than 200 μm is not easy and probably not
150 compatible with most of the automatic equipment in
151 the fabrication laboratory. To address this problem, we
152 plan to use thin substrates having a support wafer that
153 should then be selectively removed by local etching
154 based on deep reactive ion etching (normally used for
155 3D detectors [14]) or chemical etching [15].

156 **3. TCAD simulations**

157 Simulations have been performed with the
158 Sentaurus Device program, incorporating parameters
159 typical of FBK technology. Depending on the type of
160 simulations, different domains have been used: in
161 particular, 2D simulations were used to predict the
162 electrical characteristics of the devices (e.g., leakage
163 current and breakdown voltage). For the dynamic
164 simulations (charge collection and gain), 2D
165 simulations are not ideal since they do not properly
166 account for the lateral spread of charge clouds, thus
167 overestimating the effects of high charge
168 concentrations [16]. To this purpose, 3D simulations
169 would be the best solution, but they are very time-
170 consuming due to the very large numbers of grid
171 points. Therefore, we have used 2D simulations with
172 cylindrical coordinates that are a good trade-off.
173 Results are here presented showing direct
174 comparisons between data relevant to the first batch
175 (275 μm thickness) and the future one (100 μm
176 thickness). Figure 2 shows the breakdown voltage as a
177 function of the boron dose of the gain layer. The dose
178 dependence of the breakdown voltage is pretty high in
179 both cases, and more pronounced in the thicker device,
180 thus confirming the need for fine tuning of this
181 parameter with process splits.
182

187 In order to compare the device performance for
188 different thicknesses, we considered two doses
189 providing very similar breakdown voltages of about
190 1050 V, i.e., 2.6×10^{12} cm^{-2} for 275 μm and 2.1×10^{12}
191 cm^{-2} for 100 μm. Figure 3 shows the leakage currents
192 as a function of voltage (I-V) in the two devices.
193 Simulation results are scaled to pixels of 50×50 μm^2
194 size. Of course, larger current is observed in the
195 thicker device, due to the larger depletion volume. In
196 both cases, impact ionization effects start affecting the
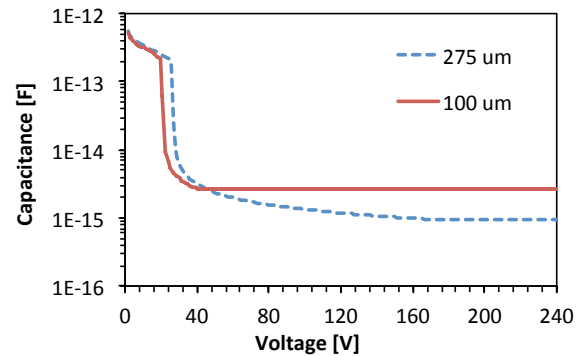197 leakage current well below the breakdown voltage.
198
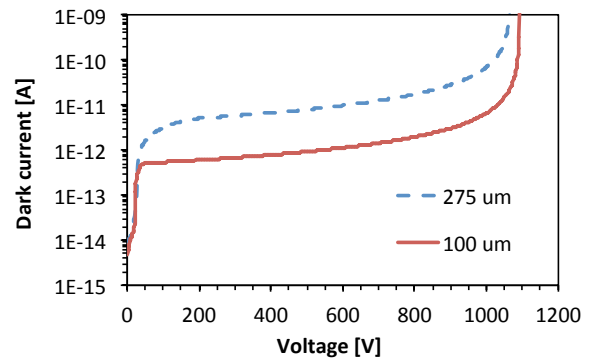
199
200 Figure 3 Leakage current as a function of reverse voltage for
201 100 μm and 275 μm thick sensors.
202

203 Figure 4 shows the capacitance curves as a function
204 of voltage (C-V), which exhibit a two-phase
205 behaviour: at low voltage, the gain layer is initially
206 depleted, then the substrate is depleted until the curves
207 saturate at different values due to the different
208 thicknesses. The transition between the two phases
209 correspond to a sharp decrease in the capacitance, that
210 takes place at a slightly lower voltage in the 100 μm
211 thick device due to the lower boron dose. From the
212 $1/C^2 - V$ curves (not shown), the full depletion
213 voltages are found to be 40 V and 170 V for the 100
214 μm thick and the 275 μm thick devices, respectively.
215

183
184 Figure 2 Breakdown voltage as a function of the boron dose of the
185 gain layer for 100 μm and 275 μm thick sensors.
186

216
217 Figure 4 Capacitance as a function of reverse voltage for 100 μm
218 and 275 μm thick sensors.

219 Simulations also demonstrated that the gain layer
220 can be patterned in macro-pixels without
221 compromising the high voltage capability of the
222 device. In fact, the breakdown voltage of JTEs
223 separated by a p-stop is higher than 1200 V.
224 As for the charge collection properties, Figure 5
225 shows the gain as a function of the voltage, as obtained
226 by simulating the collected charge in case the sensor is
227 hit by a minimum ionizing particle (mip). Particle hit
228 was simulated using the Heavy-Ion model available in
229 the simulator: the released charge was 80 electron-hole
230 pairs per micrometer and the spatial distribution was
231 Gaussian in a region of 1 μm diameter around the
232 track. The gain was calculated as the ratio of the
233 collected charge values obtained by activating the
234 avalanche model divided by those obtained without
235 avalanche multiplication. It can be seen that gain
236 values in the order of 15 can be obtained at high
237 voltages in both cases, but with different trends. In
238 fact, for the 100 μm thick device, the gain remains
239 relatively low up to 800 V, and then sharply increases
240 at higher voltage (a similar behaviour can be observed
241 in the I-V curves in Fig. 3). This is due to the lower
242 boron dose, which requires higher voltages to reach
243 the electric field values necessary for significant
244 charge multiplication. It should also be noticed that, in
245 spite of the relatively low amount of charge released
246 by a mip, high charge concentrations in the gain layer
247 cause a small reduction of the electric field (~ 2
248 kV/cm), yet high enough to slightly reduce the gain,
249 because of the exponential dependence of the
250 ionization coefficients with the electric field. Care
251 should therefore be taken when measuring LGADs
252 with lasers or alpha particles, for which this effect
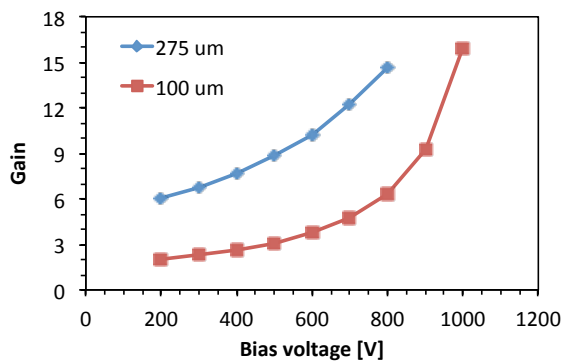253 might be much more pronounced.
254

255
256 Figure 5 Gain as a function of reverse voltage for 100 μm and
257 275 μm thick sensors. Data refer to the sensor response to a mip.
258
259 The gain was also calculated analytically using
260 McIntyre model [17], and it was found in excellent
261 agreement with the simulated one. The model was also

262 used to predict the excess noise factor (F) that takes
263 into account the statistical nature of impact ionization
264 processes and the fluctuations in the actual value of the
265 multiplication gain (M). F depends on M and on the
266 ratio between the ionization coefficients of holes and
267 electrons (k) [16]. As can be seen in Fig. 6, no
268 appreciable differences are observed in the values of F
269 between devices of different thickness, since the value
270 of k is practically the same for both devices. In fact,
271 both data sets are well fitted by the same curve
272 representing the following equation [17]:

$$273 \quad F = M \cdot k + \left(1 - \frac{1}{M}\right) \cdot (1-k) \qquad (1)$$

274
275 for a value of k=0.22. Such a value is about ten times
276 higher than those typical of low-noise APDs, but still
277 good enough for the applications of interest.
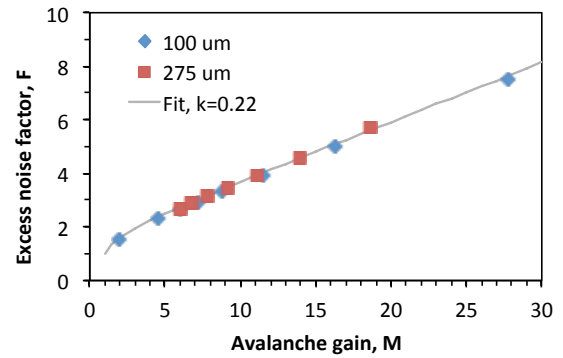278

279
280 Figure 6 Excess noise factor as a function of gain calculated
281 analytically according to McIntyre's theory [16] for the two devices
282 of different thickness, and fitting line of Eq. (1) for k=0.22.
283
284 The simulated signal current waveforms at different
285 reverse voltages are shown in Fig. 7. In the 275 μm
286 thick device, current pulses have a peak at about 4 ns
287 and a total width of almost 10 ns even at 800 V, due to
288 the drift time of the multiplied holes through the
289 substrate. As expected, much faster (~3 times) signals
290 are observed in the 100 μm thick device, with a pulse
291 width of about 3 ns regardless of the voltage, as a
292 result of the smaller distance holes have to travel and
293 to their faster drift at the saturation velocity that is
294 achieved already at low voltage.
295 These results are promising in view of obtaining
296 LGADs with very good timing resolution.
297 Nevertheless, it should be noticed that these
298 simulations were carried out on a domain
299 corresponding to pad structures, for which the
300 weighting field pattern is much more favourable than
301 that of pixel detectors. If electrode segmentation is

302 considered, the current signals can be significantly
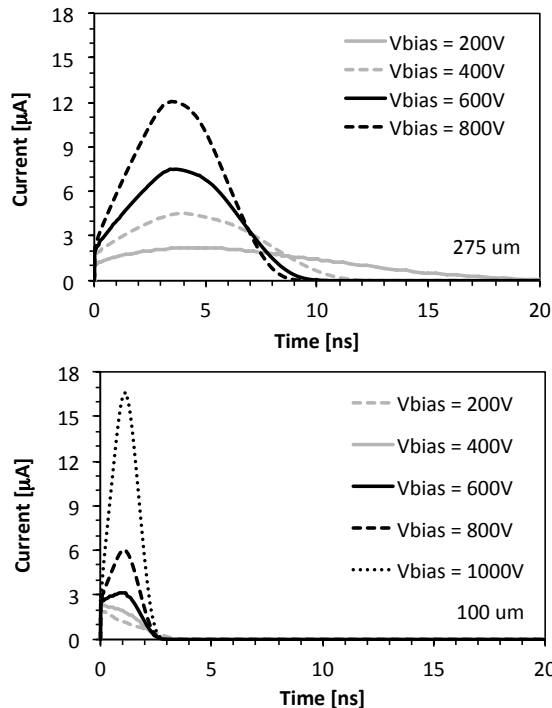303 delayed in case of thick substrates.

304

305

306   Figure 7 Current signals as a function of time at different
307 voltages: (top) 275 μm thick device, and (bottom) 100 μm thick
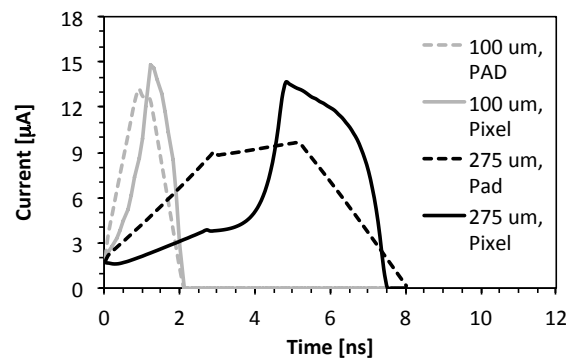308 device.
309

310
311   Figure 8 Current signals as a function of time for 275 μm and
312 100 μm thick devices (pads vs pixels, both with a gain of 15)
313 simulated with Weightfield.
314

315   As an example, Fig. 8 shows the signals simulated
316 with the software Weightfield [18], comparing pad and
317 pixel sensors, the latter with 50 μm pitch, with both
318 275 μm and 100 μm thickness. The gain is set to 15
319 for both devices. It can be seen that for thick sensors
320 the p^+ electrode segmentation results in a significant
321 delay of the signal, as well as in a shape that is not
322 suitable for timing determination, whereas for the thin
323 ones these effects are much less pronounced.

324 **4. Conclusions**

325   We have reported on the design and technological
326 options for the development of double-sided pixelated
327 low gain avalanche detectors. TCAD simulations have
328 been used to predict the sensor performance with
329 encouraging results. Multiplication gains in the order
330 of 15 can be achieved at bias voltages in the range
331 from 800 V to 1000 V, with reasonably low excess
332 noise factor.
333   The wafer layout of the first batch of the proposed
334 sensors, to be fabricated at FBK on 275 μm thick
335 sensors, is being completed, and first samples are
336 expected for delivery in Spring 2015. The timing
337 performance of these first prototypes is not expected to
338 be very good, due to the non negligible drift time of
339 multiplied holes, but it can be significantly improved
340 for 100 μm thick sensors, that will be fabricated in the
341 second batch.

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