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OF TRENTO

DEPARTMENT OF INFORMATION AND COMMUNICATION TECHNOLOGY

38050 Povo – Trento (Italy), Via Sommarive 14
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Francisco Corrêa Alegria, Antonio Moschitta, Paolo Carbone, Andrea Cruz Serra, Dario Petri

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F.CORRÊA ALEGRIA[1], A.MOSCHITTA[2], P.CARBONE[2], A.CRUZ SERRA[1], D.PETRI[3]

[1]TELECOMMUNICATION INSTITUTE AND DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING, INSTITUTO SUPERIOR TÉCNICO, TECHNICAL UNIVERSITY OF LISBON, PORTUGAL, EMAIL: acserra@alfa.ist.utl.pt

[2]DIPARTIMENTO DI INGEGNERIA ELETTRONICA E DELL'INFORMAZIONE, UNIVERSITÀ DEGLI STUDI DI PERUGIA, VIA G.DURANTI, 93, 06125 – PERUGIA – ITALY, EMAIL: carbone@diei.unipg.it

[3]DIPARTIMENTO DI INFORMATICA E TELECOMUNICAZIONI, UNIVERSITÀ DEGLI STUDI DI TRENTO, VIA SOMMARIVE, 14 – 38050 TRENTO, EMAIL: petri@dit.unitn.it

Abstract-*This paper deals with the effectiveness of the Sinewave Histogram Test (SHT) for testing analog to Digital Converters (ADCs). The implementation is discussed, with respect to the adopted procedures and to the choice of relevant parameters. Some of the published approximations currently limiting the characterization of the test performance are removed. Furthermore the statistical efficiency of the SHT is evaluated by comparing the associated estimator variance with the corresponding Cramér-Rao Lower Bound (CRLB), theoretically derived assuming sinewaves corrupted by Gaussian noise. Finally, both simulation and experimental results are presented to validate the proposed approach.*

Keywords: Sinewave Histogram Test, Cramér-Rao Lower Bound

I. INTRODUCTION

Analog to Digital Converters (ADCs) are currently adopted in many application fields to implement digital systems which achieve superior performances with respect to analog solutions. Various examples of ADC applications can be found in Data Acquisition Systems, Measurement Systems, or Digital Communication Systems. Such a widespread usage confers great importance to the testing activities, which nowadays largely contribute to the production costs of integrated circuit devices. In this regard, it should be observed that the ADC test duration and costs tend to grow significantly for high resolution ADCs [1]. Hence, choosing an efficient test and improving the associated performance may significantly reduce the industrial cost of an ADC manufacturing process. ADCs are usually characterized by figures of merit like effective resolution, Signal to Noise and Distortion Ratio (SINAD), Integral Non-Linearity (INL) or Differential Non-Linearity (DNL) [2]. In particular, INL and DNL are of great interest when the quality of the manufacturing process has to be controlled. Various ADC testing procedures have been proposed in the literature in

order to estimate these parameters [1]. A popular method is the Sinewave Histogram Test (SHT), which estimates INL and DNL related to each transition voltage of an ADC stimulated by a pure sinewave [3][4][5][6].

In this paper, the performance of the SHT is analyzed and discussed, taking into consideration both theoretical and practical aspects. In particular, a practically relevant stimulus, consisting in an ideal sinewave corrupted by an additive white Gaussian noise is considered, and the effects of noise are analyzed. First, the SHT implementation issues are discussed and improvements are presented that remove some of the published approximations currently limiting the characterization of the test performance. Then, the statistical efficiency of the SHT is evaluated by comparing the variance of the achieved estimator with the corresponding Cramér-Rao Lower Bound (CRLB) [7][8][9]. To this aim, the CRLB associated to the estimation of the transition levels of an ADC fed by a noisy stimulus has been theoretically modeled, both for biased and unbiased estimators. Finally, both simulation and experimental results are provided to validate the proposed results.

II. The Sinewave Histogram Test

The SHT is used to estimate the input-output characteristic of ADCs, that is the transition voltages and code bin widths, which are generally expressed as integral non-linearity (INL) and differential non-linearity (DNL) respectively, together with gain and offset errors. The estimates are obtained by comparing the number of samples counted in each ADC output code bin (histogram) when a sinusoidal input signal is employed, with that expected when assuming a pure sinewave feeding the ADC under test. The difference is then associated to the non-ideal ADC behavior. In particular, the transition voltages T_k are estimated by determining the probability of the input voltage being in the range $]-\infty,T_{k+1}]$, assuming an ideally behaving ADC, and measuring the cumulative histograms c_k, that is the number of acquired samples exhibiting output code equal to or lower than k. Such parameter depends on the actual transition voltage and on the total number of acquired samples M. The expression for the transition voltages estimator $\hat{T}_k$, is [3][6]:

$$\hat{T}_k = C - A\cos\left(\pi \frac{c_{k+1}}{M}\right) \qquad k = 0,\ldots,N-1 \tag{1}$$

where C and A are the input signal offset and amplitude respectively, suitably chosen to stimulate all possible output codes. The estimates are affected by various uncertainty sources. For example, according to the relative frequency approach to the probability theory, acquiring a finite number of samples limits the accuracy with which probabilities can be estimated. Other sources of uncertainty are discussed in the following.

A. Stimulus signal non-idealities

The testing process, which is easily implemented in practice, is subject to several accuracy limiting factors [2][3].

The most important are the stimulus signal non-idealities and the uncertainty of the ratio between input sinewave frequency and ADC sampling rate.

The stimulus signal usually exhibits some distortion (mainly harmonic) which affects the input voltage distribution making the estimates erroneous. To minimize the consequences of this effect, a function generator should be used with a Spurious Free Dynamic Range (SFDR) high enough to make the distortion error power negligible compared to the quantization noise power. This can be achieved by considering that an ideal n_b bit quantizer, fed with a sinusoidal signal, exhibits a signal to quantization noise ratio of approximately $(6.02n_b+1.76)$ dB.

An additional error contribution is given by wideband noise introduced by test bed components and by input-referred ADC noise sources, which cause the quantized signal to differ from a pure sinewave. Unfortunately a closed-form expression for a transition level estimator that compensates for the effects of noise has not been yet derived. Moreover, even if there was one, it would probably not be useful in practice since the noise standard deviation should be estimated with an accuracy greater than that established for the transition voltages. Noise effects are usually reduced by overdriving the ADC, that is by applying a sinewave with an amplitude slightly higher than the minimum one needed to stimulate all ADC codes. Such a strategy is effective because, due to the sinewave amplitude distribution, the noise effects are more pronounced near the ADC full-scale [4].

Furthermore, in order for the phase of the collected samples to be uniformly distributed, the sampling rate f_s and the stimulus signal frequency f should satisfy the following [3]:

$$\frac{f}{f_s} = \frac{J}{M}, \tag{2}$$

in which the integer number J of acquired sinewave periods is assumed to be mutually prime with M [2]. In real applications however, this requirement is not easily satisfied, because of the finite frequency resolution of both the sinewave generator and the ADC internal clock. Hence, phases of the collected samples are not uniformly distributed, and an additional error is introduced in the estimation of the transition voltages [2]. Finally, uncertainties in the values of both input sinewave amplitude and offset affect the accuracy of the transition voltage estimates, as can be directly deduced from (1).

B. Determination of the test parameters

Performing the SHT requires to set the value of the input sinewave amplitude, offset and frequency, and to choose the number of collected samples. The selection of these test parameters requires some caution. First, the sinewave amplitude, offset and frequency can not be arbitrarily selected, because the corresponding resolutions r_A, r_C and r_f, are limited by the function generator characteristics. Furthermore, due to the generator limited accuracy, the sinewave is affected by an amplitude error e_A, an offset error e_C and a frequency error ε_f. Similarly, a frequency error ε_{fs} is associated

to the external or internal ADC sampling clock. Second, the ADC under test is characterized by both gain and offset errors, which affect the actual ADC input range, that is the difference between the last and first transition voltages. Both these errors should be estimated a priori in order to determine an upper bound for each error contribution. Then, after the test is carried out, the estimated gain and offset errors should be compared with the corresponding bound to verify that it is not reached. If this is not the case, larger bounds should be assumed, and the test should be repeated. Notice that the input range V_r of an ideal ADC is twice the Full-Scale (*FS*) specification and that the ADC gain is the factor by which the real transition voltages should be multiplied to get the ideal transition voltages [2]. Thus, if the ADC gain is lower than the ideal value of 1, for instance $1-\varepsilon_G$ where $\varepsilon_G>0$ is the relative gain error, the ADC input range increases to $V_r^{'} = 2FS/(1-\varepsilon_G)$. Furthermore, an offset error of magnitude ε_C may directly displace the transition voltages, so that the converter input range becomes

$$V_r^{'} = 2FS/(1-\varepsilon_G) + 2|\varepsilon_C|, \tag{3}$$

in which the offset sign has been assumed unknown a priori.

Obviously, the test parameters should be chosen with the aim of minimizing the effects of all known error sources. Accordingly, it is important to characterize properly the statistical properties of the INL and DNL estimators in order to establish both test performance parameters and corresponding upper bounds. In this respect, bias and variance of INL and DNL estimators are considered and used both to provide an effective ADC testing procedure and to compute the statistical efficiency of the transition level estimator.

1) Sinewave amplitude

The signal amplitude is determined to guarantee with high confidence that the samples acquired when the input voltage is near the sinusoid extremes do not introduce errors in the estimated INLs and DNLs greater than B_{eINL} (defined in least significant bit units) and $B_{\varepsilon DNL}$ (defined as a fraction of the actual DNL values), respectively. In accordance to this requirements the following specifications apply for the sinewave amplitude:

$$A \geq \frac{V'_r}{2} + V_{OD} + e_A + \frac{r_A}{2}, \tag{4}$$

in which V'_r is given by (3) and

$$V_{OD} = \max\left(V_{OD_{INL}}, V_{OD_{DNL}}\right), \tag{5}$$

where

$$V_{OD_{INL}} = \begin{cases} 1,28\dfrac{\sigma^2}{4\cdot Q\cdot B_{eINL}} & , \quad B_{eINL} \leq \dfrac{\sigma/Q}{5} \\ 0 & , \quad \text{otherwise} \end{cases}, \tag{6}$$

and

$$V_{OD_{DNL}} = \begin{cases} \sigma\sqrt{\dfrac{3.2}{8\cdot B_{\varepsilon DNL}}} & , B_{\varepsilon DNL} < 8\% \\ 1.8\sigma\left(0.65 - B_{\varepsilon DNL}\right), & 8\% \le B_{\varepsilon DNL} \le 65\% \\ 0 & , B_{\varepsilon DNL} > 65\%. \end{cases} \quad (7)$$

where Q is the ideal code bin width and σ is the additive noise standard deviation which should be estimated prior to apply the SHT (see Appendix A). Notice that for values of the maximum allowable INL error exceeding $\sigma/5$ and DNL relative error exceeding 65% there is no need to use overdrive (if the noise standard deviation is lower than 1% of the sinewave amplitude, as often occurs in practice). Moreover, $r_A/2$ in (4) accounts for the finite amplitude resolution r_A of the function generator. Also, to guarantee that the actual amplitude of the input sinewave is never smaller than $V'_r/2 + V_{OD}$, the function generator should be set to an amplitude higher than the one required by the maximum function generator amplitude error e_A.

2) Number of samples and input signal frequency

As shown in [5], the contributions of both the unknown sinewave phase and the additive noise affect the estimation of the ADC parameters. For instance, the variance $\sigma^2_{T_k}$ of the k-th transition voltage estimator can be expressed by

$$\begin{aligned} &\sigma^2_{T_k} \cong \alpha_k(1-\alpha_k)\frac{\pi^2}{M^2}\left[A^2 - \overline{T}_k^2\right] + \frac{1.78}{M}\sigma\sqrt{A^2 - \overline{T}_k^2}, \quad A \ge \overline{T}_k,\ k = 1,..,N-1 \\ &\alpha_k = \left\langle \frac{2\psi_k}{\Delta\phi} \right\rangle, \qquad \psi_k = \arccos(-\overline{T}_k / A), \qquad \overline{T}_k = T_k - C, \qquad \Delta\phi = 2\pi / M \end{aligned} \quad (8)$$

where $\langle\cdot\rangle$ is the fractional part operator. Thus, by following a worst-case approach, for large values of M we obtain

$$\sigma^2_{T_k} \le 1.78\frac{A\sigma}{M} \quad (9)$$

In practical cases, the standard deviation of additive noise is small compared to the ideal code bin width, so that the transition voltages may be assumed mutually uncorrelated [4]. As a consequence, the variance of the estimated code widths, $\hat{W}_k$, is bounded by twice the variance given by (9). Moreover (9) shows that for large values of M the estimator variance is inversely proportional to M.

The INL and DNL are the most frequently adopted metrics for evaluating the ADC input-output characteristic and relate the real transition voltages and code bin widths, after gain and offset error correction, with their ideal values. Since gain and offset errors can be estimated with high accuracy, an upper bound to the variance of INL and DNL is

given by (9), and twice this value respectively [4]. Thus, by considering that such figures of merit are usually expressed in units of LSBs (Least Significant Bits), the minimum number of samples to acquire for achieving a given level of estimation accuracy is

$$M \geq \max\left(\frac{1}{B_{pINL}^2}, \frac{2}{B_{pDNL}^2}\right) \cdot 1.78 \cdot A \cdot \sigma \cdot \left(\frac{K_\nu}{Q}\right)^2, \tag{10}$$

where K_ν is the coverage factor corresponding to a confidence level ν such that $\sigma K_\nu \leq B_p$, where B_p is B_{pINL} or B_{pDNL} depending on whether the estimation of INL or DNL is being performed.

C. *Determining the Results*

The output codes of the acquired samples should be used to compute the cumulative histogram c_k obtained by counting the number of samples with code index equal to or smaller than k. From the cumulative histogram the estimated transition voltages $\hat{T}_k$ are obtained using (1), with a sinewave amplitude A given by (4) and a null offset (C=0).

The code bin widths are estimated by subtracting consecutive transition voltages, that is by using:

$$\hat{W}_k = \hat{T}_{k+1} - \hat{T}_k, \qquad k = 0,....,N-2. \tag{11}$$

The parameters that are usually supplied are the estimated INL and DNL given by

$$\hat{INL}_k = \frac{T_k^{id} - \left\{G\hat{T}_k + e_D\right\}}{Q}, \qquad k = 0,....,N-1, \tag{12}$$

where e_D is the maximum possible offset error and T_k^{id} is the k-th transition level of an ideally behaving uniform ADC, and

$$\hat{DNL}_k = \frac{G\hat{W}_k - Q}{Q}, \qquad k = 0,....,N-2. \tag{13}$$

The estimated gain and offset errors can be determined from the transition voltages according to [2]. Together with these values the maximum error (B_{eINL} and B_{eDNL}) and uncertainty (B_{pINL} and B_{pDNL}) should be stated.

III. CRAMÉR-RAO LOWER BOUND ON THE TRANSITION LEVEL ESTIMATION

The Cramér-Rao Lower Bound (CRLB) related to the estimation of the decision thresholds in an ADC fed by a noiseless sinewave has been theoretically evaluated in [1], where it is proven that assuming a noiseless stimulus, the efficiency of the SHT transition level estimator is nearly optimal, that is its variance tends to the corresponding CRLB, as the number M of processed samples is increased.

In this paper, the CRLB is analyzed assuming a zero mean Gaussian noise superimposed to the ADC input sinewave, which is a situation of more practical interest. In particular, Fig.1 shows how the CRLB for unbiased estimators depends on the transition level T_0 of a single bit A/D. Both simulation and theoretical results achieved for various noise levels are reported in this figure. Simulation results are obtained by applying Monte Carlo methods for the estimation of the partial derivatives required by the Fisher information matrix [6][7][8]. In particular, 10^7 data records each based on M=9 samples of a full-scale sinewave have been used. Conversely, the theoretical results have been obtained by numerically

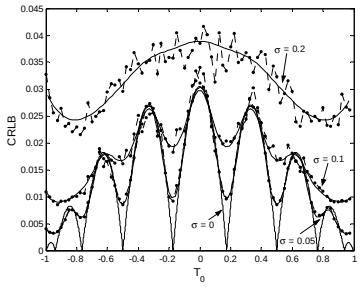

Fig. 1: CRLB, simulation and theoretical results, plotted as a function of the value assumed by the transition level T_0. The continuous lines have been obtained theoretically, while the dotted lines report simulation results.

integrating (B.7) and (B.11) reported in Appendix B, which can not be easily solved analytically. It can be seen that simulation data show a good agreement with theoretical results. Moreover, the CRLB has a more regular behavior with respect to the pure sinewave case, varying less abruptly with the threshold when additive Gaussian noise is present. This can be explained by observing that the CRLB changes are due to the lack of knowledge about the phase of the input sinewave, whose effect tends to become negligible when the noise level increases [2]. It is worth noticing that for moderate amounts of noise, the CRLB maxima are lower than the corresponding ones when a noiseless sinewave is assumed, while under the same assumptions the CRLB minima are higher.

Since (1) is a biased estimator [5], the results reported in Fig.1 require adjustments in order to provide the corresponding CRLB. Figs. 2(a) and 2(b), show the variance $\sigma^2_{T_k}$ of (1) (given by (8)), the related noise contribution, and the CRLB associated to biased estimators (see appendix B), obtained for two different noise levels. These results have been obtained by considering an overdrive voltage V_{OD} = 0.3FS. In fact, the Cramér-Rao bound increases very

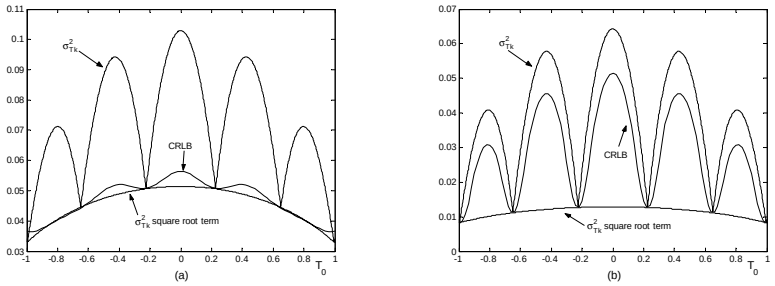

Fig. 2: Variance of the SHT estimates and CRLB, evaluated for biased estimators, σ=0.2 (a) and σ=0.05 (b). The square root term of (10) is also plotted.

quickly when transition levels close to the input sinewave amplitude are estimated. Notice that $\sigma^2_{T_k}$ presents local minima, which coincide with the CRLB when the threshold level T_0 is not close to the sinewave amplitude. Thus, the SHT is locally optimal with respect to the statistical efficiency. Also notice that (8) is the summation of two positive terms. The first one is due to lack of knowledge about the sinewave phase and is responsible for the oscillations of $\sigma^2_{T_k}$, while the second one models the noise contribution. Since the local minima of (8) correspond to values of T_0 where first term is null, Fig.2 shows that the second term of (8) is very close to the CRLB. Now, for large values of M, the effect of sinewave phase behaves like $1/M^2$, while the noise contribution tends to zero like $1/M$. Hence, for values of M used in practice, it is expected that the SHT provides almost efficient estimators also for noisy input signals. Furthermore the CRLB associated to the transition level estimators can be expressed as

$$CRLB \cong \frac{1.78\sigma}{M}\sqrt{A^2 - T_k^2}, \qquad A \geq T_k, \quad k = 0,..,N-1 \tag{14}$$

IV. EXAMPLE

To illustrate the use of the procedure described in section II, we performed a SHT on a National Instruments 6023E 12-bit data acquisition board (DAQ). On preparing the test we assumed the following requirements were made: "Test the dynamic performance of this DAQ at its maximum sampling frequency and in the ±10V range using the SHT". Since we are testing a 12-bit ADC we need a sinusoidal function generator with a SFDR better than 74dB as mentioned before and which can output amplitudes a little higher than 10V (the DAQ full-scale). Thus we used the Stanford DS360 Function Generator**.** We chose here to perform the test with a 200Hz sinusoidal stimulus signal. A more complete approach would require the repetition of the test for different input frequencies in order to transmit to the end-user the behavior of this particular board in different input signal conditions. Since the specifications for the function generator do not supply information about the SFDR but only about the total harmonic distortion (THD) [2], which is stated to be better than 105dB, we will assume that the SFDR will be better than the required 74dB.

For the determination of the exact amplitude of the sinusoid to use we will assume a maximum possible gain error, ε_G, of 2.75% and a maximum possible offset error, e_D, of 28mV according to the DAQ specifications. Using (3) this leads to an input range, V'_r, of 20.62V.

To determine the required overdrive the standard deviation of additive noise must be known. The DAQ specifications state a value of 0.1 LSB for the "system noise not including quantization." The test setup however also contributes to the additive noise. We performed a test using the method recommended in [2] and estimated the total additive noise to have a standard deviation of 2mV. The function generator amplitude error was stated has being 1%. In our case where the sinusoid amplitude is close to 10V this corresponds to a possible amplitude error of 100mV (e_A). The amplitude resolution is stated to be "4 digits or 1μV whichever is greater." In our case this corresponds to 10mV (r_A). The sinusoid amplitude chosen was A=10.42V according to (4), and considering B_{eINL}=0.1LSB and B_{eDNL}=10%.

The minimum number of samples has been calculated, obtaining 1,684,607 for a precision in the INL and DNL values of B_{pINL} =0.1LSB and B_{pDNL}=0.2LSB. In order to guarantee (2) and using the procedure suggested in [2] we reached the value of 1,684,999 for the number of acquired samples and an input frequency of 200 Hz (J=1685). Furthermore, the standard uncertainties σ_{INL} and σ_{DNL} have been evaluated according to [10], obtaining σ_{INL}=0.06LSB and σ_{DNL}=0.016LSB. Such results are compatible with the INL and DNL precisions.

The test was executed and the independently based gain and offset errors were computed according to [2] leading to the values 0.14% and -2.82mV respectively. These values are lower than the maximum values chosen a priori (2.75% and 28mV) so those assumptions were verified. The estimated INL and DNL, computed from (11) and (12), are represented in Fig. 3.

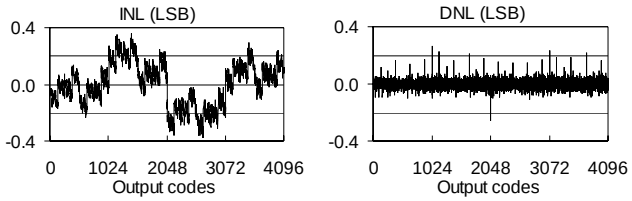

Fig. 3: Representation of the estimated INL and DNL sequences.

V. CONCLUSIONS

The performances and the efficiency of the SHT, have been discussed and analyzed in this paper. In particular, the characterization of the test performance has been improved by removing some commonly adopted approximations. Finally the statistical efficiency of the SHT has been evaluated by comparing the estimator variance to the corresponding CRLB, computed both theoretically and by means of simulations. The results suggest that the SHT is asymptotically optimal also when a Gaussian white noise is superimposed to the sinusoidal stimulus.

VI. Appendix A: Derivation of the Considered Overdrive

In [4] the sampled voltage amplitude distribution is computed by convolving the amplitude distribution of a perfect sinusoidal signal with the probability density function of Gaussian noise (see (31) in [4]). The probability distribution of the estimated transition voltages is then approximated using a Taylor expansion leading, after some simplification, to (33) of [4]. The overdrive is then determined so that the maximum error for the INL is less than $B/4$ LSBs where B is specified by the user:

$$V_{OD_{INL}} = \frac{\sigma^2}{QB}. \tag{15}$$

Because of the approximations used, the actual error is 28% greater then *B/4* when using $V_{OD_{INL}}$ given by (15) for values of $V_{OD_{INL}}$ lower than 2σ [4], expression (15) was changed to

$$V_{OD_{INL}} = \max\left(2\sigma, \frac{\sigma^2}{QB}\right), \tag{16}$$

which is the expression (9) proposed in [4] and also used in Eq. (10) of [2]. Here we suggest three changes to it, leading to Eq. (6):

- Instead of defining the maximum admissible error for the INL has a fraction of ¼ LSB (B) we define it as a fraction of 1 LSB (B_{eINL}). So $B_{eINL}=B/4$;
- We calculated numerically the actual INL error for a wider range of values of the additive noise standard deviation than those calculated in [4] and found that it is in the worst case 28% higher than the value given by the approximation leading to (15) for any value of $V_{OD_{INL}}$, not just for values higher than 2σ as stated in [4]. So we propose that the factor 2σ is removed from (16) and a multiplying factor 1.28 is used as shown in (6);
- In Fig. 4 we represent the results of the numerical calculation of the transition voltage estimation error. It is observed that the error is always lower than σ /5 for σ lower than 1% of the sinusoid amplitude (A). As a consequence we would limit the usage of overdrive to the situation when the maximum admissible error is lower than one fifth than the noise standard deviation. For higher values of maximum admissible error (B_{eINL}) there is no need to use overdrive because the error will never be greater than B_{eINL} as shown in Fig. 4 for A=1 (A=V_r/2).

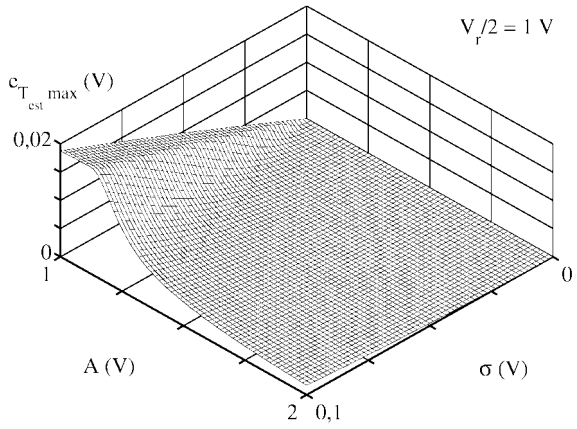

Fig. 4: Representation of the maximum estimated transition voltages error as a function of sinusoid amplitude and noise standard deviation determined by numerical integration of the analytical expressions for the error.

The proposed expression for the amount of overdrive required to guarantee an error in the estimated values of the INL lower than B_{eINL} is thus (6).

In the case of the error in the code bin widths (and DNL), [4] starts by calculating the probability density of the sampled signal by convolving the probability density of a sinusoid with the probability density of Gaussian noise [4]. Then the ratio between the estimated code bin width $\hat{W}$ and the real code bin width W is approximated by the ratio between the probability density of the sampled voltage when additive noise is present ($g(x)$) and when it is not ($f(x)$) as stated in the equation following Eq. (27) in [4]. This is just approximately true because the proportionality constant between W_m and $g(x)$ is different from the probability constant between W and $f(x)$. Blair then proceeds to determine the relative error and then the amount of overdrive required, obtaining the following expression

$$V_{OD_{DNL}} = \sigma\sqrt{\frac{3}{2B}}\,. \tag{17}$$

Because of the approximations used, the actual error is 43% greater then B when using $V_{OD_{DNL}}$ given by (17) for values of V_{ODDNL} lower than 3σ, so expression was changed to

$$V_{OD_{DNL}} = \max\left(3\sigma, \sigma\sqrt{\frac{3}{2B}}\right), \tag{18}$$

which is present in Eq. (8) of [4] and which is also used in [2].

Here the relative error ε_{Lest} of the code bin widths estimation was computed numerically (solid line in Fig. 5) and an empirical expression was determined in order to a make it possible to compute approximately the relative error (dashed line in Fig. 5). This lead to expression (7) for the amount of overdrive required to guarantee a relative error lower than $B_{\varepsilon DNL}$ (in LSB).

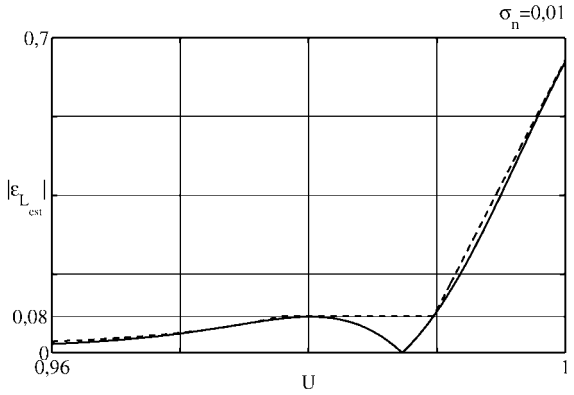

Fig. 5: Representation (solid line) of the relative error of the estimated code bin widths as a function of the transition voltage divided by the sinusoid amplitude (for null offset), U, for a noise standard deviation equal to 1% of the sinusoid amplitude. This was determined using numerical simulation. The dashed line represents the approximation given by (7).

VII. Appendix B: Derivation of the CRLB for Sinewave ADC input affected by additive Gaussian Noise

Let us indicate with T the vector of the ADC transition levels to be estimated, and let us define $\mathbf{Y}$ as a random variable (rv) whose possible realizations belong to the space of the experimental outcomes. Furthermore, let us assume that t_T is a scalar statistic of the sample space associated to the ADC output, expressed as a function of the unknown ADC transition levels. The *CRLB* associated to the variance of an estimator t' of t_T with a bias $b_T = \mathrm{E}[t']-t_T$ is given by

$$CRLB = \left[\nabla t_T + \nabla b_T\right]^T F^{-1}\left[\nabla t_T + \nabla b_T\right], \tag{B.1}$$

where ∇ is the gradient operator, that is $\nabla t_T=[\partial t_T/\partial T_0, \partial\, t_T/\partial T_1,\ldots, \partial t_T/\partial T_{N-1}]$, and $\nabla b_T=[\partial b_T/\partial T_0, \partial b_T/\partial T_1,\ldots, \partial b_T/\partial T_{N-1}]$ [5]. As this analysis is focused on the CRLB associated to the estimation of the i-th transition level-T_i, we have $t_T = T_i$ and:

$$\frac{\partial t_T}{\partial T_j} = \begin{cases} 1, & i = j \\ 0, & i \neq j \end{cases}, \tag{B.2}$$

Let us define $P\{\mathbf{Y}=Y;T\}$ as the probability of occurrence of a given realization Y in the sample space of the ADC output. The Fisher information matrix can be expressed as [7]:

$$F = E\left\{\left[\nabla \log P\{\mathbf{Y} = Y;T\}\right]\left[\nabla \log P\{\mathbf{Y} = Y;T\}\right]^T\right\}, \tag{B.3}$$

where $E\{\cdot\}$ is the expected value operator. By developing (B.3), the elements of the Fisher information matrix may be obtained as

$$F_{n,m} = \sum_Y \frac{1}{P\{\mathbf{Y} = Y;T\}} \frac{\partial P\{\mathbf{Y} = Y;T\}}{\partial T_n} \frac{\partial P\{\mathbf{Y} = Y;T\}}{\partial T_m}, \tag{B.4}$$

where the summation is performed on all the possible realizations Y for which $P\{\mathbf{Y}=Y;T\}\neq 0$.

In the following subsections, the CRLB on the estimation of the ADC transition level will be discussed for an ADC stimulus consisting of a sine-wave corrupted by additive white Gaussian noise. Both unbiased and biased estimators will be considered.

a) *Unbiased estimators*

Let us assume that the ADC stimulus is expressed by the following

$$x_n = A\sin\left(2\pi\frac{D}{M}n+\phi\right)+\eta_n, \qquad n=0,...,M-1, \tag{B.5}$$

where M is the record length, D and M are mutually prime numbers, ϕ is the initial phase, which is uniformly distributed in $[0,2\pi]$ when different records are considered, and η_n is a zero mean Gaussian white noise with standard deviation σ. Let us define $\mathbf{X}=[\mathbf{x}_0\ldots\mathbf{x}_{M-1}]$ as the vector of random variables that models the samples at the ADC input. Similarly, let us define $\mathbf{Y}=[\mathbf{y}_0\ldots\mathbf{y}_{M-1}]$ as the vector of the corresponding ADC output codes. If N is the number of ADC thresholds and $N+1$ the number of output codes, $\mathbf{Y}$ may assume $(N+1)^M$ different values. In a single record of M samples, ϕ is constant, so the ADC input (B.5) is a sequence of normally distributed and mutually independent random variables, with mean values $\mathrm{E}\{x_n\} = A\sin(2\pi Dn/M+\phi)$. Hence, by noticing that the ADC transfer function is memoryless, the probability of occurrence of a given ADC output sequence is given by the product of the marginal probabilities of occurrence of the individual samples, that is:

$$P\{\mathbf{Y}=Y;T\}=E\{P\{\mathbf{Y}=Y\mid\phi;T\}\}=\frac{1}{2\pi}\int_0^{2\pi}\prod_{j=0}^{M-1}P_j(y_i\mid\phi;T)d\phi\,. \tag{B.7}$$

where $P_j\{y_i|\phi\,;T\}$ is the probability that the *j-th* sample of the ADC output equals a given output code y_i, conditioned to the values assumed by the initial phase ϕ, and the outermost expectation is carried out over ϕ. This operation, performed by integrating on the real axis the product of the marginal probabilities $P_j\{y_i|\phi\,;T\}$ and the phase probability density function, removes the dependence on ϕ. By observing that $P_j\{y_i|\phi\,;T\}=\mathrm{P}\{T_{i-1}\le\mathbf{y}_j<T_i\}$, the marginal probabilities can be easily defined in terms of the noise probability distribution function, giving the following

$$P_j(y_i \mid \phi;T)=\begin{cases}\Phi\left(\dfrac{T_0-A\sin\left(\dfrac{2\pi Dj}{M}+\phi\right)}{\sigma}\right) & i=0\\ \Phi\left(\dfrac{T_i-A\sin\left(\dfrac{2\pi Dj}{M}+\phi\right)}{\sigma}\right)-\Phi\left(\dfrac{T_{i-1}-A\sin\left(\dfrac{2\pi Dj}{M}+\phi\right)}{\sigma}\right) & i=1,...,N-1\\ 1-\Phi\left(\dfrac{T_{N-1}-A\sin\left(\dfrac{2\pi Dj}{M}+\phi\right)}{\sigma}\right) & i=N\end{cases}, \tag{B.8}$$

where $\Phi(\cdot)$ is the probability distribution function of a zero mean unity-variance Gaussian rv.

In order to derive the Fisher matrix, the partial derivatives of $P(\mathbf{Y}=Y;T)$ with respect to the transitions levels T_i are needed. To this extent, it can be observed that $P_j(y_i|\phi,T)$ is differentiable with respect to any T_i. Hence, according to theorem 4.1 in [11] it is possible to differentiate under the integral sign, as expressed by the following

$$\frac{d}{dT_h}P\{\mathbf{Y}=Y;T\}=\frac{1}{2\pi}\frac{d}{dT_h}\int_0^{2\pi}\prod_{j=0}^{M-1}P_j\{y_i \mid \phi;T\}d\phi=\frac{1}{2\pi}\int_0^{2\pi}\frac{d}{dT_h}\prod_{j=0}^{M-1}P_j\{y_i \mid \phi;T\}d\phi, \tag{B.9}$$

where the derivative of the product of the marginal probabilities can be rewritten as

$$\frac{d}{dT_h}\prod_{j=0}^{M-1}P_j\{y_i \mid \phi;T\}=\sum_{j=0}^{M-1}\left[\left(\frac{d}{dT_h}P_j\{y_i \mid \phi;T\}\right)\prod_{k\neq j}P_k\{y_i \mid \phi;T\}\right], \tag{B.10}$$

By applying (B.8), the derivatives of the marginal probabilities are expressed by

$$\frac{d}{dT_h}P_j(y_i \mid \phi;T)=\begin{cases}\dfrac{1}{\sigma}\varphi\left(\left(T_i-A\sin\left(2\pi\dfrac{D}{M}j+\phi\right)\right)\Big/\sigma\right), & i=0,...,N-1, & h=i\\ -\dfrac{1}{\sigma}\varphi\left(\left(T_i-A\sin\left(2\pi\dfrac{D}{M}j+\phi\right)\right)\Big/\sigma\right), & i=1,...N, & h=i-1,\\ 0, & otherwise & \end{cases} \tag{B.11}$$

where $\varphi(\cdot)$ is the pdf of a Gaussian zero mean unity-variance rv. Finally, equations (B.4), (B.7) and (B.11) provide the Fisher information matrix and the CRLB for unbiased estimators.

b) *Biased Estimators*

When biased estimators are considered, the CRLB depends on how the bias varies with the ADC transition levels. In particular, for SHT estimators we have [3]:

$$b_{Tk} = E\{t'_k\} - t_{Tk} = \frac{\sigma^2}{2}\frac{\overline{T}_k}{A^2 - \overline{T}_k^2}, \quad \overline{T}_k = T_k - C, \qquad k = 0,...,N-1, \tag{B.12}$$

where b_{Tk} is the k-th element of b_T, that is the bias of the k-th ADC transition level estimator. It follows that the partial derivatives of b_T are given by

$$\frac{\partial b_{Ti}}{\partial T_j} = \begin{cases} \dfrac{\sigma^2}{2}\dfrac{A^2 + \overline{T}_i^2}{\left(A^2 - \overline{T}_i^2\right)^2}, & i = j \\ 0, & i \neq j \end{cases} \tag{B.13}$$

In particular, when a single bit ADC is considered , from (B.4) we have:

$$CRLB = \left(1 + \frac{\sigma^2}{2}\frac{A^2 + \overline{T}_0^2}{\left(A^2 - \overline{T}_0^2\right)^2}\right)^2 F^{-1}, \tag{B14}$$

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