UNIVERSITÀ
DI TRENTO

Department of Industrial Engineering

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Development of monolithic active pixel sensors for radiation imaging

Supervisors:
Prof. Lucio Pancheri
Prof. Gian Franco Dalla Betta

PhD candidate:
Thomas Corradino

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Abstract

The development of Fully Depleted Monolithic Active Pixel Sensors (FD-MAPS) represents nowadays a hot-topic in the radiation detector community. The advantages in terms of production costs and easiness of manufacturing in comparison to the state-of-the-art hybrid detectors boost the research effort in the direction of developing new CMOS compatible detector technologies. To this end, the INFN ARCADIA project targeted the design of a sensor platform for the production of FD-MAPS to be employed in different scientific, medical and space applications. The sensor technology has been developed in collaboration with LFoundry on the basis of a standard 110 nm CMOS production process with some modifications needed to meet the project requirements. High resistivity n-type silicon substrates have been chosen for the sensor active volume and a n-type epitaxial layer has been included at the sensor frontside to delay the onset of the punch-through current flowing between the frontside and backside p-type implants. The sensor n-type collection electrodes are surrounded by pwells, which can host the embedded analog and digital frontend electronics, and deep pwells have been included below the pwells to shield them from the sensor substrate. Three engineering runs have been submitted and the produced wafers have been delivered in 2021, 2022 and 2023, respectively. An

additional p-type implant has been added in the third production run to create an embedded gain layer below the n-type collection electrodes, to enhance the signal through avalanche multiplication.
A selection of the main results obtained from the TCAD simulations and of the most relevant measurements performed on the designed MAPS passive test structures will be presented and discussed in chapter 4. In an analogous way, the experimental results obtained from the characterization of an active sensor designed for brachytherapy, called COBRA, are reported in chapter 5. The calibration of the capacitance included in the internal charge injection circuit of two TJ-Monopix2 MAPS having different substrate types is reported in chapter 6. These sensors represent examples of fully functional and full scale monolithic prototypes realized in a 180 nm TowerJazz CMOS process, that have been characterized using X-rays fluorescence techniques at the SiLab of the University of Bonn. Finally, in the Conclusions section the main results of the research activity are summarized and the possible future spin-offs of the project are presented.

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Chapter 1

Silicon radiation detectors

1.1 Introduction

Solid state radiation detectors and, in particular, silicon radiation detectors represent nowadays the state-of-the-art technology in most radiation imaging applications ranging from medical imaging to high energy physics and space experiments. The low production costs and the excellent performance in terms of energy, position and time resolution are the main advantages provided by solid state detectors, which have replaced the previous technologies in most scientific, medical and space applications. The development of silicon-based radiation detectors takes advantage of the extensive knowledge of the properties of this material acquired in the last century and of the infrastructures and design tools developed for the commercial electronics mass production. The Technology Readiness Level (TRL) of silicon-based devices is on average the highest among the different technologies employed for the commercial electronics and radiation detector production.

An ideal radiation detector material should have a high Signal-to-Noise Ratio (SNR) resulting from an intrinsic low noise

level and, at the same time, a large signal generated from the interaction of the radiation with the detector material. With a low band gap energy many e^--h^+ pairs can be created when a particle or a photon travels through the material and, thus, a large signal can be observed an the detector output. On the other hand, an high band gap energy limits the intrinsic carrier concentration due to thermal generation and, as a consequence, the associated detector dark current and the resulting detector noise lower. Having a band gap energy and a mean ionization energy around 1.12 eV and 3.6 eV, respectively, silicon is an indirect band gap semiconductor well suited for the detection of charged particles as well as photons with wavelengths covering the Electro-Magnetic (EM) spectrum from X-rays to visible and NIR regions. These characteristics make silicon detectors suited for room-temperature operation, except for special applications which require cryogenic cooling e.g. when the devices are exposed to extreme radiation doses. A common solution to reduce the concentration of free charge carriers in the material is to take advantage of the properties of reverse biased p-n junctions. Namely, once depleted, the dark current in the space charge region of a silicon detector reaches a level low enough to enable an efficient and reliable detection of the e^--h^+ pairs resulting from photogeneration or ionization due to an incident charged particle.

1.2 Radiation types and effects

Different mechanisms explain the interaction between different radiation types and nuclear particles with the detector material. As a consequence, different detectors structures have been designed and optimized for the detection of specific radiation types. Detectors for nuclear particles can be subdivided in charged particle detectors and neutron detectors. In the first case, the interaction mechanism changes for heavy charged particle e.g. ions or protons and for light charged particles e.g. positrons or electrons. Both particle types interact through Coulomb force with the orbital electrons of the material but they show different behaviors due to their different mass. For heavy charge particles, depending on the distance of the particle from the electron orbits along its track, the Coulomb interaction can result in the ionization of the detector atoms due to complete removal of an orbital electron or in the excitation of the orbital electrons to an higher energy shell. The particle trajectory through the material remains nearly linear and unaffected from the Coulomb interactions thanks to the high momentum related to its heavy mass. The particle kinetic energy is released continuously along the track and, as a result, e^--h^+ pairs are generated and the particle speed decreases. Due to the statistical nature of the energy loss phenomenon the probability distribution function of the mean energy transfer can be approximated by a Landau dis-

tribution for thin detectors. The mean energy loss per unit of distance for a charge particle traveling inside the detector material is inversely proportional to the square of the particle speed as described by the Bethe-Bloch formula (eq. 1.1), where n represents the electron density inside the material, β is the ratio between the particle speed and the speed of light c, Z is the atomic number of the ionizing particle, m_e is electron rest mass and e is the electron elementary charge and I is the mean ionization energy [1]–[3]. According to this formula and considering the proper corrections needed for low particle energies, the maximum energy loss value is located at the end of the particle track resulting in the characteristic Bragg peak.

$$-\frac{dE}{dx} = \frac{4\pi}{m_e c^2}\frac{nZ^2}{\beta^2}\left(\frac{e^2}{4\pi\epsilon_0}\right)^2\left(\ln\left(\frac{2m_e c^2\beta^2}{I(1-\beta^2)}\right) - \beta^2\right) \tag{1.1}$$

On the contrary, the trajectories of light charged particles inside the material are heavily affected from Coulomb interactions leading to scattering effects, which can affect the reconstruction of the particle track. Light charged particles can lose energy also due to electromagnetic radiation emission like Bremsstrahlung or braking radiation, which is relevant especially for high Z materials.

Due to their neutral charge, which prevents Coulomb interactions with the detector material, neutrons can be detected only in indirect ways by looking at the product of their interac-

tions with specific absorber materials. These materials can be scintillators, which emit photons converting the neutron kinetic energy into electromagnetic radiations, or absorber materials able to release charged particles, for example α particles released form ^{6}Li or ^{10}B, that can be detected through one of the aforementioned mechanisms. Due to the need of a conversion medium, the detection efficiency of neutron detectors is generally lower than the one of a common detector for charged particles because the conversion efficiency of the absorber material is always ≤ 1.
Photons interact with silicon following different mechanisms as a function of their energy ($\mathrm{E_{ph}}$) and thus as a function of their wavelength (λ) according to Plank's relation

$$\mathrm{E_{ph}} = \mathrm{h}\frac{\mathrm{c}}{\lambda}, \tag{1.2}$$

with h the Plank constant and c the speed of light in vacuum. While low energy photons can be transmitted, absorbed, refracted or diffracted in Si, high energy photons are instead mainly absorbed. Since Si is an indirect band gap material, photons with an energy lower than the direct gap energy of 3.6 eV require the presence of a phonon to provide the necessary momentum for the promotion of an electron to the conduction band, generating an $\mathrm{e^-}$-$\mathrm{h^+}$ pair. Depending on the amount of energy transferred from the photon to the detector material three main interactions are more likely to occur. Considering decreasing photon energy levels, these are in the order: pair

production, Compton scattering and photoelectric effect.

When the photon energy is greater than 14 MeV, pair production is the most probable interaction with Si. However, this effect can take place for lower photon energy as well, provided a minimum $E_{ph} \geq 1.022$ MeV. In pair production, an e^{-}-e^{+} pair is generated from the direct interaction of a photon with the nucleus of a detector atom. Both generated particles have a kinetic energy equal to half of the difference between the E_{ph} and the minimum E_{ph} for pair production. The two particles travel inside the detector material in different directions and, as soon as an e^{+} meets an e^{-}, it annihilates releasing two photons in opposite direction having each 511 keV energy.

For lower E_{ph} comprised within 50 keV and 14 MeV Compton scattering becomes the most probable effect. In this case, an electron acquires part of the E_{ph} in the form of kinetic energy and breaks its bound. The scattered photon continues its path inside the material in a different direction and, depending on the remaining E_{ph}, can interact with another weakly bounded electron causing a new Compton scattering or, if the energy is lower than 50 keV, can be finally absorbed by photoelectric effect. The recoil e^{-} travels inside the material generating new e^{-}-h^{+} pairs along its path until it loses all its kinetic energy. Due to the variable amount of energy exchanged during Compton scattering, this effect results in a peculiar shape of the energy spectrum in this photon energy range called Compton continuum.

Finally, for E_{ph} lower than 50 keV photoelectric effect represents the only possible interaction between the incident photon and an electron which, absorbing the photon energy, is released from its atomic shell, usually from the inner Si K-shell. As a consequence, the excited atom will try to restore its energy equilibrium through the transition of an electron of the outer shells to the vacancy in the inner shell and this process causes the characteristic emission of X-rays inside the material. The kinetic energy of the generated electron is equal to the difference between E_{ph} and the electron bond energy and the traveling electron will create e^{-}-h^{+} pairs along its path until it finally stops.

1.3 Radiation detector types

During the years many approaches have been exploited to design radiation detectors able to satisfy the needs of the different application fields. Most of the proposed solutions exploit reverse biased p-n junctions working in photoconductive mode, where the total current collected at the detector electrodes is the flux of charges generated from the interaction of the substrate material with photons or nuclear particles. The PIN diode structure is commonly exploited for the design of particle and spectroscopy detectors due to the advantages provided from a low doped intrinsic silicon bulk in terms of reduction of the applied reverse bias voltage needed to deplete

the detector substrate and in terms of lower defect and trap concentrations, which can lead to the recombination of part of the generated charges, w.r.t. a standard p-n junction having same geometry.

Different strategies have been proposed during the years to design position sensitive silicon detectors, which are employed in applications where the information on the particle incident position and track are required. Most solutions exploit a geometrical approach where the readout electrode is segmented in strips or pixels. The former enable a 1D position resolution with a single detector layer and a 2D position resolution segmenting the electrodes on both the sensor substrate sides in orthogonal directions or, alternatively, employing at least two different strip layers with different orientations. The latter provide a native 2D position resolution with a single detector layer at the cost of a higher number of readout channels. Considering a squared detector structure with the readout electrode segmented in N equal areas, a detector with 2D position sensitivity needs at least $2 \times \mathrm{N}$ readout channels for a strip array, N channels for each strip layer, or N^2 readout channels for a pixellated array to get a comparable spatial resolution. In both cases, depending on the pixel or strip size, the generated charges are likely to be collected by multiple electrodes and, exploiting this information, it is possible to enhance the spatial resolution reaching values lower than the electrode pitch. For a digital binary readout the maximum achievable spatial

resolution is equal to the ratio between the electrode pitch and $\sqrt{12}$. Instead, for an analog readout the spatial resolution can be further improved exploiting the information given by the centroid of the collected charge spatial distribution.
Silicon Drift Detectors (SDD) follow instead a different approach, where the position sensitivity is provided by a combination of the temporal information contained in the acquired signals and the geometry of the collection electrode. In these peculiar sensors, first devised from Gatti and Rehak in 1984 [4], a drift electric field orthogonal to the detector substrate thickness is exploited to move the charges generated inside the depleted active volume to a small collection electrode. The drift time is function of the distance from the collection electrode to the point where the charges have been generated. Therefore, computing the electron drift velocity through eq. 1.3, where E represents the existing electric field and μ_{n} is the electron mobility, it is possible to get information on the interaction position by looking at the signal temporal evolution.

$$\mathrm{v_d} = -\mu_{\mathrm{n}}\mathrm{E} \tag{1.3}$$

Considering a segmented collection electrode with known geometry, the previous information is able to guarantee the 2D reconstruction of the particle or photon incident position. Moreover, the possibility to reduce the collection electrode dimensions w.r.t. a standard PIN diode results in a excellent signal-to-noise ratio (SNR), which makes SDD one of the best

solutions for spectroscopy applications still today [5].

Charge Coupled Devices (CCD) represents a third detector category, historically employed in imaging application mainly in the visible region. These devices have a peculiar structure with the frontside layout segmented as an array of pixels made of MOS gates or p-n junctions. Employing a clocked switching sequence to the voltages needed to remove the potential barrier between the wells, where the generated charges are confined, it is possible to get information on the radiation interaction point simply counting the number of clock cycles needed to collect the generated charges at the end of the pixel columns. This readout scheme provides a native 1D position resolution that can be turned into a 2D position resolution by shifting the charges in two orthogonal directions or by segmenting the readout contact so that each column can be read independently.

Another possible way to categorize silicon radiation detectors is to distinguish between hybrid sensors, where the electronics and the sensing elements are realized on different silicon substrates, and monolithic sensors, where the electronics and the sensor are instead embedded on the same silicon substrate. The first approach represented the state-of-the-art technology for decades and most X-rays or IR sensors and almost every particle detector, e.g. CMS, ATLAS, LHCb, include at least a layer of hybrid sensors [6]–[10]. The chance of optimizing independently the electronics and the sensing element is the

main advantage of this technology. On the other hand, the need of connecting the two different substrates through the expensive and yield critical bump bonding process limits the potential of this sensors.

Monolithic active pixel sensors can represent a cost effective alternative to hybrid sensors thanks to the possibility to exploit the existing commercial CMOS production processes for the sensor fabrication [11]–[13]. The price to pay for this technology is the trade off in the sensor and electronics optimization. Namely, there exist contrasting requirements in terms of silicon substrate resistivity in order to reach the best performance for both the electronics and the sensing element. Moreover, a second thing to take into account is the need to deplete the substrate volume applying in many cases a high voltage bias to the sensor substrate. This voltage can be in the order of tens or hundreds of V depending on the substrate thickness and resistivity. Since the transistors of commercial CMOS electronics work usually at 1.2V or 3.3V, special solutions have been designed in order to shield the electronics and decouple it from the electrode where the bias voltage is applied. Monolithic sensors with depleted substrate thicknesses up to several hundreds of micrometers have been demonstrated in [14]–[16]. A third challenge is related to the maximization of the detector fill factor due to the unavoidable amount of space occupied from the embedded electronics, which could lead to a significant decrease in the chip total

active area.

The existing detector technologies can be also subdivided on the basis of the charge collection mechanism that is mainly exploited. In the so-called fully depleted sensors, the applied reverse bias voltage, called full depletion voltage, is high enough so that the space charge region covers the whole detector active volume. As a consequence, the generated charges are collected by drift and the resulting signals show fast collection dynamics with most of the charge collected within tens of ns or less [17]–[21]. The TJ-Monopix, the LF-Monopix and the ARCADIA Main Demonstrator chips represent some examples of fully depleted MAPS, which are able to collect the generated charges by drift mechanism working in fully depletion condition [22]–[24]. On the contrary, when the applied reverse voltage is lower than the full depletion voltage, the charge collection speed is limited from the slower charge transport by diffusion in the non-depleted sensor volume. An example of this sensor type is the ALPIDE chip that has been selected for the ALICE ITS (Inner Tracking System) upgrade to cover with monolithic pixels a total area around 10 m^2 [25].

Finally, it is possible to distinguish between detectors with or without internal gain. Detectors with internal gain take advantage of the impact ionization mechanism leading to the avalanche multiplication of the charge carriers inside the detector substrate. The avalanche multiplication in an avalanche photodiode (APD) can take place when the electric field in-

side the detector material exceeds locally a threshold value. This value should be high enough to guarantee that the accelerated carrier has the energy needed to create a new e^{-}-h^{+} pair colliding with an orbital electron and breaking its bound. The charges generated from the first impact ionization are accelerated from the electric field as well and undergo the same process generating a new couple of e^{-}-h^{+} pairs, leading to a chain reaction for the charge multiplication. According to [26], the minimum electric field needed to trigger the avalanche multiplication is in the order of $2 - 5 \times 10^5$ [V/cm] for silicon detectors. The ionization rates of electrons and holes in silicon, representing the number of e^{-}-h^{+} pairs created per μm traveled in the high field region, are both dependent on the electric field intensity, with the former showing an higher value than the latter considering the same electric field value. The gain provided by an avalanche detector can vary from a few units or tens of units to several million units. Namely, there are different operating conditions for radiation detectors working in avalanche mode. If the maximum gain value is limited in the order of some tens, corresponding to the nearly linear avalanche multiplication region, which is associated to applied bias voltages lower than the breakdown voltage, the avalanche detectors are called Low Gain Avalanche Diodes (LGADs) [27], [28]. Instead, when the applied bias voltage exceeds the breakdown voltage, an APD works in Geiger-mode condition, reaching high gain values that tend ideally to infin-

ity. APDs working in Geiger-mode are commonly called Single Photon Avalanche Diodes (SPADs) and are usually employed in applications which require extreme sensitivity like single photon counting in the measurements of fluorescence lifetimes. Silicon Photon Multipliers (SiPMs) represent a special type of SPAD with a structure segmented in an array of micro-SPAD connected in parallel that can be used to determine the number of photons incident on the SPAD area [29]. In SiPMs, the number of photons incident on the SiPM matrix can be determined from the total collected current that is proportional to the number of micro-SPADs that are triggered from photons incident on their areas.

During the last two decades several projects were committed with the development of APD for light detection employing standard CMOS commercial technologies [28], [30]–[32]. Taking inspiration from this concept, in the last few years there were attempts to integrate a gain layer inside a MAPS structure designed for radiation imaging in order to take advantage of the characteristics of both technological solutions obtaining a cost effective detector with integrated electronics and gain amplification [33], [34]. This approach is considered a promising candidate for the new generation of sensors that will be employed in timing applications e.g. 4D particle track reconstruction in particle collider experiments.

1.4 Detectors Figures of Merit (FoM)

Looking at the characteristic parameters and FoM of a device represents a common way to evaluate its performance in comparison to the existing alternatives. Therefore, some common metrics used to describe the performance of a silicon detector will be presented in this section. As previously mentioned, reaching a low Equivalent Noise Charge (ENC) or equivalently a high SNR, larger than 10 for most applications, is commonly one of the main targets when designing a new device. The SNR can be expressed through eq. 1.4 as the ratio between the voltage amplitude $\mathrm{V_{out}}$ at the detector output, once that the signal has been amplified and conditioned in the preamplifier and shaping amplifier stages, and the related Root Mean Squared (RMS) output voltage noise $\mathrm{v_{n_{RMS}}}$.

$$\frac{\mathrm{S}}{\mathrm{N}} = \sqrt{\frac{\mathrm{V_{out}^2}}{\mathrm{v_{n_{RMS}}^2}}} \tag{1.4}$$

Considering the signal chain of a simplified detector system that, according to [35]–[37], can be schematically represented by a sensing element, a preamplifier and a shaper, the output voltage amplitude can be computed starting from the collected charge Q, obtained by integrating the detector signal $\mathrm{I_{det}}$ for a given integration time $\mathrm{t_{int}}$.

$$\mathrm{Q(t)} = \int_0^{\mathrm{t_{int}}} \mathrm{I_{det}(t)\,dt} \tag{1.5}$$

Most of the detector front-end designs exploit a charge sensitive amplifier (CSA) as input stage, which can be schematically represented as an active integrator, able to provide an output voltage $V_{pre_{OUT}}$ equal to the ratio between the charge at the preamplifier input Q_{IN} and the preamplifier feedback capacitance C_{fb}. Exceptions are represented from the ALPIDE and ARCADIA front-end architectures, where the signal is integrated on the detector input capacitance and the resulting output voltage is fed to a voltage amplifier.

In the following equations, the charge at the CSA input Q_{IN} is assumed to be equal to the total charge collected from the detector Q under the hypothesis that the effective capacitance at the preamplifier input equal to the product of C_{fb} with the premplifier gain is much larger than the detector capacitance [36].

$$V_{pre_{OUT}} = \frac{Q_{IN}}{C_{fb}} = Q_{IN} \times A_{pre} \tag{1.6}$$

The previous equation describes the behavior of an ideal charge sensitive preamplifier having an infinite feedback resistor R_{fb}, which makes its contribution negligible in the gain computation, and therefore represents an approximation of the transfer function able to describe the actual behavior of a real CSA.

Considering the shaper transfer function H_{shaper}, the output voltage at the end of the signal chain V_{OUT} can be computed

through eq. 1.7.

$$V_{OUT} = V_{pre_{OUT}} \times H_{shaper} = \frac{Q_{IN}}{C_{fb}} \times H_{shaper} \tag{1.7}$$

The RMS output voltage noise $v_{n_{RMS}}$ is usually treated as the sum of three different noise contributions which are the 1/f noise, the parallel noise and the series noise, respectively. The 1/f noise results from the trapping and detrapping mechanism of the charge carriers and is usually related to the presence of defects at the surface of the MOSFETs which are used in the different amplification stages. Considering its frequency content through the Power Spectral Density (PSD), this noise contribution can be expressed using eq. 1.8,

$$v_{1/f_{RMS}} = \sqrt{\frac{1}{2\pi} \int_{-\infty}^{+\infty} S_{1/f}(\omega)\, A_{pre}^2\, |H_{shaper}(j\omega)|^2\, d\omega} \tag{1.8}$$

where $S_{1/f}(\omega)$ is the PSD of the 1/f noise and A_f is the 1/f noise coefficient

$$S_{1/f}(\omega) = \frac{A_f}{\omega}\,. \tag{1.9}$$

In an analogous way, the parallel noise contribution $v_{I_{RMS}}$ can be computed from its PSD S_I using eq. 1.10.

$$v_{I_{RMS}} = \sqrt{\frac{1}{2\pi} \int_{-\infty}^{+\infty} \frac{S_I}{\omega^2\, C_T^2}\, A_{pre}^2\, |H_{shaper}(j\omega)|^2\, d\omega} \tag{1.10}$$

The parallel noise contribution can be seen as a white current noise source in parallel with the amplifier input, having an equivalent total leakage current $\mathrm{I_L}$. This noise component, commonly called shot noise, is related to the charge quantization, to the dielectric losses and to the presence of the feedback resistance in the charge preamplifier [38] and its PSD is usually expressed as

$$\mathrm{S_I} = \mathrm{q\, I_L} + \mathrm{b_f}\, \omega. \tag{1.11}$$

Finally, the third noise contribution represents the noise component in series with respect to the preamplifier input $\mathrm{v_{V_{RMS}}}$, that can be modeled as a series voltage noise source.

$$\mathrm{v_{V_{RMS}}} = \sqrt{\frac{1}{2\pi}\int_{-\infty}^{+\infty} \mathrm{S_V\, A_{pre}^2\, |H_{shaper}(j\omega)|^2\ d}\omega} \tag{1.12}$$

The PSD of $\mathrm{v_{V_{RMS}}}$ is inversely proportional to the transconductance of the transistor at the preamplifier input and directly proportional to the temperature and to an empirical coefficient α that depends on the device characteristics and belongs to the range [0.7, 1] for MOSFETs or to the range [0.5, 0.7] for JFETs [38], [39].

$$\mathrm{S_V} = \alpha \frac{\mathrm{2kT}}{\mathrm{g_m}}\,. \tag{1.13}$$

The Equivalent Noise Charge (ENC) can be alternatively used to express the noise performance of a detector. Namely, it is

strictly related to the SNR since it is defined as the minimum number of charges that need to be collected in order to guarantee an SNR equal to 1.

Considering the hypothesis of the abrupt p-n junction model, the extent of the space charge region (SCR) in the detector substrate can be easily estimated using eq. 1.14,

$$d = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(\Psi_0 - V_{Bias})}\,, \tag{1.14}$$

where Ψ_0 represents the built-in potential and N_A and N_D are the concentrations of ionized acceptors and ionized donors, respectively.

The thickness of the depleted region is inversely proportional to the detector capacitance 1.15 and thus, since the detector capacitance influences both the noise and the charge collection dynamics, the previous equation is commonly employed to have a first indication of the voltage bias V_{bias} to be applied to guarantee the optimal depletion depth.

$$C_{det} = \frac{\epsilon_s}{d} \tag{1.15}$$

For spectroscopy application the detector energy resolution is another fundamental metric since this application requires to precisely measure the energy spectrum of an incident radiation. The detector ability to discriminate between different radiations with similar energies represents its energy resolution. The output of an ideal spectroscopy detector should

provide a single impulse on the charge histogram, if the incident radiation is produced from a mono-energetic source. However, due to their statistical nature, the generation of e^{-}-h^{+} pairs inside the detector material and the electronics noise cause fluctuations in the amplified signals and, as a consequence, the resulting output spectrum of a spectroscopy detector shows a distribution of events around the peak mean value also for a mono-energetic radiation source having a specific energy (E). In X-ray spectroscopy, the statistical variation of the generated e^{-}-h^{+} pairs can be described using a Poisson statistics with a correction term called Fano factor (F) that should be taken into account to match the experimental results. Usually, the intrinsic energy resolution is defined as the Full Width at Half Maximum ($\mathrm{FWHM_{lb}}$) of the Gaussian shape representing the detector line broadening. Therefore, considering its standard deviation σ_{lb}, that is proportional to the square root of the average number of generated e^{-}-h^{+} pairs N and the needed correction term F, the energy resolution can be expressed with eq. 1.16, where E_i is the ionization energy [2].

$$\mathrm{FWHM_{lb}} = 2.35 \cdot \sigma_{\mathrm{lb}} = \frac{\mathrm{dE}}{\mathrm{E}} \cdot \mathrm{N} \cdot \sigma_{\mathrm{lb}} \tag{1.16}$$

with

$$\frac{\mathrm{dE}}{\mathrm{E}} = 2.35 \cdot \sqrt{\mathrm{F}\frac{\mathrm{E_i}}{\mathrm{E}}} \tag{1.17}$$

In addition to this component, the detector energy resolution is affected from the noise associated to the detector electronics and the charge collection efficiency as well. Therefore, the actual FWHM corresponding to its energy resolution can be computed as the quadrature sum of the FWHM associated to the different noise contributions.

Talking about photodetectors, the quantum efficiency represents another relevant FoM, describing the ratio between the photo-generated electrons and the number of photons incident on the device. The counting efficiency can be considered the equivalent FoM for particle detectors, representing the ratio between the number of incident particles revealed by the detector and the number of incident particle emitted by the radioactive source. In photodetectors for visible, IR and NUV radiation, eq. 1.18 is commonly employed to estimate the quantum efficiency η as a function of the detector responsivity R, which is defined as the ratio between the photo-generated current (I_{ph}) and the incident optical power (P_{opt}). The remaining terms in the equation represent the photon wavelength λ, the speed of light c, the electron elemental charge q and the Plank constant h.

$$\eta = \frac{\frac{I_{ph}}{q}}{\frac{P_{opt}\lambda}{hc}} = R\frac{hc}{\lambda q} \tag{1.18}$$

The quantum efficiency depends on different factors that are influenced by the detector design, which are the transmis-

sion efficiency, the absorption efficiency and the collection efficiency, respectively. The transmission efficiency measures the amount of photons that are able to reach the detector active volume, crossing the passivation and Anti Reflective Coating (ARC) layers that are usually included on top of the detector optical window surface. The fraction of photons that are absorbed in the detector material represents the absorption efficiency of the detector. Finally, the collection efficiency can be measured as the fraction of photo-generated e^{-}-h^{+} pairs that are collected at the detector electrodes and, therefore, takes into account the recombination and trapping mechanism occurring inside the detector material.
The dark current I_{dark} in a reverse biased p-n junction can be computed as the sum of two different contributions related to the thermal generation in the depleted volume J_{gen} and to the diffusion of the free carriers coming from the neutral regions in the surroundings J_{diff}. Usually, the major contribution comes from the thermal generation for silicon detectors and can be estimated using eq. 1.19, where d is the width of the detector depletion region, n_i is the intrinsic concentration of free carriers and τ_0 is the mean carrier lifetime.

$$J_{gen} = qd\frac{n_i}{2\tau_0} \tag{1.19}$$

Minimizing this current contribution is essential to limit both the noise floor of the detector and increase its SNR as well as to decrease the static power consumption of the device and,

thus, avoid possible thermal heating issues and fulfill the requirement related to the finite energy availability typical of space applications.

Talking about detectors for timing applications, the charge collection time τ_{cc} and the timing resolution σ_t become the most relevant FoM. The time constant of the detector can be estimated from eq. 1.20 as the quadrature sum of three different contributions τ_{drift}, τ_{diff} and τ_{RC}.

$$\tau_{cc} = \sqrt{\tau_{drift}^2 + \tau_{diff}^2 + \tau_{RC}} \tag{1.20}$$

τ_{drift} represents the time needed from the generated charges to travel in the depletion region, which can be computed as a first approximation using eq. 1.21.

$$\tau_{drift} = \frac{d}{v_d} = \frac{W^2}{\mu V_{Bias}} \geq \frac{d}{v_{d_{sat}}} \tag{1.21}$$

The diffusion time of the charges generated in the non depleted region can be instead estimated from eq. 1.22, where D stands for the diffusion coefficient. τ_{diff} usually represents the main contribution responsible for the slow components in the signal dynamics associated to the signal tail.

$$\tau_{diff} = \frac{d_{undepleted}^2}{2D} \tag{1.22}$$

The last component is related the RC time constant associated to the detector capacitance C_{det} and to the load resistance R_L

and can be computed using eq. 1.23.

$$\tau_{\mathrm{RC}} = 2.2\mathrm{R_L C_{det}} \tag{1.23}$$

The timing resolution of a detector becomes fundamental in specific applications e.g. 4D particle track reconstruction and Time of Flight (ToF) measurements, which require pileup rejection [40]. It depends both on the intrinsic timing characteristics of the sensors and on the time jitter associated to the readout electronics. In particular, the first term takes into account the fluctuations in the signal shape or, if present, in the detector gain as well as the contribution related to the unavoidable Landau fluctuations in the number of generated charges [41]. Common strategies to enhance the timing resolution of a silicon detector include the use of thin detector substrates in the order of few tens of micrometers trying at the same time to keep the pixel capacitance as low as possible to maintain a favorable SNR. However, thinner sensor substrates correspond to a lower number of generated charges leading to lower SNR. Decreasing the pixel dimension can be a strategy to decrease the $\mathrm{C_{det}}$ value but, at the same time, it leads to non-uniform weighting field and weighting potential resulting in a degraded charge collection speed. Attempts have been made to maximize the timing performance of MAPS with small electrodes for example using peculiar pixel layouts like in the Fastpix project [42]. Considering an internal amplification obtained by embedding a gain layer in the detector

can be a possible solution to overcome the aforementioned limitation in terms of SNR given by the usage of thin substrates. Namely, some of the best results in terms of timing resolution obtained so far have been demonstrated by using LGADs [27], [40]. According to [43] the timing resolution of an LGAD can be computed as the quadrature sum of three terms representing the jitter, the time walk and the TDC binning (eq. 1.24).

$$\sigma_{\mathrm{t}} = \sqrt{\sigma_{\mathrm{j}}^2 + \sigma_{\mathrm{tw}}^2 + \sigma_{\mathrm{TDC}}^2} \tag{1.24}$$

Finally, for detector with internal amplification the provided gain value is one of the most relevant parameters. Usually, the detector gain can be evaluated as the ratio between the signal or the amount of charges collected from a device with internal gain layer and the corresponding one collected from a device without gain, considering the same active volume and the same illumination or irradiation conditions. Due to its relation with the electric field, the gain varies as a consequence of the applied voltage bias. TCAD simulations and experimental results have demonstrated the dependence of the LGAD gain on the amount of generated charges. Namely, the space charge effects related to higher carrier concentrations lead to a local weakening of the electric field peak in correspondence of the gain layer and thus to a decrease in the avalanche multiplication [44]. A similar effect can be noticed considering increasing radiation damage levels, which lead to a decrease in the gain

value after the sensor irradiation in the same test conditions [45]–[47].

1.5 State-of-the-Art of MAPS

The scientific community is always at the search of novel solutions able to guarantee better detector performance in terms of radiation hardness, power consumption and collection dynamics and, at the same time, to decrease the fabrication costs exploiting the existing commercial electronics production processes. To this end, different collaborations have been involved with the development of MAPS based on different commercial CMOS processes with technology node size ranging from 350 nm [48] to the most advanced chip designed in a 65 nm CMOS technology [49]–[51]. Thanks to their growing TRL and their advantages in terms of production cost and bonding easiness, MAPS have started to replace hybrid pixels that have represented the state-of-the-art detectors in most radiation imaging applications for decades.

The most known examples of a MAPS currently employed in a large Physics experiment is the ALPIDE chip developed for the ALICE upgrade exploiting the 180 nm CMOS Imaging Sensor process of TowerJazz [25]. The ALPIDE modules are mounted in the ALICE detector Inner Tracking System covering a total area in the order of 10 m^2. Figure 1.5.1 represents a schematic cross section of an ALPIDE pixel, where the main

sensor layout characteristics are depicted.

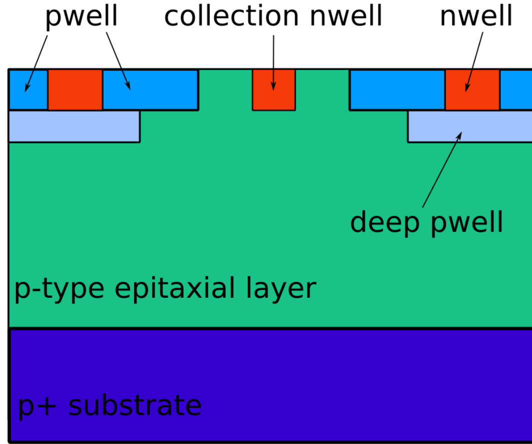


Figure 1.5.1: Schematic cross-section of an ALPIDE pixel.

The main advantages of this sensor are represented by the possibility to embed a full CMOS electronics, hosted in the front-side deep pwell implants, which shield the electronics from the high resistivity p-type epitaxial layer; by the lower production costs in comparison to the standard hybrid pixels and by its excellent spatial resolution in the order of 10 μm. Moreover, its small collection electrode size enable to reach a low C_{det} ($\simeq$ 2.5 fF @ -6V), which guarantees an excellent SNR. The embedded frontend electronics has been designed to be low power, reaching an overall power consumption in the order of less than 40 mW/cm^2. The main limitation of this device is the use of the diffusion mechanism to collect the charges

generated in the thin epitaxial layer, which leads to slow collection times and, as a result, this device is forced to operate at maximum rates of few MHz. The second relevant issue is the limited radiation hardness of this sensor concept, which is able to withstand a maximum Non-Ionizing Energy Loss (NIEL) fluence only slightly higher than 10^{13} n_{eq}/cm^2 with 1 MeV energy or a Total Ionizing Dose (TID) of 2700 krad [52].

The TJ-Monopix1 and TJ-Monopix2 represent CMOS sensors designed for the upgrade of the ATLAS ITS that can be seen as an evolution of the ALPIDE sensor since these chips are realized on the basis of the same 180 nm TowerJazz production process. In order to work in full depletion conditions, the TJ-Monopix chips have been designed employing a modified 180 nm TowerJazz Sensor Imaging process, which includes a low doped n-type layer under the pixel area [18], [53], [54]. This low doped layer enables to reach the full depletion of the p-type epitaxial substrate applying a small negative voltage bias to the sensor substrate in the order of -20V. A schematic cross section of this sensor concept is reported in Figure 1.5.2.

A full CMOS electronics is embedded in the frontside pwells and nwells, which are shielded from deep pwells in order to avoid competitive charge collection from the electronics nwells. Collecting the generated charges by drift, these devices are able to operate at much higher rates w.r.t. the ALPIDE chip. Namely, a detector operating frequency of 40 MHz can be achieved from these chips meeting the requirement set for the

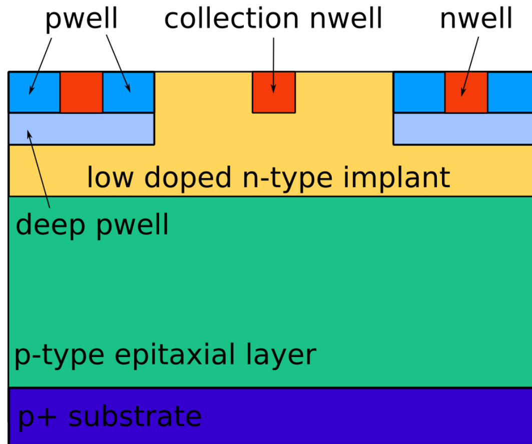


Figure 1.5.2: Schematic cross-section of a TJ-Monopix chip having p-type epitaxial layer.

upgrade of the ATLAS ITS [55]. Moreover, the experimental results proved the radiation hardness of these sensor concepts, which proved a detection efficiency of 98.6% after an irradiation with a neutron fluence up to $10^{15} n_{eq}/cm^2$ for a TJ-Monopix2 chip with a high resistivity Czochralski substrate having 300 μm thickness [23]. However, as a consequence of the layout with a small collection electrode size and due to the presence of the frontside deep pweel, the charge collection results slower at the pixel borders which feature low electric field regions. Special design solutions have been implemented to solve this issue including an additional p-implant below the deep pwell or a small gap in the n-type epitaxial layer between

the collection electrodes to reshape the electric field lines at the pixel borders (see Figure 6.0.1).
The LF-Monopix1 and LF-Monopix2 chips have been instead fabricated exploiting the 150 nm CMOS production process of LFoundry [56] and the sensor layouts have been designed following an alternative approach based on the sensor concept proposed by Perić [48]. As can be seen in Figure 1.5.3, in these chips the nwells and the pwells, where the electronics is embedded, are realized inside a large nwell, which works also as collection electrode.

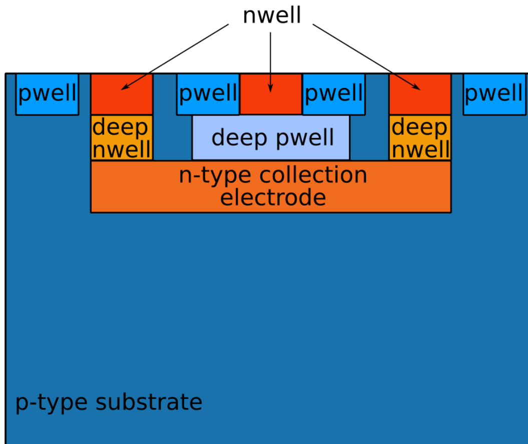


Figure 1.5.3: Schematic cross-section of a LF-Monopix pixel.

As a result, the layout of the sensors guarantees a larger fill factor and a more uniform electric field inside the sensor p-type substrate. At the same time, the design proved to guar-

antee an excellent radiation hardness in terms of TID and NIEL and the depletion of sensor substrates with thickness up to several hundreds of micrometers has been achieved. In particular, irradiation studies have been performed on the LF-Monopix1 chip using an x-ray tube and the JSI TRIGA reactor to reach a TID of 100 Mrad and a neutron fluence of $10^{15} n_{eq}/cm^2$, respectively. The experimental results showed an increase in the detector noise lower than 25% as a consequence of the TID and a hit detection efficiency higher than 99% for the considered NIEL [57]. The main drawbacks of this approach consist of the large sensor capacitance, which is related to the large collection electrode size, and of the possible interaction between the sensor and the embedded electronics. Moreover, the significantly larger pixel size leads to a worse position resolution w.r.t. the TJ-Monopix chips, which can be potentially employed in the same applications.

The Silicon On Insulator technology represents a third alternative, where two different substrates containing the sensing element and the frontend electronics are connected through a buried oxide layer [58]. Usually, the sensing element and the electronics are realized on a thick high resistivity silicon substrate and on a thin microelectronics grade silicon layer, respectively. This enables the independent optimization of both the sensor and the electronics and gives to the designers the opportunity to change the high resistivity substrate thickness depending on the requirements of the considered application,

enabling the depletion of regions with thickness up to 500 μm [59]. On the other hand, this sensor design implies some issues related to the accumulation of positive charges in the buried oxide after irradiation. According to [60] this effect becomes relevant for TID larger than a few hundred krad. To mitigate this effect, a thin silicon buried layer is included below the buried oxide layer and a second buried oxide layer is created below this additional silicon layer. Then, a voltage bias is applied to the buried Si layer in order to compensate the effect of the accumulated charges. This modification characterizes the sensors implemented in the Double-SOI technology, that is schematically represented in Figure 1.5.4.

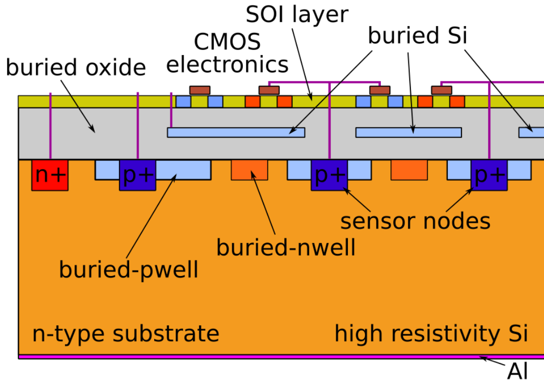


Figure 1.5.4: Schematic cross-section of a Double-SOI sensor.

Moreover, a buried p-well is needed to shield the CMOS electronics due to the presence of a high voltage bias applied to the high resistivity substrate that can affect the threshold of the

CMOS electronics and thus have a detrimental effect on the electronics performance. The need of these additional modifications to the standard CMOS production processes makes having cost effective production on a large scale difficult and, as a consequence, makes this approach less convenient from the economic point of view and similar to the expensive special technologies used to design the standard hybrid pixels.

A selection of relevant Figures of Merit has been reported in Table 1.1 to provide a comparison of the presented MAPS technologies. As shown in the Table, the size of the pixels included in the ARCADIA Main Demonstrator (MD) chip is in line with the ones employed in the most advanced MAPS prototypes. The 110 nm technology node of the CMOS electronics embedded in the MD chip is the smallest among the considered chips and one of the most advanced implemented in a large area MAPS prototype so far. The ARCADIA technology offers a wide range of active substrate thickness that can be properly fully depleted resulting in a versatile sensor that is suitable for several different applications. Exploiting the drift mechanism to collect the charges generated in the depleted active volume the collection time of the ARCADIA sensors ranges from a ten to about a hundred of nanoseconds depending on the considered substrate thickness. The MD chip has been designed to guarantee a radiation hardness in terms of TID and NIEL that is comparable with the ones of the ALPIDE and Double-SOI chips and, therefore, much lower

than the ones achieved by the TJ- and LF-Monopix2 chips. At the same time, the maximum event rate that the MD chip can withstand in the order of 100 MHz/cm^2 is slightly less than the rate guaranteed by the TJ- and LF-Monopix2 chips. According to the literature, the ALPIDE chip and the derived TJ-Monopix2 chip show exceptional performance in term of noise with a measured ENC lower than 10 e^- and, thus, represent currently the references used as term of comparison to evaluate the noise level of the other MAPS detectors.

Table 1.1: State-of-the-Art MAPS main characteristics

	ALPIDE [25], [52], [61]	TJ-Monopix2 [23], [62]	LF-Monopix2 [23], [57]	Double-SOI [58], [59]	ARCADIA MD [24], [63], [64]
Pixel Size [μm]	28	33	50×150	18	25
CMOS Tech. [nm]	180	180	150	200	110
t_{act} [μm]	~ 25	~ 25 or ~ 300	$100 - 750$	~ 300	$48 - 500$
Coll. Time [ns]	> 20	< 10	< 25	~ 150	$\sim 10 - 100$
TID [Mrad]	2.7	100	> 100	~ 10	~ 10
NIEL [$1\,\mathrm{MeV} \cdot \frac{n_{eq}}{cm^2}$]	$\sim 10^{13}$	$\sim 10^{15}$	$\sim 10^{15}$	-	$\sim 10^{13}$
Event Rate $\left[\frac{MHz}{cm^2}\right]$	< 10	> 100	> 100	-	~ 100
ENC [e^-]	< 10	< 10	~ 100	-	tbd

Chapter 2

The ARCADIA project

The ARCADIA (Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays) project targeted the development of a novel platform for the design and fabrication of MAPS based on the commercial 110 nm CMOS production process of LFoundry [63]. The project has been founded by the Istituto Nazionale di Fisica Nucleare (INFN) - CSN5 and the ARCADIA collaboration included working groups from different INFN sections and Italian Universities. A detailed description of the contribution to the project provided by the different working groups can be found in [63], [65]. Exploiting the experience and the knowledge acquired with the previous SEED (Sensor with Embedded Electronics Development) project, the ARCADIA collaboration was able to deliver three different production runs, that have been designed, fabricated and tested between 2020 and 2023. The Sensor Design working group, including the TIFPA-UNITN and the INFN Torino groups, was in charge of the device electrical simulations used to design the sensing elements of the different ARCADIA active chips and of the passive test structures. Moreover, the Trento group had the task to perform the electrical and op-

tical characterization of the passive test structures and the optical and functional characterization of the active COBRA chips.

The main derivable of the project was a pixelated monolithic CMOS sensor, realized in a commercial 110 nm CMOS technology with 1.2 V transistors, able to work in full depletion condition and thus to exploit the drift mechanism for the collection of the generated charges. The readout electronics is based on a scalable and modular architecture design and is able to operate in low power mode in order to meet the power consumption requirements needed in the low event rate and low power environment of space applications. Figure 2.0.1 shows the pixel layout, that is based on a small collection electrode realized with an n-type implant. A pwell and a deep pwell surround the n-type sensor and can host the embedded frontend electronics, shielding it from the sensor substrate.

The small dimension of the collection electrode and the full depletion of the substrate result in a small pixel capacitance value, which can potentially lead to an excellent SNR. Different nominal substrate thicknesses ranging from 48 μm up to 200 μm have been included in the produced wafers and the possibility to fully deplete substrates with 300 μm thickness was experimentally proved measuring the IV characteristics of the test structures of the SEED project [16], [24]. While thinner substrates are required to speed up the charge collection and to maximize the timing performance of the device,

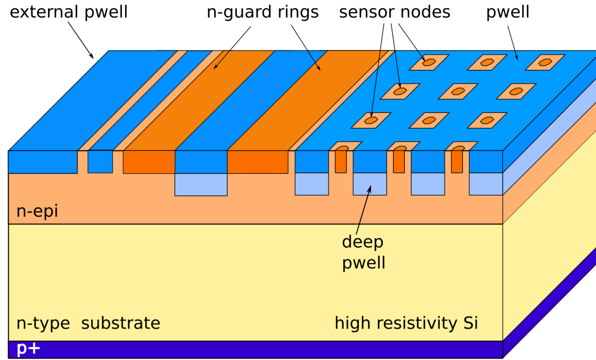


Figure 2.0.1: Schematic representation of a pixel array.

thicker substrates can provide a higher amount of generated charges when MIPs are crossing the detector and an enhanced efficiency which is required for the detection of X-rays with energies in the range from 1 to 20 keV. Wafers with two different substrate types and three different nominal thicknesses have been employed for the sensor production in the three engineering runs. Wafers characterized by an active region with a nominal thickness of 48 μm were realized starting from p^+ substrates, where a n-type epitaxial layer and a second n-type epitaxial layer with higher doping concentration were grown in sequence to create the active volume. Using high resistivity n-type substrates, sensors with two different active thicknesses equal to 100 and 200 μm were realized. The former have a homogeneous p^+ implantation on the backside surface created by laser annealing which forms the device pn junction, the

latter needed a dedicated backside lithographic step in order to create the backside p$^+$ implants corresponding to the diode pn junction and the surrounding floating guard rings. The presence of the floating guard rings avoids issues related to the breakdown at the junction borders and thus enable the application of the negative voltage bias needed to deplete the substrate from the backside p-type contact. Namely, the guard rings lower the electric field peak located in correspondence of the junction border, reducing the gradients in the electrostatic potential.

2.1 Main Demonstrator and active chips

The wafer reticle (Figure 2.1.1) included several active detectors with embedded electronics as well as a group of passive test structures used to characterize the production process and arrays of pixels and strips with different pitch and layouts so as to evaluate their performance independently from the CMOS electronics.

Although the wafer reticle has been modified in the different engineering runs, two different versions of the main demonstrator chip with different electronics design were always present inside the reticle. The ARCADIA Main Demonstrator (MD) chip has been designed with an active matrix composed of a 512 $\times$ 512 pixels array with 25 μm pixel pitch. This corresponds to an active area of the pixel matrix equal

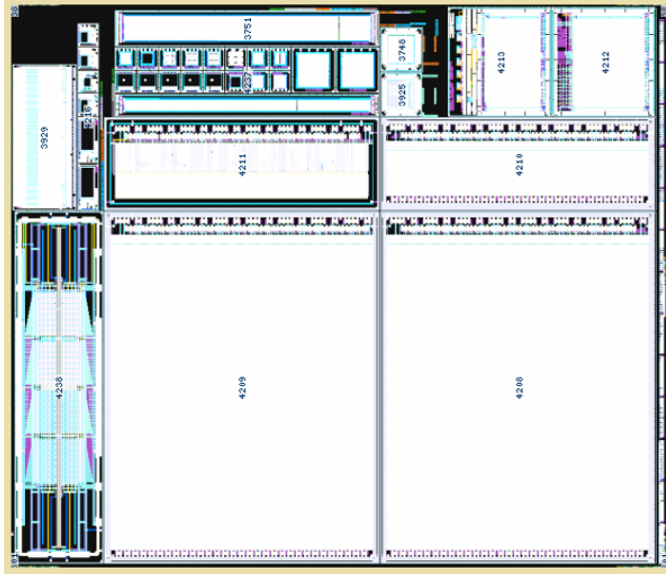


Figure 2.1.1: ARCADIA wafer reticle floorplan (Courtesy of Marco Mandurrino).

to 1.28×1.28 cm^2 with an integrated custom low power frontend electronics. The electronics has been designed to ensure the scalability of the sensor matrix up to a maximum size of 2048×2048 pixels. An analog front-end, a comparator and a digital readout circuitry have been included in the pixel and, in order to minimize the power consumption, a clock-less matrix with an event driven readout scheme has been envisaged. The chip is organized in 16 Sectors composed of 32×512 pixels with a dedicated serialiser and a custom LVDS transceiver for each Sector. Each Sector contains 16 Double Columns made of

2×512 pixels, that can be further subdivided in 16 2×32 pixel Cores [66]. The chip can work selecting between two different electronics operating Modes called High Rate Mode, which enables to cope with a maximum event rate of 100 MHz/cm^2 targeting a maximum power consumption of 20 mW/cm^2, and Low Rate Mode, which should further reduce the maximum power consumption to about 5 mW/cm^2 by switching off 15 out of 16 Sector serialisers and LVDS transceivers [67]. To ensure the lower power consumption, the second Mode implies a reduction of the maximum event rate that can be detected and processed from the chip to 10 MHz/cm^2. Since the design of a full-custom electronics from scratch is extremely challenging, a few small issues have been noticed in the proper functionality of the MD chip produced in the first and second engineering run. As a consequence, the origins of these problems have been deeply investigated, detected and solved leading to a fully functional chip in the third production run that is currently under test (Figure 2.1.2).

Apart from the MD, several different active chips have been included in the wafer reticle of the different engineering runs. Two Mini Demonstrator (MiniD) chips having the same periphery and frontend electronics of the MD but a smaller pixel matrix have been produced as a backup chip, in case of critical problems in the MD chip design to still provide a chance to test the in-pixel and periphery electronics.

A group of 32 active microstrips with integrated electron-

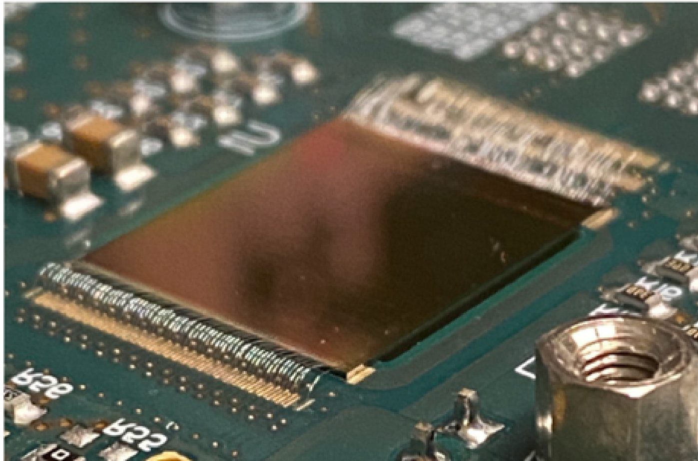


Figure 2.1.2: ARCADIA Main Demonstrator picture [68].

ics was contained in the ASTRA-VI (Adaptable Space sTrip Readout ASIC) chip, which covers a total area of 16×4 mm^2. Each strip column is composed of 2×256 pixel with 50 μm pitch connected in parallel and is read out by a dedicated channel. The chip architecture allows to select between two different values for the channel gain and two different readout modes i.e. analog or digital. Four different peaking times between 1.5 μs and 9 μs can be selected in the RC-CR analog shaper depending on the needs of the considered application.

Different versions of a simple fully depleted monolithic active sensor designed for brachytherapy composed of a pad diode with integrated electronics have been included in the wafer reticle of the three production runs. These chips called COBRA

are characterized by a small total area of 1×1 mm^2. Namely, the chips have been designed to be mounted on a prostate catheter that will be used to check the proper position and orientation of the radioactive seeds used in the brachytherapy treatment in order to ensure the delivery of the intended radiation dose, following the concept proposed in [69]. In a brachytherapy treatment a group of radioactive seeds, usually ^{125}I or ^{103}Pd, are directly placed inside the patient body near the target cancer cells, therefore a precise monitoring of the released dose is essential for the success of the medical treatment. In the first prototype (Figure 2.1.3) the sensor active region covers a total area of 460×340 μm^2 leaving the remaining space to the embedded electronics, composed of a dual gain frontend amplified and a buffer, and to the pads needed to apply the analog and digital voltage bias [70].

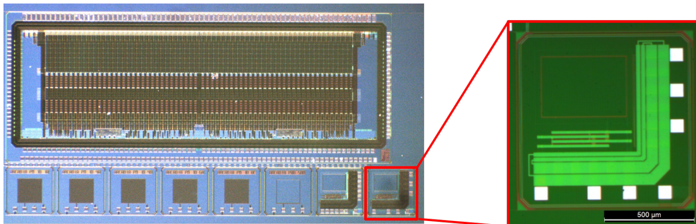


Figure 2.1.3: Picture of the silicon tile containing in the top section the ASTRA chip and in the bottom right corner the COBRA chips.

2.2 Passive Test Structures

A group of passive test structures has been included in two dedicated chips (Figure 2.2.1) in the first and second production runs and in a single chip in the third run to characterize the production process and evaluate the performance of the different pixel and strip layouts. Passive pixel arrays with the pixel n-type collection electrodes connected in parallel have been used to investigate the effect of different pixel layouts and pitches on the static IV and CV characteristics and on the charge collection dynamics. In an analogous way, an array of passive strips with different layout has been realized for the same purpose. Other test structures e.g. MOS capacitors and gated diodes have been used to get information on the concentration of charges in the passivation layer and on the surface generation velocity at the interface between the backside surface passivation layer and the silicon substrate. Backside diodes with different floating guard rings numbers have also been produced to determine the minimum guard ring number and the optimal guard ring pitch able to prevent the early breakdown of the backside junction.

Test structures with integrated gain layer have been designed and included in the third engineering run of the project targeting the possible use of MAPS with internal gain in timing applications. The design effort was supported from the ALICE 3 timing layers Working Group, in particular from INFN Torino

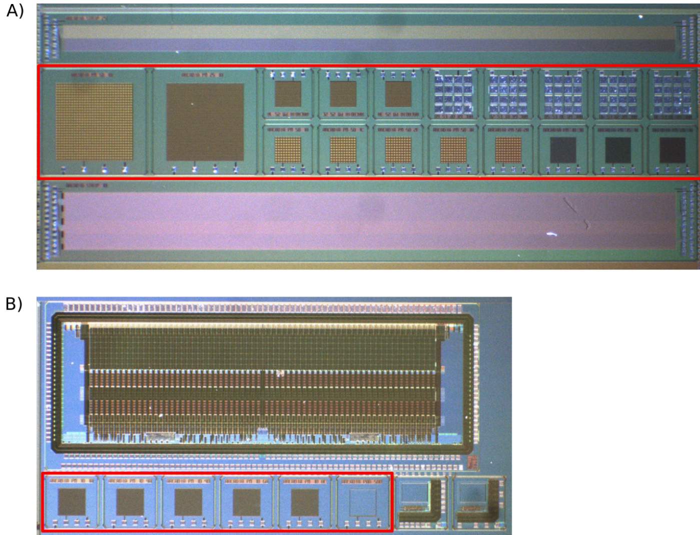


Figure 2.2.1: Picture showing the two chips containing the designed passive test structures highlighted with the red boxes.

and PoliTo, and the experimental results proved the feasibility of the gain layer integration inside the production process by a single process add-on. In the schematic cross section of a device with integrated gain layer reported in Figure 2.2.2, it is possible to notice that this layer has been realized by an additional p-type implantation below the n-type collection electrode.

The internal gain enables to increase the device SNR needed to improve the performance in terms of timing resolution. The targeted timing resolution for the ALICE Time of Flight layers is less than 20 ps and the required radiation hardness in terms

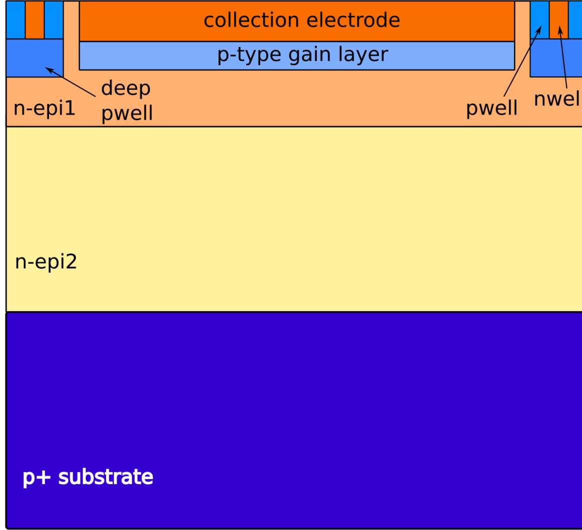


Figure 2.2.2: Schematic cross section of a monolithic LGAD.

of NIEL and TID is in the order of 10^{13} 1 MeV n_{eq} cm^{-2} and 1 Mrad, respectively [71]. The study of the charge collection dynamics performed with TCAD simulations, lead to the choice of a large size of the pixel pads with two possible pixel layouts, squared 250×250 μm^2 or rectangular 250×80 μm^2 pixels, to guarantee a uniform electric field shape which enables to speed up the charge collection. In order to achieve the desired timing resolution, the performed TCAD and MonteCarlo simulations showed that substrates thicknesses lower than 50 μm are needed. In the future production that will be dedicated to timing test structures for the ALICE 3 upgrade, the fore-

seen active substrate thicknesses will be in the order of 25 and 15 μm.

Chapter 3

Introduction to TCAD simulations

Nowadays, almost every engineering project exploits Computer Aided Design (CAD) tools in the design phase to make savings in terms of time and economic resources. The use of this powerful tools enables the numerical solution of complex and non trivial engineering design problems, which in many cases cannot be solved analytically in a closed form, employing the principles of Finite Elements Modeling. However, despite their potentiality, these software should be used with care and only specifically trained users are able to fully exploit their capabilities. If the user is not aware of the physical principles at the base of the design problem, the CAD simulation may be set improperly leading to a misinterpretation of the obtained results or to the belief in the correctness of a completely wrong solution. This can lead to expensive and time consuming mistakes in the design phase that jeopardize the possible advantages of the CAD tool employment. Talking about bottom-up electronics design projects, the most common approach is the use of Technology CAD tools for the

simulation of the actual device physical behavior on the basis of its layout and of the employed production process characteristics. In this way, it is possible to evaluate the dependence of the device performance on the design choices in terms of geometry and technology solutions without the need of testing an actual prototype. Moreover, exploiting a multi-parametric design approach, it is possible to get information on the most promising design solutions considering different combinations of the design parameters. Another common feature of TCAD software is the possibility to implement custom SPICE models reproducing the characteristics of the designed devices, which can be imported and employed in the simulations of complex circuits or electronics systems.

3.1 TCAD modeling principles

The Synopsys® - Sentaurus™ TCAD software has been employed to perform the electronics device simulations reported in this work. Most TCAD software follow a common procedure in the simulation definition that can be schematically described in the following steps:

- first of all, the geometry of the device structure has to be carefully defined. To this end, it is mandatory to assign the proper dimensions to the different doping regions, material layers and electrodes and to specify the values of the doping concentrations for the different regions. If

needed, a TCAD software allows the definition and thus the modeling of the sequence of production process steps employed to create the device;

- once the device structure has been defined, it is mandatory to define a suitable mesh discretization for the simulation domain selecting the proper element dimensions and types;

- then, the physical models used in the simulations to describe the device behavior must be selected among the available ones or, alternatively, can be defined and implemented from scratch, if needed;

- afterwards, one should select the numerical methods needed to solve the discretized version of the equations describing the physical behavior of the device;

- employing the selected numerical method, a TCAD software computes the numerical solution of the aforementioned equations at the mesh nodes and, to guarantee the continuity of the computed solution, the program interpolates the nodal values inside each mesh element and between the neighboring elements on the basis of the chosen shape functions;

- finally, the obtained nodal values are saved in binary files, having the characteristic .tdr file extension in Sentaurus™, which store also the information on the position

of the nodes and elements in the mesh. In an analogous way, at the end of each simulation step a set of output quantities related to the device electrodes can be stored in dedicated files, e.g. the .plt files in Sentaurus™, which represent the overall device behavior in terms of voltage, current and charges at the different electrodes.

In the following subsections the main step of this procedure will be explained in detail with reference to the specific characteristics of the Sentaurus™ TCAD environment. To have a more detailed explanation of the software commands and characteristics, one can refer to [72].

3.1.1 Device structure and mesh definition

Defining the materials of the different device layers and assigning them the proper dimensions represents the first step in the device structure definition. Depending on the complexity of the device geometry, it is usually convenient to exploit potential symmetry planes or periodicity in the layout in order to reduce the size of the simulation domain and thus decrease the total simulation time. Moreover, if the device structure is characterized from a constant layout in one direction, like in the case of strip arrays, which present a constant geometry along the strip direction, it is convenient to reduce the simulation domain to a 2D case representing a slice of the device in the direction orthogonal to the strip length. Once defined the

overall sizes of the device structure, if specific production steps are needed to realize the device geometry, Sentaurus™ allows the selection of the sequence of production process employed for the device creation. This feature results particularly useful in the design of Micro Electro-Mechanical Systems (MEMS), which require dedicated fabrication steps as the etching treatments for the creation of complex 3D geometries e.g. microcantilevers or thin membranes.

The following step in the simulation domain creation is usually related to the definition of the contact and doping region areas. In the case of 2D simulation domains, this corresponds to the definition of segments on the device surface where the electrodes will be placed or the ion implantations will be performed. Non contiguous segments can be assigned to the same electrode to simulate the connection to a common readout channel. Constant doping regions as well as 1D- and 2D-doping profiles, representing the concentration and spatial distribution of the chosen dopants, can be defined on the basis of the available built-in function already implemented in the software. Sentaurus™ provides built-in Gaussian or Error Function functions to describe the doping profiles and allows also the implementation of custom analytic functions. Moreover, the doping profiles can be imported from external files, where the doping concentration are listed as a function of their depth w.r.t. the device surface. These files can be provided directly from the silicon foundries, which have com-

monly an excellent control on the dopant implantation. This fact is beneficial for the reliability of the simulation results since the simulated device structures can represent more precisely the fabricated ones.

Choosing the proper mesh to be applied to a simulation domain is one of the most relevant and tricky task in the definition of a TCAD simulation. Namely, the simulation time and computational resources required from a simulation are function of the total number of elements and nodes in the simulation domain mesh. Moreover, the accuracy of the simulation results is strictly related to the unavoidable error associated to the approximated numerical solution of the discretized equations describing the physical behavior of the device, which is also dependent on the mesh element size. Triangular elements and tetrahedral elements represent the default element types employed by Sentaurus™ for the mesh generation in the 2D and 3D case, respectively. Usually, assigning a coarse general mesh to the whole simulation domain represents the first step in the mesh definition. Then, finer mesh refinements are assigned to specific regions of the device, where the element dimensions of the general coarse mesh would not be able to represent properly the device characteristics. This procedure enables to limit the total number of nodes and elements increasing the element and node densities only in the critical regions of the simulation domain. The mesh refinement regions are commonly selected on the basis of the following general

criteria:

- regions characterized by high gradients in the electric field or by high electric field values;
- regions having high gradients in the doping concentration of the device material;
- regions showing high current densities;
- regions close to charge generation centers e.g. due to optical generation or charged particles incident on the simulation domain.

In Sentaurus™ the minimum and maximum element sizes along the different directions are assigned to the general mesh and to the different refinement regions and additional specific rules can be defined and employed in the mesh generation. In the simulations described in the following chapter, a local mesh refinement based on doping concentration gradients was used. As a consequence, the element size decreases in correspondence of a sharp gradient in the doping concentration or, alternatively, the mesh is relaxed in regions with constant doping.
Once created a first tentative mesh on the basis of the aforementioned conditions, the mesh generator applies a Delaunay algorithm to the mesh draft to avoid the generation of critical mesh elements [73]. To this end, the algorithm evaluates the generated mesh elements trying to maximize the size of

the smallest angle inside each mesh element. The algorithm considers the circumcircle of each triangular element in the 2D case or the circumsphere of each tetrahedron in the 3D case and accommodates the mesh so that only the nodes associated to the considered elements are contained inside the circumcircle or circumsphere. This enables to avoid the presence of critical centers within the generated mesh and thus improves the simulation robustness against non-convergence problems as well as the simulation results reliability.

3.1.2 Physical models and numerical methods

The definition of the physical models and numerical methods to be employed in the simulation usually follows the device structure creation and the mesh generation. TCAD simulations of semiconductor electronic devices are based on the solution of the semiconductor model equations, which are a combination of the Poisson, transport and continuity equations. The Poisson equation (eq. 3.1) expresses the relation of the electric field with the concentration of charge carriers inside the material in a mono-dimensional device case, which can be easily extended to the multidimensional case using eq. 3.2.

$$\frac{\partial^2\Psi}{\partial x^2} = -\frac{q(N_D + p - N_A - n)}{\varepsilon_s}, \quad \text{1D case} \tag{3.1}$$

$$\nabla^2\Psi = -\frac{q(N_D + p - N_A - n)}{\varepsilon_s}, \quad \text{multi-D case} \tag{3.2}$$

In the previous equations Ψ stands for the electrostatic potential, ε_s for the silicon dielectric constant and N_A, N_D, p and n for the concentrations of ionized acceptors, of ionized donors, of holes and of electrons, respectively.

Different formulations for the transport equations are already implemented and thus available in Sentaurus™. The available models give the possibility to choose among the Boltzmann transport equations, Hydrodynamics equations, quantum approaches or the classical Drift-Diffusion model, which has been used in the performed simulations.

The Drift-Diffusion equations (eq. 3.3) describe the total electron (J_n) and hole (J_p) current densities as the sum of two different current components related to the drift and diffusion mechanisms. These relations can be extended to their multi-dimensional formulation (eq. 3.4), where μ_n and μ_p represent the electrons and holes mobility and D_n and D_p the electrons and holes diffusion coefficients.

$$\begin{cases} J_n = qn\mu_n E + qD_n \frac{\partial n}{\partial x} \\ J_p = qp\mu_p E - qD_p \frac{\partial p}{\partial x} \end{cases} \quad \text{, 1D case} \tag{3.3}$$

$$\begin{cases} \mathbf{J_n} = qn\mu_n \mathbf{E} + qD_n \nabla n \\ \mathbf{J_p} = qp\mu_p \mathbf{E} - qD_p \nabla p \end{cases} \quad \text{, multi-D case} \tag{3.4}$$

Finally, the continuity equations (eq. 3.5 for 1D and eq. 3.6 for multi-D cases) ensure the respect of the law of conservation of charges, that guarantees the balance between the input and output charge fluxes and the changes in the charge carrier concentrations inside the material. These equations take into account the contributions related to the external generation phenomena (G_{ext}) and to the net recombination rate R.

$$\begin{cases} \frac{\partial n}{\partial t} = G_{ext} - R + \frac{1}{q} \frac{\partial J_n}{\partial x} \\ \frac{\partial p}{\partial t} = G_{ext} - R - \frac{1}{q} \frac{\partial J_p}{\partial x} \end{cases} \quad \text{, 1D case} \tag{3.5}$$

$$\begin{cases} \frac{\partial n}{\partial t} = G_{ext} - R + \frac{1}{q} \nabla J_n \\ \frac{\partial p}{\partial t} = G_{ext} - R - \frac{1}{q} \nabla J_p \end{cases} \quad \text{, multi-D case} \tag{3.6}$$

The system of partial differential equations obtained by combining these three sets of equations enables the description of the electrical behavior of the simulated devices. However, the closed-form analytic solution of the problem can be obtained only in few simple cases with proper boundary conditions, thus requiring numerical approaches to get an approximated solution in most cases.

The formulation of the Drift-Diffusion model implemented in the TCAD software relies on a discretized version of these equations that, applying a generalization of the finite difference method called box method, can be expressed through eq. 3.7, 3.8, 3.9 [74]–[77]. In the derived discretized equations, the partial time derivatives of the electrons and holes concentrations have been considered equal to zero and, therefore, this formulation does not hold for transient simulations, which have time dependent boundary conditions. Applying this method, the system of partial differential equation is transformed in a system of N algebraic equations having N+2 unknowns representing the nodal values of the elements in which the simulation domain is subdivided. The formal mathematical description of the box method and a more detailed explanation of this topic can be found in [74], [75], [77].

Figure 3.1.1 shows a schematic representation of a simulation domain detail, where a single box has been sketched on a group of neighboring triangular elements. Looking at the Figure, it is possible to find a visual representation of the apex and pedex notation employed in the discretized equations. Namely, the pedex i and the apex e refer to the i-th control region of the box method and to the e-th element of the mesh, respectively, and the pedex j represents the j-th node belonging to the considered e-th mesh element and contained in the i-th control region Λ_i. Moreover, this sketch enables to get an idea of the physical meaning of the t_{ij}^e and f_{ij}^e terms, which show up in

the aforementioned equations.

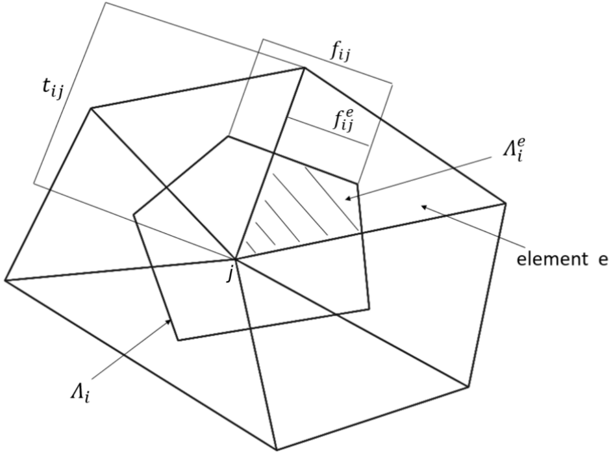


Figure 3.1.1: Box region in a 2D mesh with triangular elements [78].

Looking in the details at the box method working principle, it is possible to notice that the derivatives are converted in the corresponding incremental ratios and the complex functions are approximated with numerical successions. The continuity of the obtained nodal solutions, representing the field variables, is guaranteed by using properly chosen shape functions, that interpolate the nodal values within each mesh element and among the neighboring elements.

$$\sum_{e \in element(\Lambda_i)} \varepsilon_s \left(\sum_{\substack{j \neq i \\ j \in vert(e)}} \frac{f_{ij}^e}{t_{ij}^e} \left(\Phi_i^e - \Phi_j^e \right) \right) + \Lambda_i^e \, q \left(n_i^e - p_i^e - N_i^e \right) = 0 \tag{3.7}$$

$$\sum_{e \in element(\Lambda_i)} D_n^e \left(\sum_{\substack{j \neq i \\ j \in vert(e)}} \frac{f_{ij}^e}{t_{ij}^e} \left(n_i^e \, B(\Phi_i^e - \Phi_j^e) - n_j^e \, B(\Phi_j^e - \Phi_i^e) \right) \right) + \\ + \Lambda_i^e \, q \left(R_i^e - G_i^e \right) = 0 \tag{3.8}$$

$$\sum_{e \in element(\Lambda_i)} D_p^e \left(\sum_{\substack{j \neq i \\ j \in vert(e)}} \frac{f_{ij}^e}{t_{ij}^e} \left(p_i^e \, B(\Phi_i^e - \Phi_j^e) - p_j^e \, B(\Phi_j^e - \Phi_i^e) \right) \right) + \\ + \Lambda_i^e \, q \left(R_i^e - G_i^e \right) = 0 \tag{3.9}$$

The Bernoulli function $B(x)$ (eq. 3.10) applied to the electrostatic potential Φ has been employed to simplify the notation in the previous equations.

$$B(x) = \frac{x}{e^x - 1}, \tag{3.10}$$

Since the system results undetermined, having a number of unknowns greater than the number of derived algebraic equations, boundary conditions are needed to decrease the number

of unknowns and, thus, get a numerical solution of the system at the element nodes. The Dirichlet and Von Neumann boundary conditions represent the two different families of boundary conditions that can be imposed to the problem [76]. The former set a specific condition on the semiconductor potential at the contact surfaces Φ_s, which is assumed to be equal to the external applied voltage $\mathrm{V_{ext}}$ and thus representing an Ohmic contact (3.11).

$$\Phi_\mathrm{s} = \mathrm{V_{ext}} \tag{3.11}$$

The latter prevent the flow of any current component in the direction normal to the device surfaces (N) and, as a consequence, are also known as reflective boundary conditions, which can be expressed in terms of the electrons ($\mathrm{J_n}$) and holes ($\mathrm{J_p}$) current densities by eq. 3.12.

$$\begin{cases} \mathrm{J_n} \cdot \mathrm{N} = 0 \\ \mathrm{J_p} \cdot \mathrm{N} = 0 \end{cases} \tag{3.12}$$

Usually, iterative Newton based solvers are employed to obtain the numerical solution of the system of equations on the basis of the imposed boundary conditions [79], but there is also the possibility to choose a different numerical method among a set of available algorithms already implemented in the software. Common parameters that can be modified to control the numerical methods are the maximum number of solver iterations that the algorithm is allowed to perform before chan-

ging the step size or the number of iterations which triggers the modification of the Newton based solver on the base of the Rose-Bank damping scheme [79], [80]. The size of the relative error, which is related to the solution accuracy, represents another control parameters, whose modification acting on the number of precision digits influences the convergence rate of the solution as well.

In the performed simulations, the Shockley-Read-Hall (SRH) model has been employed to describe the trap assisted generation and indirect recombination effects inside the detector material [81], [82]. According to the model, the traps induce the presence of additional energy levels in the band gap between valence and conduction bands, where the charge carriers can recombine following an indirect process and thus release thermal energy in the form of phonons resulting in lattice vibrations. Eq. 3.13 represents the relation between the net generation-recombination rate and the carrier concentrations and carrier lifetimes (τ).

$$R_{SRH} = \frac{np - (n_i)^2}{\tau_p(n + n_I) + \tau_n(p + p_I)} \tag{3.13}$$

The terms n_i, n_I and p_I, employed in the previous equation, represent the intrinsic carrier density and the electrons and holes concentrations associated to a trap energy equal to E_t. These concentrations can be described by eq. 3.14 and 3.15 according to [74].

$$n_I = n_i\, e^{\frac{E_t - E_i}{kT}} \tag{3.14}$$

$$p_I = n_i\, e^{\frac{E_i - E_t}{kT}} \tag{3.15}$$

The doping dependence of the carrier lifetimes has been considered in the simulations using a modified version of the Scharfetter relation, which can be expressed by eq. 3.16 according to [83], [84].

$$\tau = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^{\beta}} \tag{3.16}$$

Several built-in models are available to describe the dependence of the electron and hole mobility on the total concentration of dopants and on the temperature variation [85], [86]. For example, eq. 3.17 represents the relation describing the dependence of the carrier mobility on the total concentration of dopants (N_{tot}) according to the Arora model [85].

$$\mu_{n,p} = \mu_{n,p_{min}} + \frac{\mu_{n,p_0}}{1 + \left(\frac{N_{tot}}{N_0}\right)^{\alpha}} \tag{3.17}$$

In this model the values of $\mu_{n,p_{min}}$, μ_{n,p_0}, N_0 and α show a non-linear dependence on the temperature variation according to eq. 3.18, thus representing the empirical relation describing the mobility variation as a function of the temperature.

$$x(T) = x(300K)\left(\frac{T}{300}\right)^{\beta} \tag{3.18}$$

The tunneling effect has been also considered including, among the different available models [87]–[89], the one described by Fowler and Nordheim in [87], which can be summarized in eq. 3.19, where c_1 and c_2 represent tabulated experimental coefficients and E is the electric field at the pn junction.

$$J_{tun} = c_1 E^2 e^{-\frac{c_2}{E}} \tag{3.19}$$

The presence of charge multiplication and of the possible breakdown of the junction has been included in the simulations. Two models, the van Overstraeten–de Man and the Okuto–Crowell, have been tested and compared in order to determine the most reliable one in predicting the actual breakdown voltage of the designed devices [90], [91].

Models specifically implemented for describing the optical generation and the e^--h^+ pairs generation due to the silicon interaction with different radiation types are available in the software. Therefore, these models have been exploited to predict the sensor response in different illumination condition and its possible interaction with different charged particle types.

In the optical simulations, a light pulse from a monochromatic source was employed to evaluate the charge collection dynamics of sensors with different pixel pitches, pixel layouts and substrate thicknesses. The obtained results have been compared with the experimental measurements performed in an optical setup with a near-IR or a red laser source with 1060 nm and 660 nm wavelength, respectively. The optical charac-

teristics of the monochromatic source were specified in term of optical power, shape and sizes of the illumination window and temporal characteristics of the light pulse.
On the other hand, the presence of an incident charged particle was used to predict the sensor response to an external particle flux. The employed model enabled to define the amount of e^{-}-h^{+} pairs deposed along the particle track per unit of path length inside the detector material. Dedicated features of the model were available to control the dimension of the radius of the cylindrical volume around the particle track, where the charges were generated, and thus to monitor the spreading of the generated electron cloud, as well as to define the position of incidence of the particle on the simulation domain and the particle track direction. The Linear Energy Transfer (LET) between the particle and the detector material was set to be constant along the particle track, modeling the charge deposition of different particles ranging from Minimum Ionizing Particles to heavy ions.
The radiation hardness of the designed sensors has been evaluated employing the so-called New-Perugia model that has been implemented from scratch in the TCAD software and tuned on the basis of the experimental results [67], [92], [93]. Both the bulk damage specified in terms of Non Ionizing Energy Loss (NIEL) and the surface damage represented by Total Ionizing Dose (TID) have been considered and evaluated for the different layouts and pitches.

Chapter 4

ARCADIA test structures

4.1 TCAD simulations

Following the TCAD design principles illustrated in Chapter 3, preliminary simulations have been performed before submitting the final wafer reticle to the foundry. In this way, only the active and passive structures with the most promising layouts were fabricated and then tested experimentally. This step enabled to spare resources from the economical point of view and, at the same time, allowed the reduction of the total amount of time spent in the experimental characterization of the produced devices, testing only a subset of the possible strip and pixel layouts and pitches. In particular, these layouts were selected on the basis of the following evaluation criteria: the minimization of the pixel or strip capacitance, the optimization of the timing performance and the expected radiation hardness estimated on the basis of the employed radiation damage model. The results of the TCAD simulations performed to determine the optimal pixel and strip layouts for the three considered pitches equal to 50, 25 and 10 μm were reported in [24], [67], [78] and in [94], respectively.

First of all, simulations with 2D domains were performed to get a preliminary fast evaluation of the considered layouts. Namely, the use of simplified 2D domains, representing a cross section of the device along a cut plane parallel to the device thickness, allows the allocation of a limited amount of computation resources thanks to the usually lower total number of mesh elements and nodes in comparison to whole 3D simulation domains. However, this fact represents at the same time a limit to the reliability of the simulation results since possible 3D-related spatial effects are neglected or badly modeled. As a consequence, simulations on complete 3D domains have been performed as well in all the cases when the accuracy of 2D simulations could result too poor. The results presented in the following Sections refer to simulations in which a temperature of 300 K has been considered, if not stated otherwise.

4.1.1 IV and CV

As a rule of thumb, preliminary 2D simulations followed by more accurate 3D simulations have been used to evaluate the punch through V_{PT} and full depletion V_{depl} voltages and the pixel or strip capacitance C_{pix} from the obtained IV and CV characteristics, respectively. Simulations in quasi-stationary regime have been used to estimate the IV characteristics of the considered pixel pitches and layouts acting on multiple design parameters like the substrate and epitaxial layer thicknesses and doping concentrations [67], [78], [94]. In these simula-

tions a small voltage unbalance equal to 10 mV was applied between the collection electrodes of two neighboring pixels, see Figure 4.1.1, in order to enable a current flow between the two n-type electrodes. A negative voltage sweep was applied to the backside p-type electrode (V_{bias}) to gradually deplete the sensor substrate until the full depletion was reached. Finally, the internal pwell contact was set to 0 V and used as ground reference. V_{PT} and V_{depl} represent the upper and lower voltage limits in the definition of the operating voltage range ΔV of the designed pixels. In particular, the extracted full depletion voltage corresponds to the voltage bias at which the n-type collection electrodes become isolated due to the space charge region growing from the sensor backside which chokes the conductive path between the nwells. Instead, the punch through voltage represents the bias voltage able to reduce the potential barrier between the frontside and backside p-type implants and thus enabling the flow of a hole current. Looking at the simulated pwell and n-type collection electrode currents displayed in Figure 4.1.1, it has been possible to estimate V_{PT} and V_{depl}, taking as a reference the dips in the curves associate to the change of sign in the pwell and nwell current, respectively. In the graph it is possible to notice the effect of the voltage applied to the collection electrode (V_n) on the extracted value of the full depletion voltage, which decreases for increasing V_n values. The simulations proved that at the foreseen operating voltage V_n equal to 0.8 V, the punch

through voltage occurs at higher V_{bias} w.r.t. the full depletion voltage.

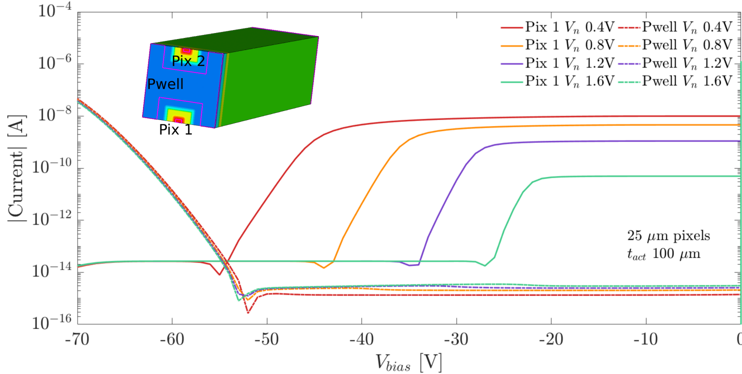


Figure 4.1.1: Simulated IV characteristics of 25 μm pixels with 100 μm active thickness for different V_n values. The results refer to TCAD simulations performed on 3D domain composed by two pixel halves.

The preliminary simulation predicted a different operating voltage range for the pixel arrays with 10 μm pixels with respect to the pixel arrays with 25 and 50 μ pixels [67]. As a consequence, the passive pixel arrays with the 10 μm pixel layouts have been included on a different test chip in order to avoid possible issue related to the application of the backside voltage bias. Namely, the punch through voltage of the pixel arrays with larger pitches was in most cases lower than the full depletion voltage of the 10 μm pixel arrays.
The pixel CV characteristics were estimated through small signal AC analysis performed in mixed mode TCAD simu-

lations, where the device nodes have been connected in a SPICE-like netlist [72]. 3D domains composed of a single pixel with an oxide layer included on top of the pixel frontside have been employed in these simulations, considering an initial concentration of positive charges at the Si-SiO_2 interface equal to 6.5×10^{10}cm^{-2} before irradiation, chosen according to the Hamamatsu parametrization described in the "new Perugia model" [64], [67], [95]. A fixed negative voltage bias greater than V_{depl} was applied to the backside electrode and, at the same time, a voltage sweep was applied to the frontside internal pwell thus changing the extension of the depletion region inside the epitaxial layer [95]. An example of the CV curves obtained from the simulations of three different pixel layouts is shown in Figure 4.1.2.

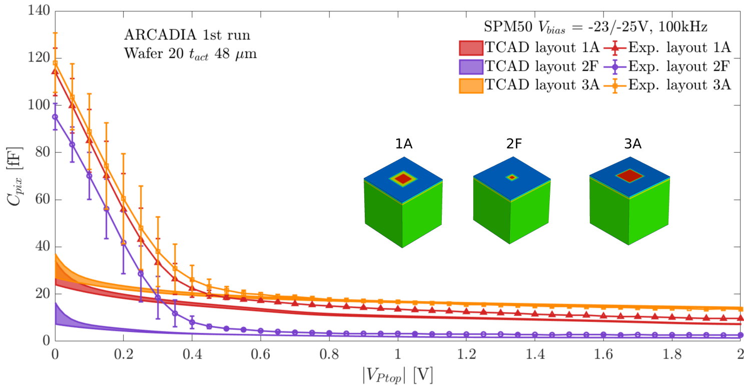


Figure 4.1.2: Simulated and measured pixel capacitance as a function of the frontside pwell voltage for 50 μm pixels with different pixel layouts and 48 μm active thickness.

In these curves it is possible to observe a plateau for applied pwell voltages greater than 1 V, that is linked to the full depletion of the epitaxial layer. A good agreement for bias voltages larger than 0.5 V was found between the simulated and measured pixel capacitance values, proving the reliability of the models employed in the design phase. As expected, larger capacitance values were obtained for the pixel layout characterized by larger collection electrode size and smaller gap between the frontside nwell and pwell.

4.1.2 Radiation hardness

The evaluation of the foreseen radiation hardness for the different pixel layouts to a Total Ionizing Dose up to 1000 Mrad has been performed through simulations on 3D domains, where the radiation damage model known as "new Perugia model" was implemented. The same passivation layer composed of silicon dioxide considered also in the aforementioned CV simulations was included on top of the simulation domains to take into account its effects on the pixel capacitance and the dark current values due to the accumulation of positive charges at the interface between silicon and silicon dioxide for increasing TID values [67]. Figure 4.1.3 shows the simulated CV characteristic of a 50 μm pixel with standard pixel layout and 50 μm substrate thickness for increasing TID values. In these simulations a voltage sweep between 0 and -45 V was applied to the pixel backside electrode to observe the variation in

the pixel capacitance for increasing bias voltages. In the plot, it is possible to observe the increase in the pixel capacitance related to the accumulation of positive oxide charges at the Si-SiO_2 interface. An initial small concentration of acceptor and donor trap states equal to 2×10^9 cm^{-2} was included in the simulations to account for possible recombination centers at the detector material interface. Moreover, the employed "new Perugia" model considered also the non ionizing radiation damage occurring in the silicon bulk introducing three trap levels in the silicon bandgap [67].

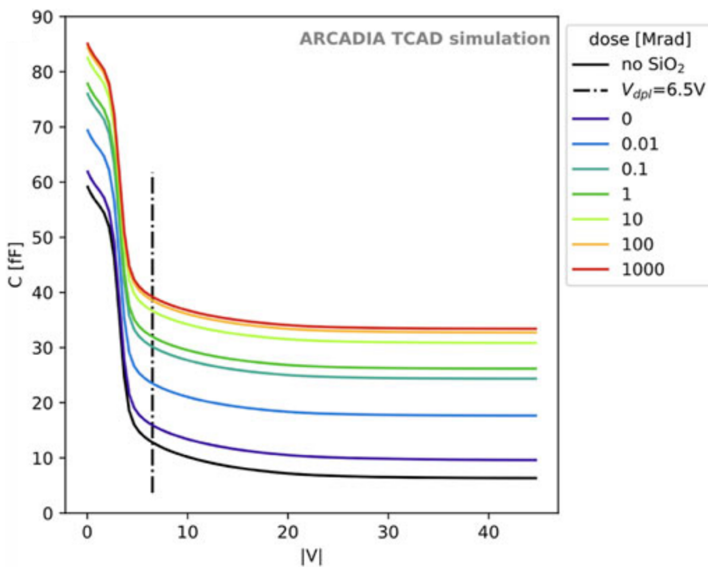


Figure 4.1.3: Pixel capacitance for different TID levels for a 50 μm pixel with 50 μm active thickness. Picture from [67] (CC BY 4.0).

4.1.3 Backside junction terminations

The backside termination structures needed to guarantee the possibility to apply the negative bias voltage to the backside electrode avoiding the breakdown at the junction borders have been designed exploiting 2D simulation domains with 300 μm substrate thickness and variable guard ring number and guard ring pitch [16]. These simulations enabled to determine the minimum floating guard ring number and the optimal guard ring pitch able to prevent the breakdown of the junction for applied bias voltages lower than the foreseen operating voltage range. The cross section of a 2D simulation domain, together with the associated electric field and electrostatic potential profiles is reported in Figure 4.1.4 [16]. In the cross section, the blue regions represent the p-type implants of the backside diode p-n junction and of the surrounding floating guard rings, while the low doped n-type silicon substrate and the passivation layer are shown in green and light blue, respectively. Three different concentrations of positive charges at the interface between silicon and the passivation layer made of silicon dioxide equal to 0.5, 1 and $2 \times 10^{12}\,\mathrm{cm}^{-2}$ have been considered in the performed simulations to ensure the reliability of the termination structures for different oxide charge concentrations. According to the mean value extracted from the measurements performed on a group of process control structures, a surface generation velocity in the order of 200 cm/s at the interface between silicon and silicon dioxide has

been included in the simulations. Finally, metal field plates were included on top of the floating guard rings to smooth out the local peaks in the electric field and thus guarantee an higher breakdown voltage [16]. A comparison between the breakdown voltages predicted from TCAD simulations and the actual values obtained from the experimental measurements on a group of backside diodes with variable guard ring number and pitch will be presented in the following Section.

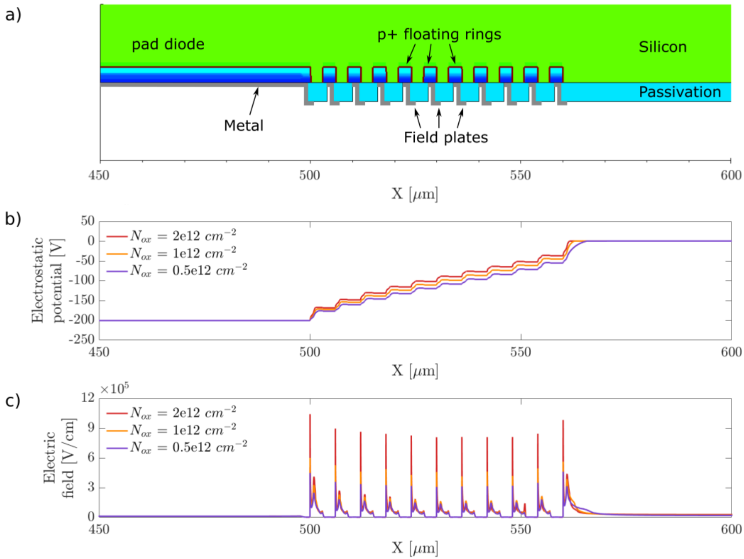


Figure 4.1.4: (**a**) Cross section of a 2D simulation domain showing the designed guard ring structure. (**b**) Electrostatic potential profile. (**c**) Electric field profile. Picture from [16] (CC BY 4.0).

4.1.4 Transient simulations with charged particles

The evaluation of the charge collection dynamics of the devices has been performed by mean of transient simulations on 3D domains or, if possible, 2D domains with cylindrical coordinates. 3D multi-pixel domains have been employed to evaluate the charge sharing between neighboring pixels and possible blooming effects associated to the voltage drop at the collection electrodes concurring to the collection of the deposed charges. In particular, the planes of symmetry in the pixel matrix were exploited to decrease the total simulation domain size and thus to reduce the simulation time in the transient simulations performed on large multi-pixel domains. The charge sharing among neighboring pixels was evaluated for increasing Linear Energy Transfer (LET) values of the incident charge particle and three increasing substrate active thicknesses equal to 50, 100 and 300 μm. In the computation of the cluster size, a threshold corresponding to 10% of the charge deposed from a MIP in an equivalent silicon thickness was considered to decide whether a pixel had to be considered fired and thus included in the pixels of the cluster. Three different positions of incidence for the charged particle have been considered, corresponding to the pixel center, the border between two pixels or the corner among four pixels. A dedicated simulation domain was built for each case in order to exploit in the best way the symmetry planes of the pixel

matrix and thus create a reduced simulation domain with minimum size corresponding to a quarter of the whole considered domain. The created simulation domains are shown in Figure 4.1.5, where the position of the incident particle has been highlighted with a red dot in the top right corner of the domains.

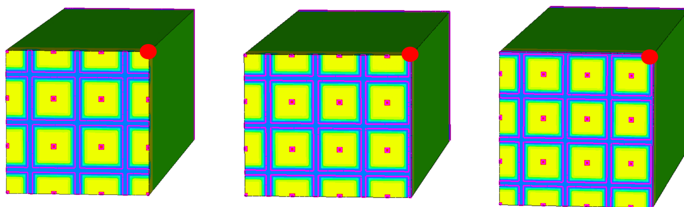


Figure 4.1.5: Reduced simulation domains created for the three considered positions of the incident particle.

According to the mesh principles explained in Chapter 3, an additional mesh refinement was included in correspondence of the particle track in order to properly model the charge generation localized in the surrounding cylindrical volume with 1 μm diameter. Figure 4.1.6 shows the pixel cluster size as a function of the particle LET for the three considered substrate thicknesses of an array with 10 μm pixels. A threshold corresponding to 10% of the charge deposed from a MIP in an equivalent silicon thickness was chosen to consider a pixel fired and thus included in the cluster. In the simulations a voltage of 1.2 V was applied to the frontside collection elec-

trodes, the pwell was grounded to 0 V and a negative bias voltage larger than the full depletion voltage was applied to the backside p-type electrode. As expected, the cluster size increased for increasing particle LET values and for increasing substrate thicknesses, reaching a maximum size of 45 pixels for the considered extreme case with LET equivalent to 100 MIP and substrate thickness of 300 μm.

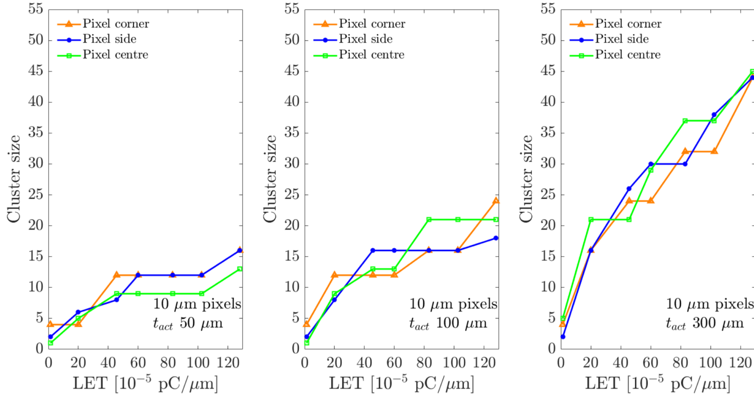


Figure 4.1.6: Simulated pixel cluster size for increasing particle LET value and three different substrate thicknesses.

The same simulations were employed to evaluate the collection dynamics of the pixels with 10 μm pitch as a function of the amount of generated charges and of the active substrate thickness. Namely, decreasing the pixel size was considered a promising strategy to improve the charge collection speed since the distance between the collection electrodes is reduced.

The time needed to collect 99% of the generated charge (t_{99}) in the cluster pixels is reported in Figure 4.1.7 for the three active substrate thicknesses equal to 50, 100 and 300 μm and the three aforementioned positions of the incident particle. The simulated collection time increases nearly linearly as a function of the particle LET for the thinner substrate thicknesses and, on the contrary, shows a non linear increase in the results of the simulations with 300 μm substrate thickness. The observed increase in the t_{99} for increasing particle LET values is related to the higher density of charges generated around the particle track, which leads to space charge effects, reducing the effective electric field and thus slowing the charge collection speed down.

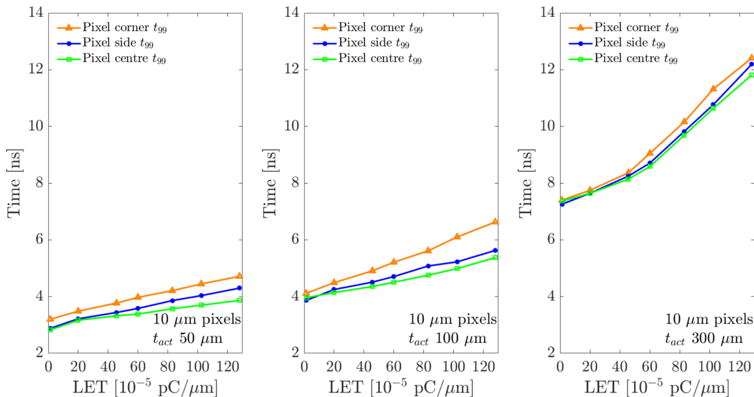


Figure 4.1.7: Simulated t_{99} of 10 μm pixels for increasing particle LET value and three different substrate thicknesses.

Transient simulations were also used to evaluate the possible presence of blooming effects, which can lead to an increase of the pixel cluster size. In the ARCADIA readout, the voltage at the pixel collection electrodes is not fixed to a constant value. Namely, when the generated charge is collected at the sensor node, the signal is integrated directly on the pixel capacitance leading to an instantaneous drop in the voltage at the collection electrode. Then, a bias transistor restores the voltage at the sensor node to its initial nominal value. To reproduce this effect, a bias resistor with a resistance of $10\,\mathrm{M}\Omega$ was connected in series to the nwells, resulting in a drop in the voltage applied to the collection electrodes associated to the collection of the generated charges. The same simulations were also conducted using a low-valued $1\,\Omega$ resistor for comparison. The simulations were performed on multi-pixel 3D domains composed of 9 pixels with 25 μm pitch and same layout of the MD pixels, considering two active substrate thicknesses equal to 48 or 200 μm. The charge generation was modeled through a charged particle incident in the central pixel of the domain, labeled as Pix5 in Figure 4.1.8, using variable LET value equal to 0.5, 1, 2 MIPs and 1, 2, 8 MIPs for the 200 and 48 μm thick substrates, respectively.

A drop in the voltage of the n-collection electrode equal to 28 mV, corresponding to the voltage difference resulting from the collection of 800 e^- in a MD pixel, was selected as threshold in order to consider a pixel as fired. This threshold is of the

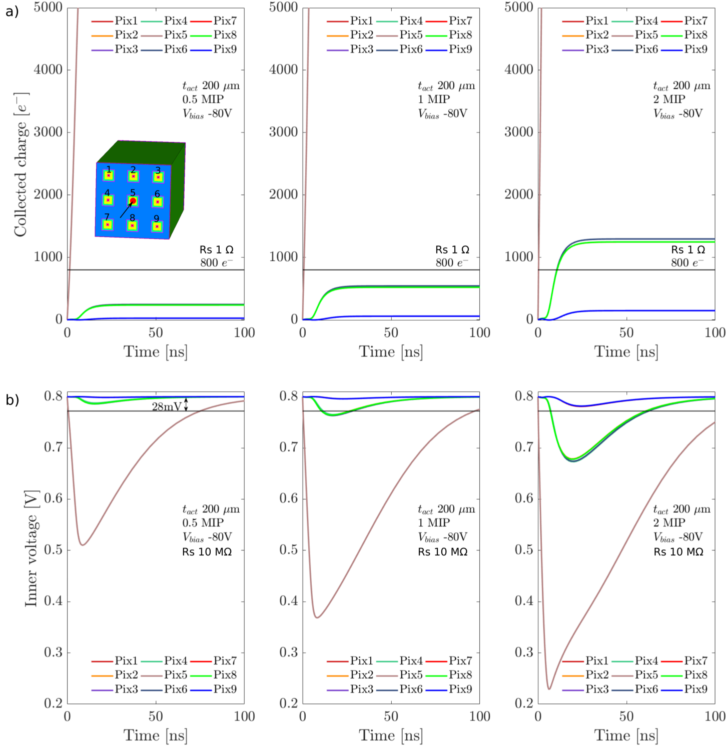


Figure 4.1.8: (**a**) Charge collected from the pixels of the domain for three particle LET values equal to 0.5, 1 and 2 MIPs. (**b**) Voltage at pixel collection electrodes for three particle LET values equal to 0.5, 1 and 2 MIPs.

same order of magnitude to the one that can be applied to the ARCADIA MD pixels. The cluster sizes provided by the simulations with different resistance values have been compared to determine whether the number of fired pixels was actually

related to the collection of an amount of charges higher than the chosen threshold or represented an artifact due to blooming effects. The difference in the extracted cluster size, that is a direct consequence of blooming, can be observed comparing Figures 4.1.8a and 4.1.8b, showing the charges collected and the voltage drop at the collection electrode as a function of the time for the simulated pixels with 1 Ω and 10 MΩ series resistors, respectively.

Looking at the charge collected from the domain pixels, a single pixel is firing when the generated charge corresponds to the one released from an half or a single MIP and, instead, considering a particle LET equal to two MIPs, five pixels collect a number of electrons greater then the chosen threshold and thus can be considered part of the cluster. On the contrary, looking at the inner voltage drop, when the 10 MΩ resistor is connected in series to the pixel electrodes, five pixels are firing in both cases with a charge generation corresponding to a single or two MIPs. Table 4.1 summarizes the cluster sizes obtained from the simulations with 200 μm thick domains for the two different thresholds and the three particle LET values. This leads to the conclusion that, choosing a threshold associated to a drop in the inner voltage measured at the pixel collection electrodes, can result in a larger cluster size due to possible blooming effects.

Table 4.1: Cluster size (CS) for 25 μm pixels with t_{act} 200 μm according to the charge collection and the inner voltage drop thresholds

threshold	800 e^-	28 mV
CS	# pixels	# pixels
0.5 MIP	1	1
1 MIP	1	5
2 MIP	5	5

4.1.5 Transient simulations with optical stimulus

A high charge density due to generation within the detector material can result in space charge effects, which spoil the detector performance in terms of charge collection dynamics and, at the same time, lower the gain value that LGADs can provide [44]. Therefore, we used transient simulations to appraise the optical response of the aforementioned and several others pixel variants having different layouts and pitches with sizes up to 250 μm to a light pulse with adjustable optical power. 2D simulations are not suitable to model space charge effects, since they do not account for charge carrier diffusion in the third dimension. Thus, a 3D domain should be used, increasing the computation time and complexity. As a consequence, 2D domains with cylindrical coordinates have been

exploited in the simulations of the region around the pixel center for the pixels with 250 μm size to reduce the simulation time and to guarantee an higher accuracy w.r.t. 2D simulations in terms of space charge effects related to the spread of the generated e^{-}-h^{+} cloud.
The optical generation was modeled through a near Infra-Red (IR) or a red light pulse with wavelengths of 1060 nm and 660 nm, respectively, and sub-nanosecond pulse lengths. A constant optical generation covering the whole simulation domain or a focused light spot with a diameter of 10 μm have been employed in the simulations to get information on the overall pixel response resulting from the contributions coming from the different pixel regions or to disentangle these signal components. A comparison of the results obtained from the performed simulations with the experimental measurements acquired in an optical setup will be presented in Section 4.4.

4.1.6 Design of pixels with integrated gain layer

Finally, an additional set of transient simulations has been implemented to evaluate the effect on the charge multiplication and on the timing response of different layouts of the terminations at the edges of the pixels with integrated gain layer. The schematic cross sections of the two considered layouts for the pixel borders are reported in Figure 4.1.9, where it is possible to observe the main features of the designed LGADs. In particular, the pixels with layout A2 present a design of

the borders with a gap region between the frontside p-type implants corresponding to the deep pwell and the gain layer. Instead, the pixels having layout A1 and G1 are characterized by the same design of the terminations with the deep pwell that forms a continuous p-type implantation with the gain layer below the n-type collection electrode of the pixel.

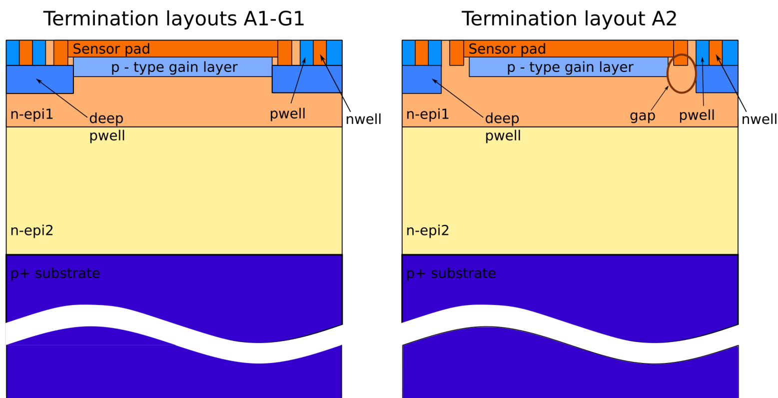


Figure 4.1.9: Schematic cross sections of the pixels with integrated gain layer and different layouts of the terminations at the collection electrode borders.

Due to their large sizes, 250×250 μm^2 for the squared or 250×100 μm^2 for the rectangular pixels, 2D domains corresponding to a horizontal cross section of two neighboring pixels have been exploited to get a fast estimation of the layout influence on the charge collection dynamics. The position of the incident focused laser spot was varied along the domain

backside surface to extract the amount of generated charges collected from the two domain pixels and from the n-guard ring placed in the inter-pixel region. The comparison of the charge collected from the three different n-type electrodes, corresponding to the two pixels and the guard ring, for the two considered layouts is shown in Figure 4.1.10a. The two termination layouts differ for the absence or the presence of a gap region between the p-type implants of the gain layer and of the frontside deep pwell.

The layout A1 has no gap region between the frontside p-type implants and, as a consequence, all the generated charges that are collected from the pixel electrodes have to travel through the gain layer region and are multiplied through impact ionization. On the contrary, the presence of a small gap region in the layout A2 creates an alternative path for the collected charges, which enables the collection of a part of the electrons generated in the inter-pixel region directly by the border of the pixel collection electrode without traveling in the gain layer region. Therefore, this second option was expected to provide a lower charge multiplication at the pad borders but, at the same time, a faster operation. Namely, the electrons can follow a shorter path to the collection electrodes and do not have to travel through regions characterized by a low horizontal electric field. The experimental results obtained from the characterization of the pixel arrays with these two termination layouts will be presented in Section 4.4.

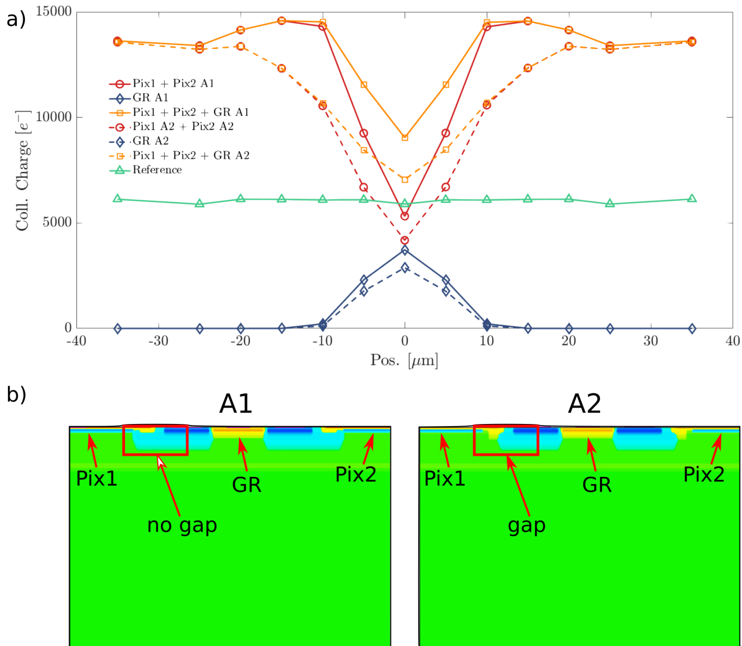


Figure 4.1.10: (a) Charge collection comparison for the two considered termination layouts of the rectangular pixels with integrated gain layer. (b) Details of the employed simulation domains.

4.2 Electrical characterization

4.2.1 Process control structures

In order to characterize the employed technology, a group of process control structures was included on the backside of the

passive test chips fabricated within the SEED project. In particular, a gated diode was used to evaluate the surface generation velocity at the interface between the silicon substrate and the backside passivation layer and a MOS capacitor was employed to determine the equivalent SiO_2 thickness of the passivation layer and the concentration of positive charges in the silicon dioxide [16].

A probe station with needle connectors connected to a Keithley 4210 Parameter Analyzer was used to perform most of the measurements that will be presented in this Section. Instead, in the measurements where an high bias voltage exceeding 400 V was needed, a Keithley 2410 or alternatively a Keithley 2470 were employed to bias devices under test through a script developed with Matlab.

Measuring the IV characteristics of the gated diode through the procedure explained in [96], [97], it was possible to estimate the characteristic surface generation velocity s_0 of the devices analyzing the current component associated to the surface leakage current of the gated diode. The following biasing scheme was employed in the measurements: the backside surface region was reverse biased applying a negative voltage of -5 V to the diode cathode and, at the same time, the diode gate voltage was swept from accumulation to strong inversion and backwards. The acquired IV characteristics, showing the diode current as a function of the applied gate voltage, are reported in Figure 4.2.1 for a positive and a negative sweep of

the gate voltage.

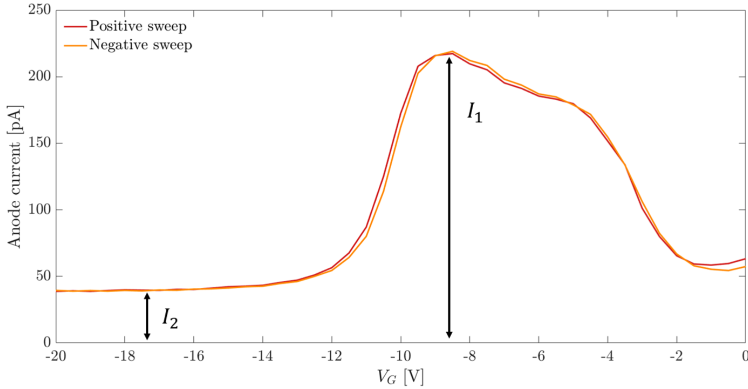


Figure 4.2.1: Gated diode anode current as a function of the voltage applied to the gate. Picture from [16] (CC BY 4.0).

From the IV curve of the gated diode, it is possible to extract the current component associated to the surface generation I_S computing the difference between the maximum diode current measured in depletion condition I_1 and the diode current in strong inversion I_2. Namely, in depletion condition the diode leakage current represents the sum of the currents due to the bulk and surface generation and the metallurgical junction leakage. Instead, when the applied gate voltage sets the diode in strong inversion, the current contribution due to the surface generation is strongly reduced [16]. According to [96], [97], the surface generation velocity can be estimated applying eq. 4.1, where n_i represents the intrinsic carrier density at room temperature and A_g is the total gate area resulting from the

sum of the finger areas of the comb-like structure of the gated diode.

$$s_0 = \frac{I_1 - I_2}{q n_i A_g} \tag{4.1}$$

The extracted surface generation velocities have been reported in a boxplot (Figure 4.2.2), where the values have been grouped according to the wafer from which the samples were extracted. The following conventions hold for all the boxplots reported in this manuscript: the boxes represent the data contained in the range between the 25th and the 75th percentiles, the whiskers include all the valid data points and the red lines and crosses stand for the median values of the measured data and for the outliers, respectively.

The obtained s_0 values were in the order of hundreds of cm/s and therefore higher than the values usually obtained for non-irradiated devices with thermally grown oxides [16]. According to these results, a value of the surface generation velocity equal to 200 cm/s was employed in the TCAD simulations with the passivation layer included on the backside surface.

In a similar way, the measured CV characteristics of the MOS capacitors have been used to estimate the concentration of positive charges trapped in the surface oxide and the thickness of the passivation layer. In the performed measurements, the gate voltage was swept from accumulation to strong inversion and backwards and a probe signal with a frequency of 10 kHz and an amplitude of 100 mV was employed for the

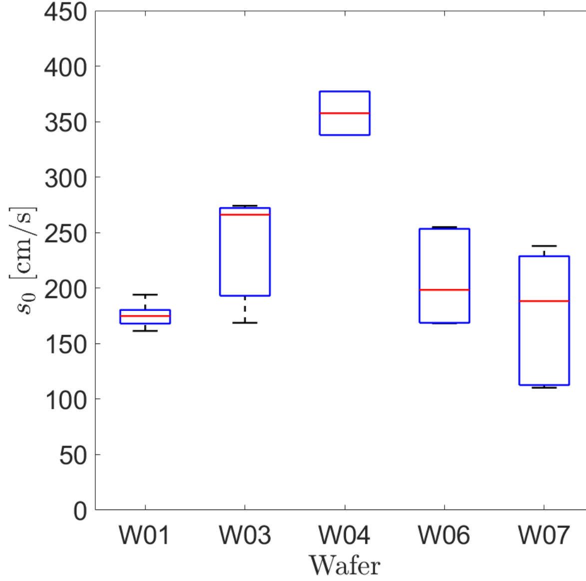


Figure 4.2.2: Surface generation velocity boxplot for the measured SEED wafers. Picture from [16] (CC BY 4.0).

AC analysis. The concentration of oxide charges, extracted according to eq. 4.2 from the measured capacitance in accumulation C_{ox}, have been reported in Figure 4.2.3, where the results have been subdivided in the boxplot according to the sample wafers.

$$Q_{ox} = \frac{(\Phi_{ms} - V_{fb})\, C_{ox}}{qA_g} \tag{4.2}$$

In the above equation Φ_{ms}, V_{fb} and A_g represent the alu-

minum to n-type silicon workfunction, the MOS flatband voltage and the gate area, respectively.

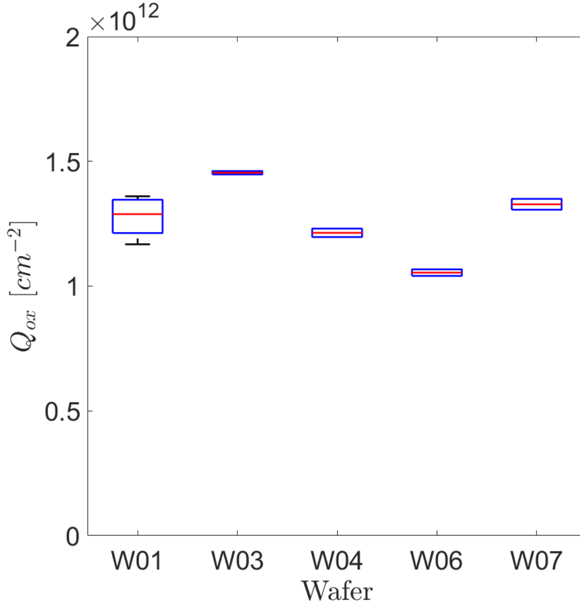


Figure 4.2.3: Boxplot of the oxide charge concentrations extracted from the different SEED wafers. Picture from [16] (CC BY 4.0).

All the extracted Q_{ox} values were in the interval between $1{\times}10^{12}$ and $1.5{\times}10^{12}\text{cm}^{-2}$ and showed a low variability among the samples extracted from the same wafer.

4.2.2 Termination structures

Backside termination structures

In addition to the aforementioned test structures, a group of backside diodes with variable guard ring number and guard ring pitch was included in the SEED and ARCADIA test chips to determine the effect of the termination geometry on the backside bias voltage associated to the junction breakdown. The results obtained from the simulations of the different termination structures, where an oxide charge concentration within the range estimated experimentally was considered, have been included in the following boxplots. In these two Figures 4.2.4 and 4.2.5, a comparison between the simulated and measured breakdown voltages for the SEED backside diodes with different guard ring number and guard ring pitch is shown [16].

In the Figures, the boxes represent the breakdown voltages measured on the backside diodes of 22 different samples extracted from 7 wafers produced within the SEED project, while the dashed orange lines represent the simulated breakdown voltages for an oxide charge concentration equal to 1 $\times 10^{12}\text{cm}^{-2}$. As expected from TCAD simulations, which provided an excellent agreement with the experimental data, an higher guard ring number guarantees a higher breakdown voltage and, at the same time, a guard ring pitch between 6 and 7 μm is able to provide the highest breakdown voltages

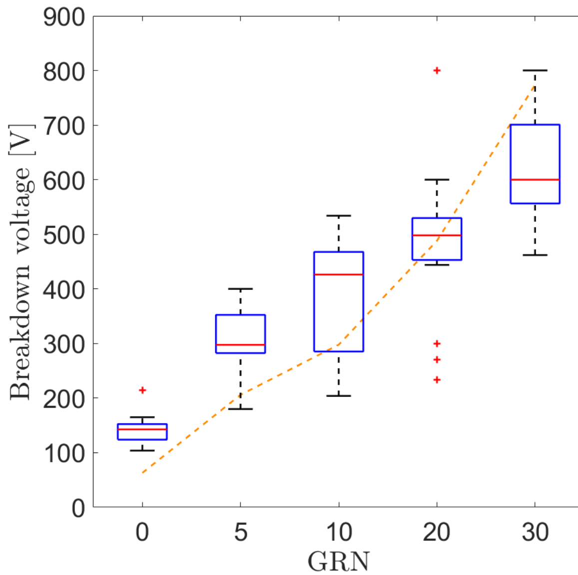


Figure 4.2.4: Boxplot of the breakdown voltages measured on the SEED backside diodes with variable guard ring number. Picture from [16] (CC BY 4.0).

[16].

Frontside termination structures

The sensors realized on the thin n-type epitaxial substrates and on the high resistivity n-type substrates with 100 μm thickness do not have any termination structures on the device backside and, as a consequence, the backside junction reaches the chip borders. The wafer dicing, which was performed

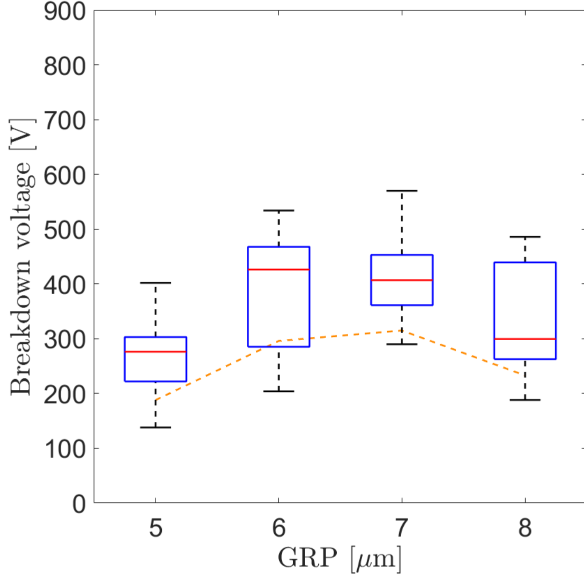


Figure 4.2.5: Boxplot of the breakdown voltages measured on the SEED backside diodes with variable guard ring pitch. Picture from [16] (CC BY 4.0).

through the mechanical action of a diamond saw, left a damaged lateral surface at the chip borders corresponding to the cut planes. Therefore, a high concentration of defects is present at the chip sides, which act as a source of e^{-}-h^{+} pairs. The charges generated in those regions can lead to high currents, which affect the proper chip behavior. On the other hand, the border conductivity can be exploited to bias the chip backside electrode applying a negative bias to the front-

side external pwell. To enable the application of a negative voltage in the order of a few tens of volts to the external pwell, dedicated frontside termination structures have been designed. Figure 4.2.6 shows a schematic cross section of these structures realized at the chip borders. In the cross section, it is possible to observe the p-type floating guard ring that has been included to increase the breakdown voltage associated to the frontside external pwell and the n-type guard ring that can be biased to increase the bias voltage associated to the onset of the punch-through between external and internal pwells.

Test structures designed with different layouts of the frontside terminations have been also included in the test chips of the first ARCADIA engineering run to evaluate their capability to avoid possible issues related to breakdown or punch through effects, when the test structures were biased from the frontside external pwell.

The performance of the different layouts of the frontside test structures have been evaluated measuring the current on the frontside internal pwell electrode as a function of the negative bias voltage applied to frontside external pwell. Three different values for the voltage applied to the frontside n-type guard ring equal to 0, 1 and 2 V have been considered in the performed measurements. The measured internal pwell currents for the three guard ring voltages and three different n-guard ring width equal to 20, 30 and 40 μm have been reported as an example in Figure 4.2.7. As expected, the exponential in-

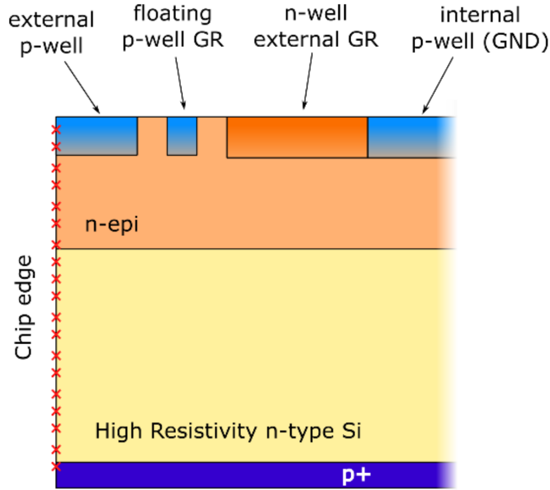


Figure 4.2.6: Schematic cross section of the frontside termination structures.

crease in the measured current related to the punch through appears at higher bias voltages for increasing n-guard ring thicknesses. In an analogous way, an increase in the applied guard ring voltage guarantees a higher punch-through onset voltage.

The extracted voltages at the onset of the punch through for the three considered test structures included in the test chips originating from different wafer positions have been reported in the boxplot of Figure 4.2.8.

The non linear dependence of the punch through voltage on the guard ring width can be clearly observed in the Figure,

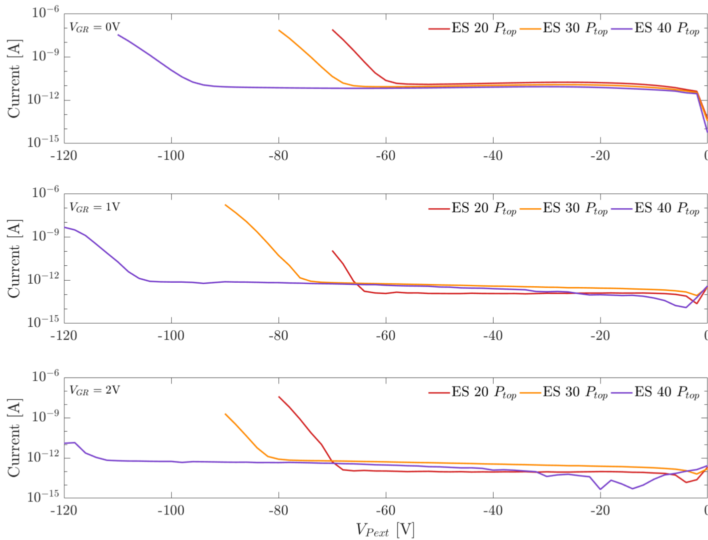


Figure 4.2.7: Measured internal pwell currents for three guard ring voltages (V_{GR}) and three termination layouts.

where it is also possible to notice the almost linear increase in the punch through voltage for increasing V_{GR}. The obtained results enabled to determine the minimum guard ring width and, thus, the resulting minimum dead area surrounding the device active region, corresponding to the termination structure width, for the two different substrate thicknesses of 48 and 100 μm that were expected to have the possibility be biased both from the backside and from the frontside.

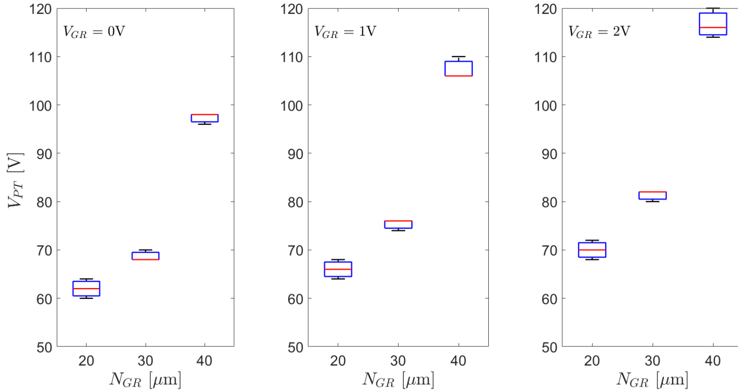


Figure 4.2.8: Extracted punch through voltages (V_{PT}) for three guard ring voltages (V_{GR}) and three termination layouts.

4.2.3 Passive pixel arrays

Most of the passive test structures fabricated within the SEED and ARCADIA project were composed of passive pixel arrays having rectangular or squared pixels with pitch sizes ranging from 10 to 250 μm. In these structures, the n-type collection electrodes of the pixels were connected in parallel to a common readout electrode. In addition to the collection electrode, two additional electrodes were present on the frontside of these test structures to contact the frontside n-type guard rings and the frontside pwell. Finally, an additional fourth frontside electrode was available on the ARCADIA passive pixel arrays to apply the negative bias voltage to the external pwell. Figure

4.2.9 shows the micrographs of two ARCADIA passive pixel arrays with 0.5×0.5 mm^2 matrix area, where the four different electrodes have been pointed out.

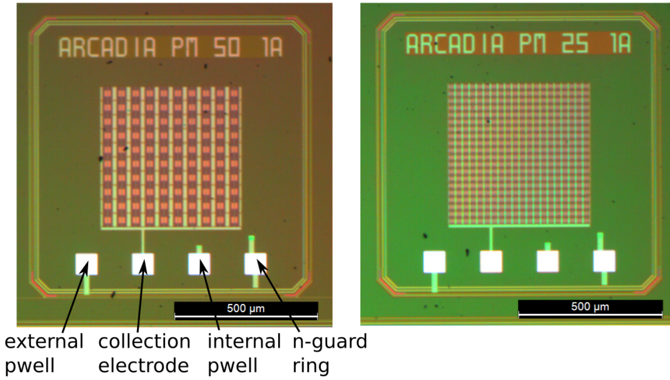


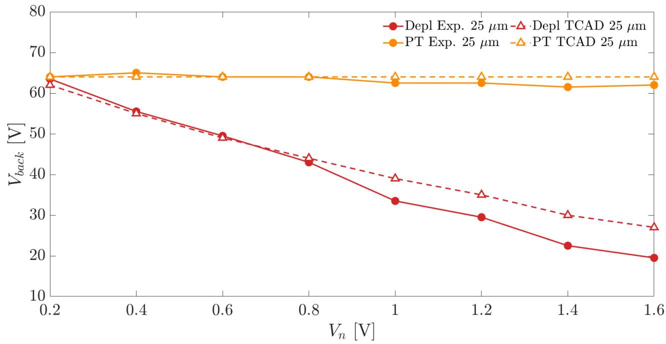
Figure 4.2.9: Micrographs of two passive arrays with 50 and 25 μm pixels and 0.5×0.5 mm^2 active area.

The comparison between the measured and simulated IV characteristics of the passive pixel arrays with 25 and 50 μm pixel pitch and standard pixel layout, that were included in the SEED test structures, showed an good agreement between the experimental and simulation results [16]. The experimental measurements proved that it was possible to apply a bias voltage able to fully deplete sensor substrates with thicknesses up to 300 μm from the backside electrode without any breakdown issue. As expected, the backside termination structures included around the SEED passive pixel array and composed of 20 floating guard rings with 6 μm pitch were able to guar-

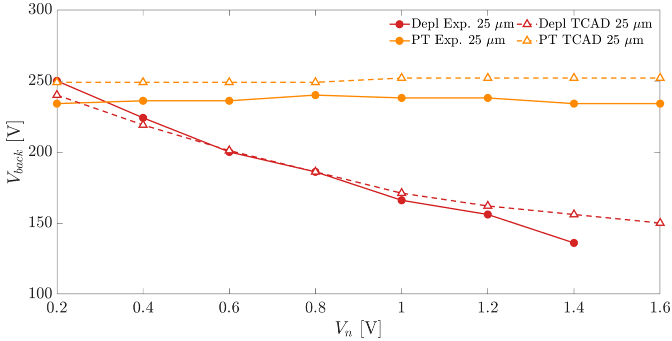
antee a breakdown voltage higher than the operating voltage range of the devices [16].

The punch through (V_{PT}) and full depletion (V_{depl}) voltages have been extracted from the measured SEED nwell and pwell currents, according to the procedure explained in [16], and then compared with the values estimated from TCAD simulations performed on domains with same substrate thickness and pixel pitch. The obtained values of V_{PT} and V_{depl} have been reported in Figures 4.2.10a and 4.2.10b, for a substrate thickness of 100 μm and 300 μm, respectively [16]. As expected from simulations, an increase in the applied V_n resulted in a decrease in the full depletion voltage, while the punch through voltage remained almost unaffected from the variation in the applied nwell voltage.

In an analogous way, the IV characteristics of the ARCADIA passive pixel arrays have been measured and compared with TCAD simulations, see Figure 4.2.11. As previously mentioned, devices with three different substrate thicknesses have been produced in the three ARCADIA production runs delivered in 2021, 2022 and 2023. The tested passive pixel arrays included the different layouts of the 50, 25 and 10 μm pixels selected on the basis of preliminary TCAD simulations. In addition to the several small pixel arrays with active area equal to 0.5×0.5 mm^2, that were labeled as SPM, two pixel arrays with larger matrix area equal 1.5×1.5 mm^2, called PM, have been realized. Having a smaller total capacitance, the



(a) *Substrate thickness 100 μm*



(b) *Substrate thickness 300 μm*

Figure 4.2.10: V_{PT} and V_{depl} as a function of the applied frontside nwell voltage V_n. Pictures from [16] (CC BY 4.0).

pixel arrays with smaller area can provide a better response in the measurements with a fast laser pulse. On the other hand, the larger arrays are easier to characterize electrically due to their larger total capacitance and the higher currents

measured at the pwell and at the collection electrodes. The pixels included in the two PM and in the two SPM having 50 and 25 μm pixels labeled with the flag 1A present the same layout of the pixels in the SEED test structures. The SPM presenting pixel layouts designed to enhance the charge collection speed, characterized by the largest dimensions of the charge collection electrode, have been labeled with the flag 3A and, instead, the ones having the layouts with smallest collection electrode size, which are expected to provide the smallest pixel capacitance values, have been called 2F and 2C for the 50 and 25 μm pixel arrays, respectively. Finally, two SPM with 50 μm pixels having same collection electrode size of the layouts 1A and 2F but different pwell dimension have been also considered to provide a complete picture of the influence of these design parameters on the pixel performance. A pad diode with same area of the small pixel arrays, named PAD 500, was also included to provide a comparison with the pixel arrays and to determine the operating voltage range of the COBRA chip.

Comparing the results of TCAD simulations with the measured IV characteristics of the ARCADIA passive pixel arrays, it was possible to notice a further improvement in the already good agreement level reached with the experimental data of the SEED samples. Figure 4.2.11 shows the mean value and the associated standard deviation computed from the pwell and nwell currents measured on four PM with 50 μm pixels

contained on four samples coming from different wafer positions. If not stated differently, in the IV measurements a positive voltage equal to 0.8 V has been applied to the collection electrode of the pixel arrays (V_n) in combination with a slightly higher guard ring voltage equal to 0.81 V (V_{GR}) to enable a small current flow in the resulting resistive path between the pixels and the guard ring surrounding the pixel array. Monitoring this current, it is possible to get information on the negative bias voltage needed to choke the conductive path and thus able to isolate the pixels from the guard ring, when the backside space charge region reaches the frontside electrodes. The measurements of the PAD diode IV characteristics represented special cases, where higher nwell and guard ring voltages up to 3 V have been applied. Namely, the electronics embedded in the COBRA chip has been designed to be biased at 3.3 V and, as a consequence, the PAD diodes have been tested in similar bias condition to extract the operating voltage range that were expected to be the same of the COBRA chips. The IV characteristics reported in Figure 4.2.11 were measured on four samples extracted from a wafer with a nominal active thickness of 48 μm and, therefore, an active thickness within the variability range provided from the foundry was considered in the performed TCAD simulation, that has been reported in the comparison.

An excellent match can be observed between the simulated pwell current and the mean value of the corresponding exper-

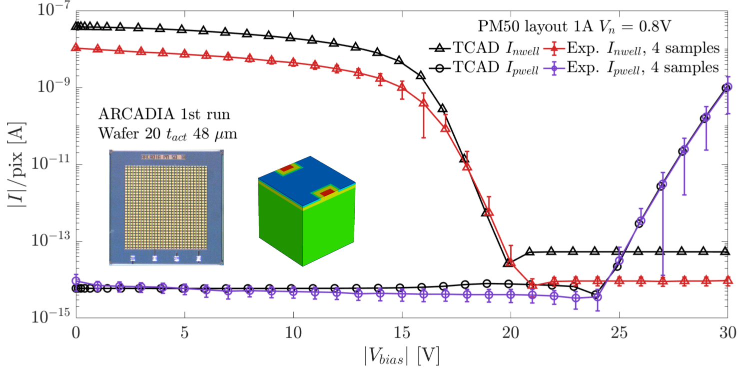


Figure 4.2.11: Simulated and measured pwell and nwell IV characteristics for 50 μm pixels with layout 1A and 48 μm nominal substrate thickness.

imental data and, instead, a small difference is still present in the collection electrode currents, where the measured pixel dark current showed to be lower than the simulated one. This meant that the real minority carrier lifetime was lower than the value considered in the simulations.

Applying the procedure explained in [98], the full depletion and punch through voltages have been extracted from the IV curves for for pixel and PAD diode test structures with different layout and substrates, produces in the first two runs of ARCADIA. The extracted V_{PT} and V_{depl} for the passive matrices with 25 μm pixels (PM 25) have been compared in Figure 4.2.12, where the boxplots of the punch through and the full depletion voltages have been reported in the first row

and second row panels, respectively [98].

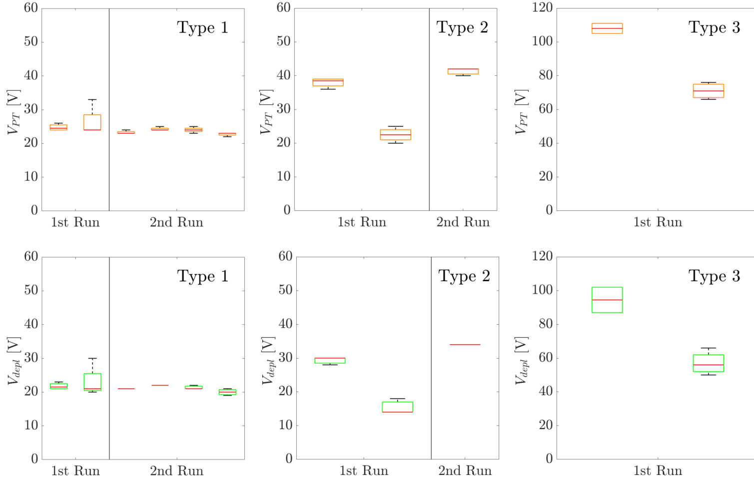


Figure 4.2.12: Boxplots of the measured V_{PT} and V_{depl} for the PM 25 with different substrate types.

The extracted values have been subdivided in three columns showing the boxplots of V_{PT} and V_{depl} measured on devices with three different substrate types. Type 1 wafers were produced starting from a p^+ substrate, where two n-type epitaxial layers with increasing doping concentrations were grown in sequence. These wafers are characterized from the lowest nominal active thickness equal to 48 μm resulting from the sum of the n-type epitaxial layer thicknesses [98]. Type 2 and 3 wafers were instead realized using n-type high resistivity substrates with nominal active thicknesses of 100 and 200 μm, re-

spectively. An additional backside lithography step has been performed on the 200 μm thick wafers in order to create the backside floating guard rings needed to prevent the junction breakdown, when the backside bias voltage is applied [98]. A lower variability in the extracted V_{PT} and V_{depl} values has been observed for the wafers having type 1 substrate produced in the second run. As expected, the larger variability in the extracted voltage values was observed in the thickest samples, while the significant difference in the median V_{PT} and V_{depl} values obtained from the different wafers having type 2 and 3 substrates is related to different thicknesses of the n-type epitaxial layer or to different doping concentration of the high resistivity n-type substrate [98].

The previous V_{PT} and V_{depl} values were also compared with the ones extracted from the IV characteristics of devices from type 1 and 2 wafers biased from the frontside. An example of this comparison has been reported in [98] for the tested PM 25, where it was experimentally proved that the two biasing schemes provided similar results and, therefore, can be independently used to bias the designed sensors for substrate thicknesses up to 100 μm.

In an analogous way, the operating voltage range (ΔV) of the considered PM 25, computed as the difference between V_{PT} and V_{depl} [98], have been compared in the boxplots of Figure 4.2.13. In these graphs, it is possible to observe the expected increase in the median value of the operation voltage range

and in the associate variability for increasing substrate thicknesses. Moreover, the operating voltage range showed a small variability for the wafers produced with same substrate type and demonstrated to be almost constant for different epitaxial layer thicknesses. Therefore, this proves that a variation in the epitaxial layer thickness results in a simple shift of both V_{PT} and V_{depl} to higher or lower values [98].

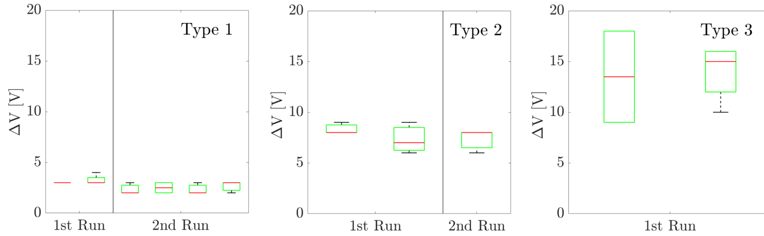


Figure 4.2.13: Boxplots of the operating voltage range for the measured PM 25 with different substrate types.

A comparison of the V_{PT} and V_{depl} extracted from the passive pixel arrays with different pixel pitch and standard layout 1A is shown in Figure 4.2.14. Again the experimental results confirmed the trend predicted by the preliminary simulations with a higher operating voltage range for the 10 μm pixels. Namely, the median value of the full depletion voltages for the smaller pixels is higher than the median values of the punch through voltages for the larger pixel pitches and, thus, these structures cannot be biased properly if included on the same chip.

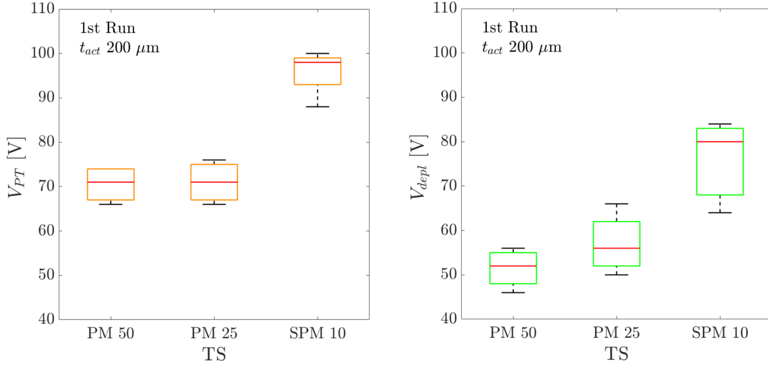


Figure 4.2.14: Boxplots of the extracted V_{PT} and V_{depl} for the passive pixel arrays with 50, 25 and 10 μm pitch.

In a similar way, the pixel dark currents have been extracted from the plateau in the nwell currents appearing for applied bias voltages higher than V_{depl} [98]. The boxplots in Figure 4.2.15 show the dark current of a single pixel with 25 μm pitch for an applied bias voltage equal to V_{PT} [98]. These values came again from the measurements performed on the PM 25 of the wafers produced in the first and second silicon run. As expected, an increase in the pixel dark current can be observed in the wafers of the first silicon run with increasing substrate thickness. The dark current increase is related to the increasing current contribution related to the thermal generation in the larger depleted volumes as a consequence of the thicker active substrates [98]. Lower dark current values have been reported for the PM 25 measured from the wafers of

the second ARCADIA production with similar median values for the type 1 wafers and the only tested type 2 wafer.

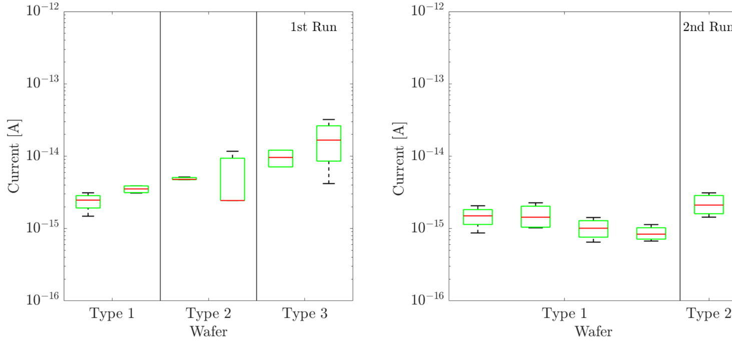


Figure 4.2.15: Boxplot of the pixel dark current for the PM 25 with different substrate types.

The pixel leakage current measured on a LF-Monopix2 chip having 100 μm substrate thickness for an applied voltage bias $\sim$ 100 V, which is in the order of 5×10^{-13} A at room temperature [99], is comparable or slightly higher than the dark current of a group of 12 ARCADIA 25 μm pixels with same substrate thickness (Type 2), which together cover a total area equal to the one of a single LF-Monopix2 pixel.
Once determined the operating voltage range of the different test structures, the CV characteristics of the devices have been measured at the probe station to retrieve the value of the pixel capacitance for the different layouts. In the performed tests, a fixed negative bias voltage larger than the measured V_{depl} was applied to the backside electrode or, alternatively,

to the external pwell. At the same time, the collection and the n-guard ring electrodes were biased at 0 V and, finally, a negative voltage sweep was applied to the frontside internal pwell to deplete the sensor epitaxal layer [95]. An AC probe signal with a RMS amplitude of 100 mV and a frequency of 100 kHz was applied between the pwell and the collection electrode to perform the AC analysis. The pixel capacitance values obtained from the small passive pixel arrays with different layouts of the 50 and 25 μm pixels have been reported in Table 4.2 and Table 4.3. The values reported in the Tables have been estimated from the CV characteristics for an applied pwell voltage of -0.8 V and represent the mean value and the associated standard deviation computed on a group of four samples extracted from different wafer positions. The parasitic capacitance contributions due to the metal pads and to the metal lines has been estimated and subtracted from the estimated C_{pix} reported in the Tables. According to [100], this parasitic contribution has been computed using the empirical expression derived by Meijs and Fokkema [101] on the basis of the Sakurai's approach.

As expected, the lowest capacitance values have been measured on the pixel arrays with layout designed to minimize the pixel capacitance i.e. 2F and 2C for the 50 and 25 μm pixels. These layouts were characterized by the smallest collection electrode sizes for both pixel pitches. Instead, the pixel layouts with the largest collection electrode sizes, labeled as 3A,

Table 4.2: Measured C_{pix} for the different SPM 50 layouts

Layout t_{act} [μm]	1A [fF]	1C [fF]	2A [fF]	2F [fF]	3A [fF]
48	15.1±0.4	11.6±0.2	12.3±0.4	3.5±0.4	17.8±0.5
100	15.5±1.1	11.5±0.5	12.2±0.8	3.5±0.3	18.2±0.6

Table 4.3: Measured C_{pix} for the different SPM 25 layouts

Layout t_{act} [μm]	1A [fF]	2C [fF]	3A [fF]
48	4.4 ± 0.3	2.5 ± 0.1	9.1 ± 0.2
100	4.7 ± 0.4	2.7 ± 0.2	10.5 ± 2.8

that were designed to improve the charge collection speed at the pixel corners, provided the largest pixel capacitance values and thus confirmed the simulation predictions as well.
In comparison to other MAPS technology, which follow a similar pixel design characterized by a small collection electrode, the measured capacitance value for the 25 μm pixels having layout 1A, i.e. the same layout of the pixels included in the MD chip, is slightly higher than the capacitance of the 28 μm pixels included in the ALPIDE chip and of the 33 μm pixels included in the TJ-Monopix2 chip equal to ~ 2.5 fF and ~ 3 fF, respectively [102], [103]. The ALPIDE and the TJ-Monopix2

pixel capacitance values are instead comparable with the one measured on the 25 μm pixels with layout 2C.

4.2.4 Passive pixel arrays with gain layer

The IV characteristics of the passive pixel arrays with integrated gain layer and large pixel sizes, that were included in the third production run, have been also measured to estimate V_{PT} and on the nwell voltage associated to the breakdown of the frontside junction (V_{bd}). Figure 4.2.16 shows in the first row the measured pwell currents as a function of the negative bias voltage (V_{bias}) applied to the backside p-type contact of two pixel arrays having rectangular pixels with layout A1. In the second row, the collection electrode currents measured on the same test structures as a function of the voltage applied to the n-type electrode (V_n) are reported. As usual, the dip in the pwell current has been employed to estimate the punch through voltage, while the voltage associated to the breakdown of the frontside junction can be clearly established from the abrupt increase in the collection electrode current.

CV measurements have been also performed on the passive pixel arrays with large pixel size and integrated gain layer to estimate the gain layer profile from the measured CV characteristics. Namely, gain values lower than the ones expected from TCAD simulations were observed in the preliminary results obtained from the optical characterization of the passive pixel arrays. This was a first indication of a possible mismatch

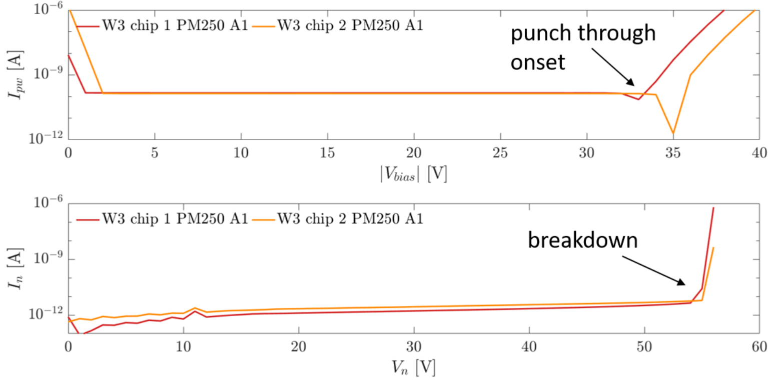


Figure 4.2.16: Measured pwell and nwell currents as a function of the applied V_{bias} and V_n [104].

between the actually implanted gain profile and the one designed in the simulations. According to [105], the relationship described in eq. 4.3 can been exploited to compute the doping concentration N(x) of a generic abrupt pn junction as a function of its depth (x) inside the substrate material, that can be also characterized by a non uniform doping concentration. The value of x, which represents the depth of the doping concentration profile, can be instead computed using 4.4 [105].

$$N(x) = \frac{2}{q\epsilon_s \frac{d(1/C^2)}{dV}} \tag{4.3}$$

$$x = \frac{\epsilon_s}{C(V)} \tag{4.4}$$

The gain layer profiles estimated using the previous equa-

tions confirmed the hypothesis of a mismatch in the implanted gain layer. A final check performed by the foundry confirmed that the profiles used in the design phase were obtained with a different energy w.r.t. the ones actually implanted. The TCAD simulations performed with a new gain layer profile with the correct implantation implant energy reached again a good agreement with the experimental data providing a gain value ranging from 2 to 4. Further details on this topic and on the obtained results can be found in [106].

4.3 X-ray irradiation studies

An extensive irradiation campaign has been performed to evaluate the radiation hardness of the different pixel layouts and pixel pitches to increasing TID resulting from their irradiation with an X-ray tube with tungsten anode. The results obtained from the experimental measurements of the pixel arrays IV and CV characteristics have been compared with the corresponding TCAD simulation and were published in [64], [95]. The employed X-ray tube, which is located at University of Padova, is characterized by a peak photon energy of 10 keV and is able to deliver 2 Mrad/h in standard conditions at room temperature [107]. The samples used for the irradiation studies were extracted from wafers of both the SEED and the ARCADIA productions having nominal active substrate thicknesses of 48 and 100 μm. The devices were irradiated in

four steps corresponding to doses of 0.01, 0.1, 1 and 10 Mrad. After each irradiation step an annealing treatment was performed, keeping the samples inside a climatic chamber for 10 min at 80 °C [95]. An X-ray source emitting photons with such low energy is able to contribute only to the surface damage of the irradiate devices, creating positive charges in the passivation layer and traps at the interface between silicon and silicon dioxide [95]. As explained in Chapter 3, the radiation damage for increasing X-ray TID has been modeled employing the 'new Perugia' radiation model and the initial concentrations of surface traps and positive charges in the oxide were chosen according to the Hamamatsu parametrization [95]. As expected from the preliminary simulations, an increase was observed in both the pixel leakage current and the pixel capacitance for increasing radiation doses. The increase in the measured leakage current is related to the effect of the surface traps that behave as generation centers when subjected to an electric field and, thus, contribute to the increase in the surface current component [95]. A clear example of this effect can be observed in Figure 4.3.1, where the nwell and pwell currents of a pixel array with 50 μm pixels and 48 μm active substrate have been reported as a function of the applied bias voltage. The pixel dark current, that before the irradiation was in the order of few fA, increased by orders of magnitude reaching a level in the pA range for a TID of 10 Mrad.

In an analogous way, the expected increase in the pixel capa-

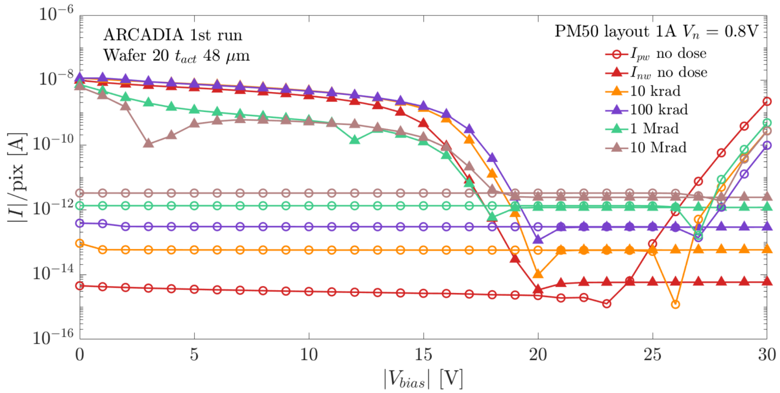


Figure 4.3.1: Measured pwell and nwell currents as a function of the applied V_{bias} for increasing TID values.

citance (C_{pix}) was observed for increasing radiation doses and the collected CV characteristics have been reported in Figure 4.3.2 for the measured pixel arrays with 50 μm pixels having the same layout and extracted from the same wafer of the device mentioned above. The simulations showed that the increase in the pixel capacitance is related to the concentration of positive charges in the silicon dioxide layer, which attract electrons from the epitaxial layer resulting in an accumulation of negative charges below the Si-SiO_2 interface. This leads to the appearance of an additional surface capacitance contribution and, as a consequence, to an increase in the measured C_{pix} [95].

After an initial small increase in the measured capacitance for

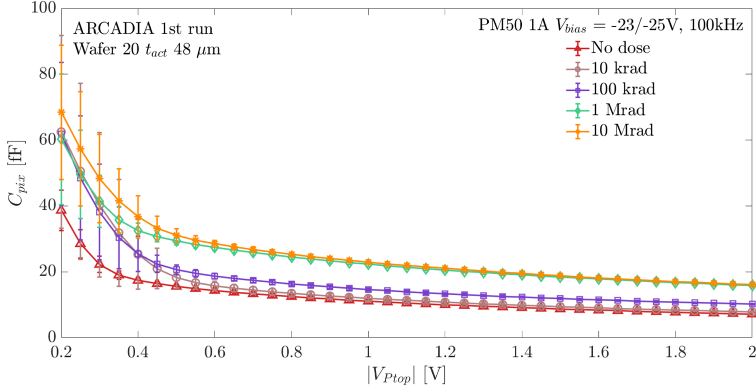


Figure 4.3.2: Measured pixel capacitance for increasing TID values.

X-ray doses up to 100 krad, it is possible to notice a significant jump in the plotted curves with the pixel capacitance that nearly doubles considering a TID of 1 Mrad. Finally, for the highest radiation dose equal to 10 Mrad no significant increase can be observed in C_{pix} with the capacitance value that saturates around the level reached for a TID of 1 Mrad.

The complete and detailed comparison of the measured C_{pix} values for all the considered layouts of the irradiated 25 and 50 μm pixel arrays can be found in [64], [95].

4.4 Optical characterization

4.4.1 Laser setup

Once characterized from the electrical point of view, the dynamics response of the small passive pixel arrays and of the PAD diodes, having same active areas equal to 0.5×0.5 mm^2, have been tested in an optical setup with a fast pulsed IR or, alternatively, red laser. The employed IR and red laser diodes have wavelengths equal to 1060 and 660 nm and are able to provide a pulse length at FWHM in the order of less than 100 ps and 350 ps, respectively. Figure 4.4.1 shows a picture of the optical setup together with a simplified schematic representation of the laser focusing system [20]. The light pulse is launched into a single-mode optical fiber connected to an achromatic collimator mounted at the entrance of the focusing system. Once collimated, the optical pulse reaches a 2 inches beam expander and goes through 90-10 beam splitter crystal cube. The beam splitter sends 90% of the incident light to a plano-convex lens having a focal length of 100 mm. The lens focuses the incident light in a spot with a diameter in the order of 10 μm at FWHM on the focal plane where the Device Under Test (DUT) is placed. A second 2 inches beam expander is attached to the beam splitter and mounted coaxial to the optical column. On top of the beam expander, a camera with tunable focal length is present and can be used to acquire images of the DUT and to adjust the laser spot position on the

focal plane acting on two step motors, which control the x-y position of the optical column [20]. The step motors can be controlled remotely using a dedicated script developed in Matlab, which enables the simultaneous and synchronous control of an oscilloscope (Tektronix MDO3102) having a bandwidth of 1 GHz, that has been used to acquire the amplified detector signals.

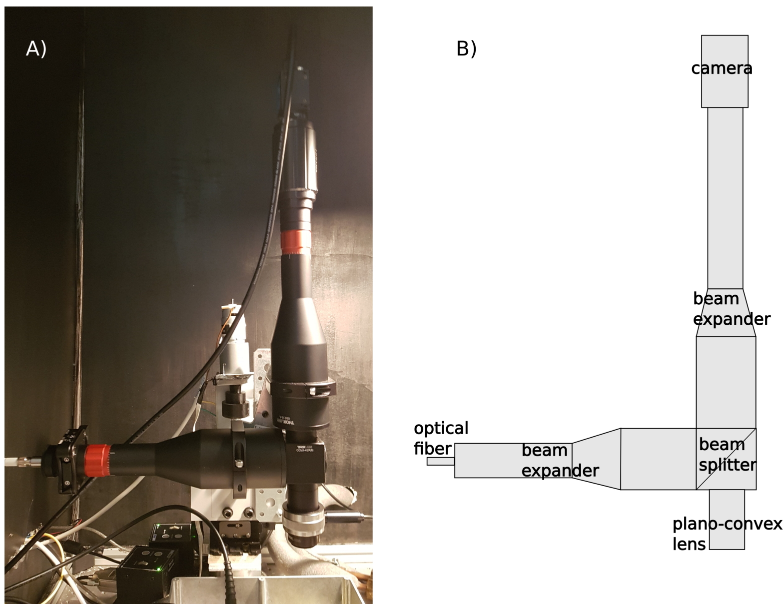


Figure 4.4.1: (A) Picture of the optical setup showing the focusing system with the embedded coaxial camera. (B) Schematic representation of the focusing system. Picture from [20] (CC BY 4.0).

Two different commercial charge amplifiers have been em-

ployed in the performed measurements to amplify the signals coming from the pixel matrices and from the PAD diodes. In particular, a MiniCircuits ZFL-1000LM amplifier with a gain of 23 dB and a bandwidth of 1 GHz was used in the optical test of the passive test structures without gain layer. Instead, a Hamamatsu C5594 amplifier with a cutoff frequency of 1.5 GHz and a gain of 36 dB has been employed in the characterization of the test structures with integrated gain layer designed for timing applications and in the measurements of the PAD diodes and of the pixel arrays with pad-like layout.

The optical characterization of the passive test structures has been performed illuminating the backside surface of the samples through a hole drilled in the PCBs, where the chips have been glued and wire bonded. In the measurements of the pixel arrays without gain layer, custom designed passive PCBs have been used to properly bias the bonded sensors, filtering the noise components of the power supplies, and to hold the sensors in the proper position. These PCBs were mounted in a metal box made of aluminum in order to shield the tested device from the environmental EM noise and a hole in the box lid was realized to enable the illumination of the sensors with the laser source. Measurements have been performed both focusing or unfocusing the laser spot. The former enable to get information on the different response of the considered pixel layouts as a function of the laser spot position inside the pixel area. Namely, with a spot diameter in the order of 10 μm the

generated charges are contained in a small volume and, as a consequence, this enables the evaluation of the charge collection dynamics in a specific pixel area. The latter provide an overall response of the test structures that represents the sum of the contributions related to the collection of the charges generated all over the pixel volume [20].

4.4.2 ARCADIA passive pixel arrays

TCAD simulations have been performed to disentangle the contributions of the different pixel areas from the overall pixel signal, confining the charge generation within small selected pixel volumes. According to the simulations, the charges generated in the volume below the collection electrode are collected quickly due to the presence of an uniform and high electric field and, therefore, represent the main contribution in the first part of the acquired signals. On the contrary, the charges generated in the pixel periphery are forced to travel through regions with lower electric field and, as a consequence, represent the main contribution to the slower charge collection associated to the signal tail [20].
The effect of the applied bias voltage (V_{bias}) on the signal dynamics has been investigated using an unfocused laser spot covering most of the area of the tested passive pixel arrays. In Figure 4.4.2 the signals measured on a pixel array with 50 μm pixels and t_{act} equal to 100 μm are reported for different V_{bias} values. As expected, increasing the applied backside

bias voltage resulted in faster signals characterized by a higher peak amplitude shifted to an earlier time instant and an associated lower tail amplitude. The bias voltage increase led to a steeper signal rising edge that is a consequence of the higher electric field at the backside junction, which causes a faster acceleration of the charges generated in that region close to the backside electrode [20]. The applied voltage bias was varied inside a wide range that included both the full depletion and the punch through voltage. Namely, a voltage bias slightly higher than the punch through voltage can be still safely applied without damaging the sensor, if the total power dissipation is under control and the total current remains in the μA range [20].

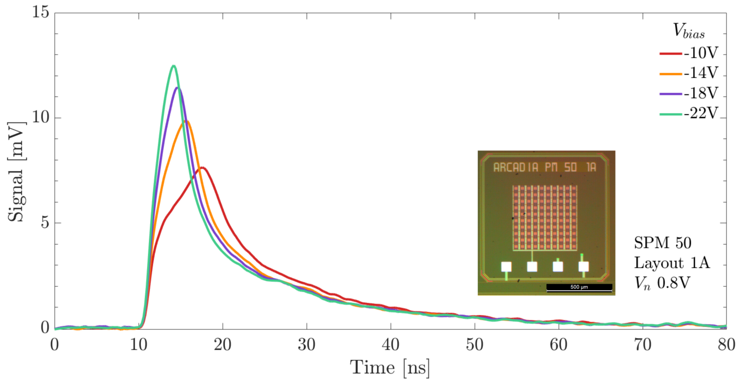


Figure 4.4.2: Acquired signals for the 50 μm pixels with layout 1A as a function of the applied V_{bias}.

In an analogous way, the charge collection dynamics of all

the produced passive pixel arrays with different layouts and pitch have been measured and compared with the behaviors expected from TCAD simulations. In order to provide a better comparison with the experimental results, a digital low pass filter reproducing the combined transfer function of the charge amplifier and of the oscilloscope was applied to the simulated data. Moreover, in order to further reduce the EM noise affecting the measurement setup, the bandwidth of the oscilloscope was limited to 250 MHz in the measurements of the passive pixel arrays with 50 μm pitch, which provided the smallest signals characterized by the slowest signal components. For these devices, it was noticed that neglecting the fastest signal components affected only marginally the final signal shape for those pixel arrays [20]. As a consequence, to provide a fair comparison with the corresponding TCAD simulations, a second digital filter tuned on this lower cutoff frequency was designed and employed in the comparison with the signals measured on the pixel arrays with 50 μm pixels. In this way, a good agreement was reached between the measured and simulated signals, providing an experimental confirmation of the reliability of the performed simulations. Figure 4.4.3 shows the comparison of the simulated and measured signals for three pixel arrays with 50 μm pitch having three different pixel layouts and a substrate active thickness equal to 100 μm.

In the first row, the results for the nominal layout (1A) having a medium size of the collection electrode are reported.

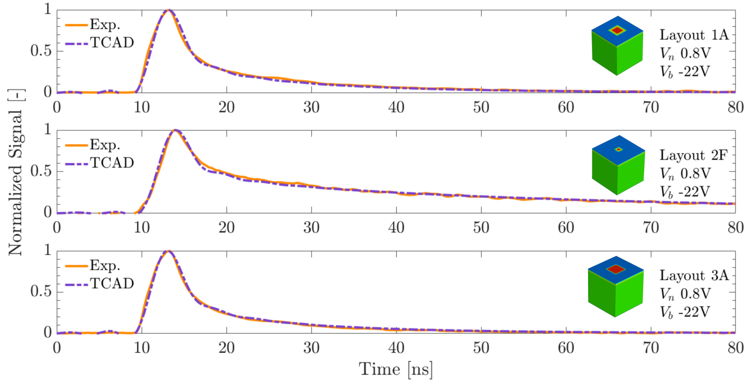


Figure 4.4.3: Acquired and simulated signals for the 50 μm pixels with nominal (1A), minimum capacitance (2F) and optimized charge collection (3A) layouts.

Instead, in the second and third row the results for the pixel layouts designed to minimize the pixel capacitance (2F) and improve the charge collection speed (3A) are displayed. As expected, the slowest signals have been acquired from the matrix with layout 2F designed to minimize the pixel capacitance and therefore characterized by the smaller collection electrode size and the larger pwell and deep pwell width. A significant signal tail amplitude is still present after 70 ns from the signal pulse, thus meaning that the charges generated at the pixel periphery are still slowly moving towards the collection electrodes. On the contrary, similar signals have been measured for the remaining layouts having larger collection electrode dimensions and almost same pwell and deep pwell width [20].

Similarly, the acquired and simulated signal for the pixel arrays with nominal active thickness of 100 μm and layout 1A having three decreasing pixel pitches equal to 50, 25 and 10 μm are compared in Figure 4.4.4.

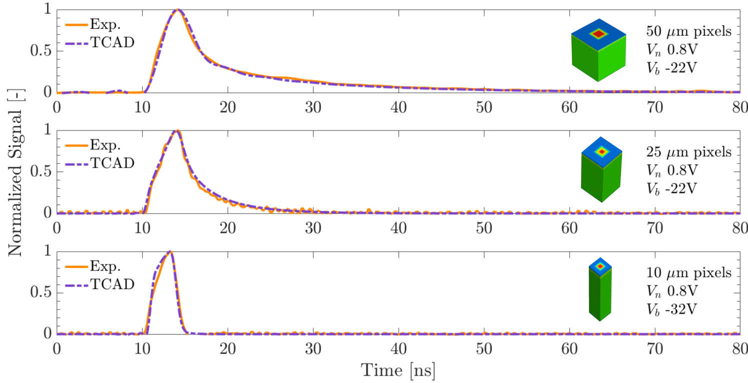


Figure 4.4.4: Acquired and simulated signals for the pixel arrays with nominal layout 1A and 50, 25 and 10 μm pixel pitch.

Again, it is possible to notice a good agreement in the displayed data and a faster charge collection associated to a decreasing pixel size [20]. This effect is related to the shorter distance among the collection electrodes in the pixel matrices with smaller pitch, which results in a shorter path to the collection nodes for the charges generated at the pixel sides or corners. As reported in the plot, a higher V_{bias} was applied in the test performed on the pixel array with smallest pixel size due to its different operating voltage range, shifted to higher

bias voltages.

The integral of the measured signals was computed to evaluate the time needed to collect the total amount or a fraction of the generated charges [20]. The obtained normalized integrated signals have been again compared in Figure 4.4.5 and in Figure 4.4.6 for the considered 50 μm pixel layouts and for the three pixel pitches, respectively. Looking at the comparison of the signal integrals for the pixel arrays with different layouts, the slower charge collection of the pixels with minimum capacitance layout (2F) is evident. Instead, the charge collection dynamics of the matrices with nominal (1A) and optimized charge collection (3A) layouts proved to be similar, with the latter providing a faster charge collection after the first nanoseconds [20]. This effect is related to the faster collection of the charges generated farther from the collection electrode, which move in a region with higher electric field for this second layout. In a similar way, the expected faster charge collection can be noticed comparing the integrated signals of the pixel arrays with decreasing pixel size. Looking at the time needed to collect 50% of the generated charges, the value decreases from around 8 ns for the larger pixels to 4.2 and 2.6 ns for the 25 and 10 μm pixels, respectively [20]. The same optical measurements were performed on several other test structures extracted from the wafers of the first and second ARCADIA silicon run.

The slow signals generated at the periphery of the sensor

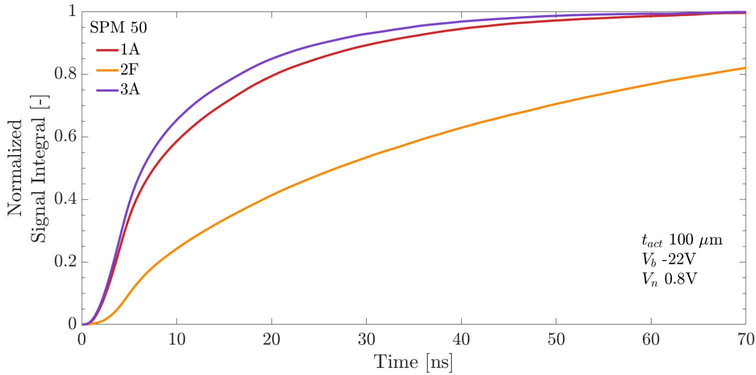


Figure 4.4.5: Normalized signal integrals for the 50 μm pixels with nominal (1A), minimum capacitance (2F) and optimized charge collection (3A) layouts.

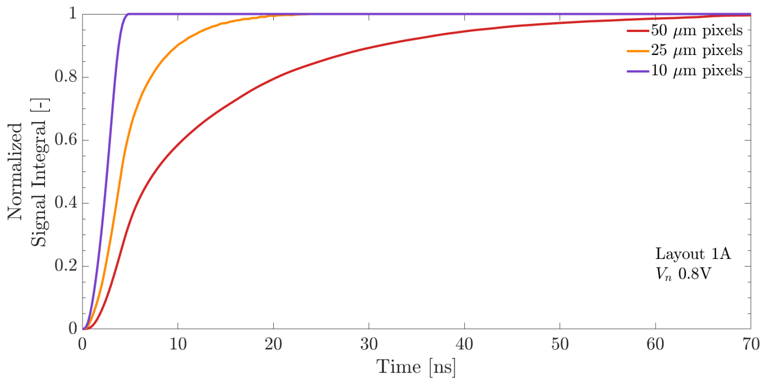


Figure 4.4.6: Normalized signal integrals for the pixel arrays with nominal layout 1A and 50, 25 and 10 μm pixel pitches.

electrodes should be minimized for high-precision timing applications, and thus a device with a large area to perimeter

ratio can provide a faster charge collection. On the other hand, if compared to a stand-alone PIN detector, the vertical field in the proposed integrated detector is not uniform and the charge-carrier velocity is not saturated in all the detector volume. Relevant information on the ultimate charge collection speed of a layout optimized for timing applications has been obtained on the PAD diodes with 0.5×0.5 mm^2 included in the test chips of the first ARCADIA production [108]. These structures showed the best timing performance with most of the generated charges collected within a few ns thanks to the more uniform electric field guaranteed by the larger collection electrode size. This led to the choice to include a few small passive pixel arrays with modified pixel design in the test chips of the second ARCADIA engineering run. Pixel pitches equal to 100 and 50 μm were chosen for these structures and the pixel layout was modified to maximize the n-type collection electrode size keeping a minimum pwell size able to guarantee the possibility to host the embedded frontend electronics. In Figure 4.4.7, it is reported a comparison of the normalized integrals computed from the signals of these structures connected to the faster Hamamatsu charge amplifier and acquired with a digital oscilloscope with 6 GHz bandwidth. The results refer to samples extracted from wafers with 48 μm nominal active thickness, which are expected to provide the best timing performance due to the shorter drift path to the collection electrodes for the generated charges.

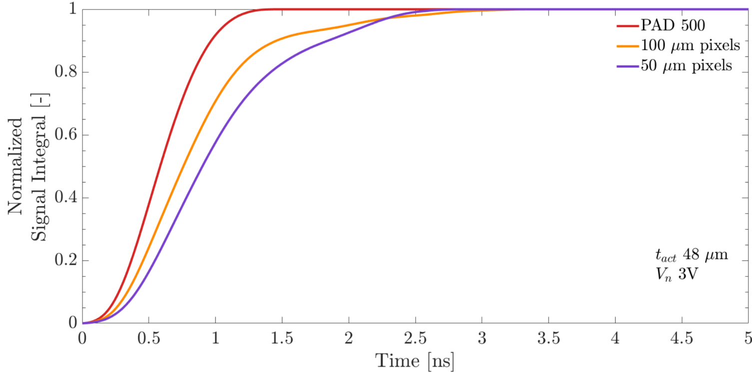


Figure 4.4.7: Normalized signal integrals for the PAD diode and the pixel arrays with PAD-like layout having 100 and 50 μm pitches.

The experimental data confirmed the expected behavior for these structures, which provided faster collection times in comparison to the pixel arrays with smaller pixel sizes. The time needed to collect 50% of the generated charges (t_{50}) estimated for the PAD diode and the pixel arrays with 100 and 50 μm pitch were in the order of 0.6, 0.75 and 0.9 ns, respectively, and therefore much lower than the t_{50} obtained with the previously tested arrays with smaller pixel sizes. This led to the conclusion that pixel sizes greater than or equal to 100 μm are needed in order to achieve the best timing performance and, thus, the three layouts of the pixel arrays with integrated gain layer, that were designed trying to further improve the achievable timing resolution, were characterized by

a minimum pixel size of 100 μm.

To evaluate the variation in the pixel response related to the collection of charges generated in different pixel positions, scans of the focused laser beam on the surface of the passive pixel arrays have been performed [20]. The preliminary acquisitions performed with the IR laser showed a position-dependence of the total integrated signal due to the back reflection of the IR light in the frontside metals and, therefore, a red laser with 660 nm wavelength, that is absorbed within a few tens of μm in silicon, was employed in the following acquisitions [20]. When the scan covered the whole backside matrix area, a motor step size of 10 μm was used, while in the scans performed on a smaller part of the array area, a finer step size equal to 5 μm was employed to capture smaller details increasing the spatial resolution [20]. An example of the acquired maps, showing the maximum peak amplitude as a function of the laser spot position on a whole passive pixel array area of 0.5×0.5 mm^2 or on a quarter of the total array area, are reported in Figure 4.4.8A and in Figure 4.4.8B for a pixel array having 50 μm pixels with layout 1A.

Looking at the signal map displayed in Figure 4.4.8B, performed with a finer motor step of 5 μm on a matrix quarter, it is easy to identify the position of the pixel centers corresponding to the yellow areas, where a higher signal was acquired. At the same time, the lower peak amplitude measured at the pixel borders and corners and the presence of the frontside guard

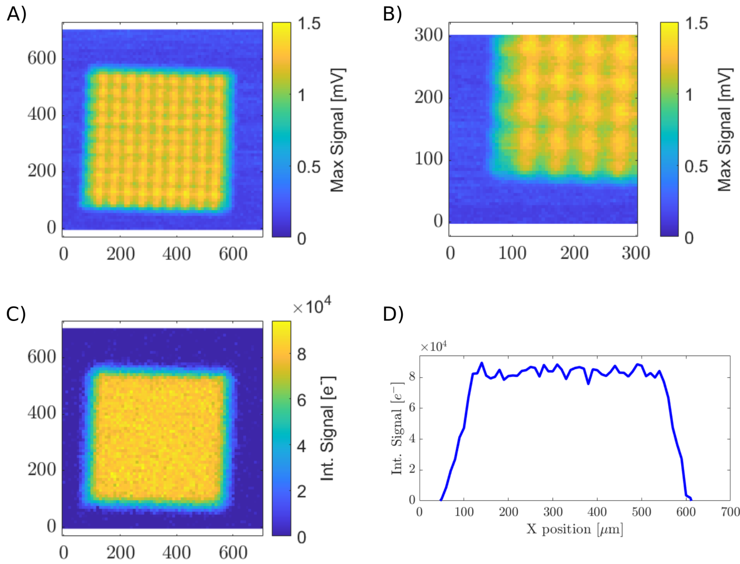


Figure 4.4.8: (A) Map of the maximum signal peak amplitude for a motor step of 10 μm. (B) Detail of the maximum signal peak amplitude map for a motor step of 5 μm. (C) Map of the charge collected for an integration time of 50 ns and a motor step of 10 μm. (D) Cross section of the signal integral map taken in a cut plane parallel to the x-axis. Pictures from [20] (CC BY 4.0).

ring around the pixel arrays can be clearly identified with the green and light blue areas [20]. Figure 4.4.8C shows the maps of the signal integral and thus the charge collected considering an integration time of 50 ns. A uniform charge collection can be observed within the matrix area with a decrease in the

signal at the matrix border due to the competitive charge collection of the frontside guard ring. Finally, a cross section of the signal integral map generated considering a cut plane parallel to the x-axis is displayed in Figure 4.4.8D [20]. Here, the competitive charge collection between pixels and guard ring can be noticed looking at the collected charge profile, which sharply decreases moving to the matrix border in the areas corresponding to the first and last pixel columns.

4.4.3 Passive pixel arrays with gain layer

As mentioned in Chapter 2, passive pixel arrays with integrated gain layer, designed to improve the timing resolution increasing the SNR of the sensor, have been included in a test chip contained in the wafers of the third ARCADIA production run. These matrices embed large pixels with squared or rectangular shape having 250×250 μm^2 and 250×100 μm^2 pixel areas, respectively. In order to achieve the desired timing resolution in the order of less than 20 ps, required for the detectors to be included in the ALICE 3 upgrade timing layers, the performed TCAD and Monte Carlo simulations predicted the need of a gain value ranging from 10 to 30 and of a detector active thickness lower than 50 μm [34]. As mentioned in Section 4.2.3, due to the different energy employed in the ion implantation performed to realize the embedded gain layer, low gain values ranging from 2 to 4 have been estimated from the optical characterization of the fabricated pixel arrays. The

gain was estimated by computing the ratio between the total amount of charges collected from a test structure with integrated gain layer and the ones collected from a reference passive pixel array without gain layer under the same illumination conditions.

The designed test structures represent essentially possible implementations of monolithic LGADs, where the frontend electronics and the LGADs can be embedded on the same substrate with the collection electrodes AC-coupled to the frontend preamplifiers that can be placed at the pixel edges [34]. AC-coupling will be needed to enable the application of the high bias voltage at the sensor collection electrode, which guarantees the presence of a high electric field in the gain layer region needed to trigger the charge multiplication through impact ionization and the full depletion of the gain layer [34]. In comparison to a standard LGAD structure, the layout of the designed test structures enables the control of the gain value and of the drift field intensity acting on the positive and negative bias voltages applied to the frontside and backside electrodes, respectively [34].

Figures 4.4.9 and 4.4.10 show the effect of the variation of these voltages on the measured signals and on the corresponding total amount of collected charges derived from the signal integrals of a pixel array with squared 250 μm pixels, called PM 250 G1, having an active thickness of 48 μm. Due to the presence of the p^+ substrate, which represents a 250

μm thick inactive region at the chip backside, the IR laser with 1060 nm wavelength was the only one suitable to reach the active volume illuminating the sensor from the backside with a focused laser spot. However, due to its absorption length in the order of 1 mm inside silicon, the measurements were unavoidably affected from the back reflection of the IR light due to the presence of metal lines and contacts at the frontside. Therefore, these measurements gave only an indication of the possible gain value due to the uncertainty in the amount of collected charges related to the back reflection phenomena. A precise estimate of the gain value can be provided only through the characterization of the structures in a test beam, where the amount of generated charges can be estimated more accurately knowing the energy released from the impinging charged particles. Looking at the left plots in the two Figures, it is possible to observe that the measured signals were affected from noise generated by the EM interference coming from the laser driver and the non optimal shielding of our setup. The plots on the right hand side of the Figures, showing the corresponding integrated charge, prove that acting on the voltage applied to the frontside collection electrode has a greater impact on the resulting charge multiplication rather than changing the applied backside bias voltage. This effect was also noticed in the results of the preliminary TCAD simulations and is related to the major impact of the frontside voltage on the electric field strength in the gain layer region

[34]. A maximum gain value around 4 was estimated from the ratio between the charges collected from the considered PM 250 and a reference structure without gain, displayed with a red dashed line in the charge collection plots. Finally, the tests showed that both the frontside and the backside voltages affect similarly the charge collection speed acting on the strength of the drift field inside the sensor active volume.

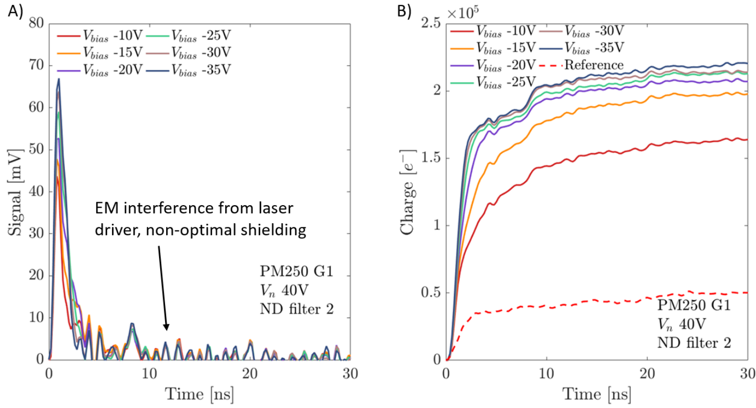


Figure 4.4.9: (A) Measured signals on a PM 250 G1 as a function of the applied V_{bias}. (B) Corresponding signal integrals as a function of the applied V_{bias}. Pictures from [104].

To evaluate the charge collection dynamics and the charge multiplication at the collection electrode sides for the pixel arrays with different layouts of the terminations at the pixel borders, scans of the matrix area have been performed changing the position of the focused IR laser spot. A motor step size

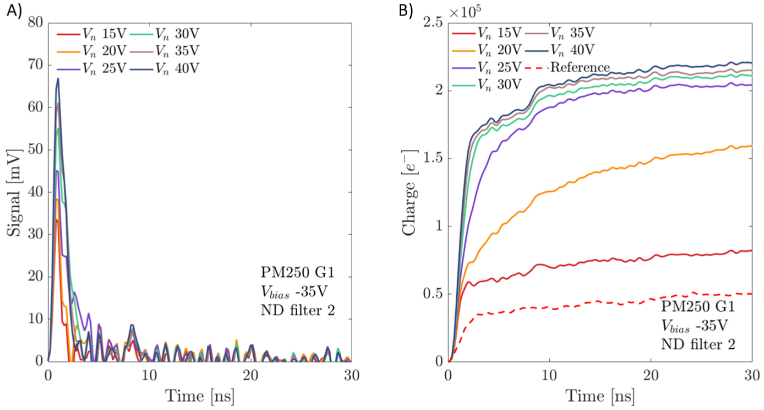


Figure 4.4.10: (A) Measured signals on a PM 250 G1 as a function of the applied V_n. (B) Corresponding signal integrals as a function of the applied V_n. Pictures from [104].

of 5 μm has been employed in the acquisitions, which covered a total area of 350×350 μm^2. The pixel arrays with different termination layouts are composed by rectangular pixels having a pixel area of 250×100 μm^2 and are characterized by the presence of a gap between the deep pwell and the gain layer implants in the so-called layout A2 or from the absence of this gap in the layout A1. As explained in Section 4.1, the former enables a faster charge collection at the pixel borders, while the latter provides a higher charge multiplication in the interpad region. Figures 4.4.11A and 4.4.11B show the maps of the maximum signal amplitude for the two measured pixel arrays having layouts A1 and A2. Due to the same issue mentioned above, related to the back reflection of the IR laser at

the frontside metal and contacts, which are characterized from different refractive indexes, both signal maps show an unexpected significant variation in the measured signal amplitude within the collection electrode regions.

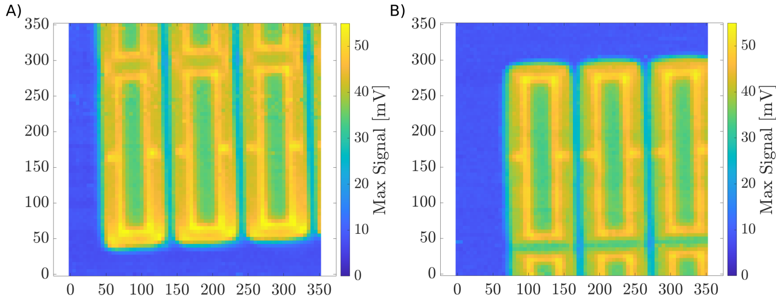


Figure 4.4.11: (A) Map of the maximum signal peak amplitude for the PM 250 with layout A1. (B) Map of the maximum signal peak amplitude for the PM 250 with layout A2. Pictures from [104].

Namely, considering a horizontal cut plane parallel to the x-axis, it is possible to extract a cross section of the signal maps, which represents the variation of the maximum signal amplitude as a function of the x-coordinate for the two different layouts. Looking at this plot, reported in Figure 4.4.12, it is easy to identify the positions of the frontside contacts and frontside guard rings with the dips in the profile present at the pad centers and in the interpad regions. Similar maximum signal amplitude can be observed comparing the two profiles, with only small differences in the height of the profile

shoulders corresponding to the pad borders, where, as expected, the layout A1 provides slightly higher signal amplitudes.

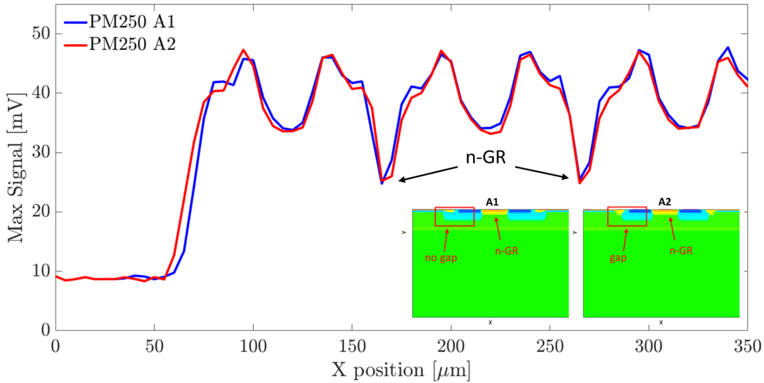


Figure 4.4.12: Cross sections of the maximum signal maps taken along a horizontal cutplane parallel to the x-axis. Picture from [104].

The difference becomes more evident looking at the derived maps showing the total amount of collected charges computed from the acquired signals within an integration time window of 30 ns for the two considered pixel arrays. These maps are displayed in Figures 4.4.13A and 4.4.13B for the PM with layout A1 and A2, respectively. As expected, a higher amount of charges is collected in the interpad regions by the pixel arrays having layout A1 i.e. without gap regions at the pad borders.

This effect can be clearly noticed in Figure 4.4.14A and even better in Figure 4.4.14B, that show the comparison of the sig-

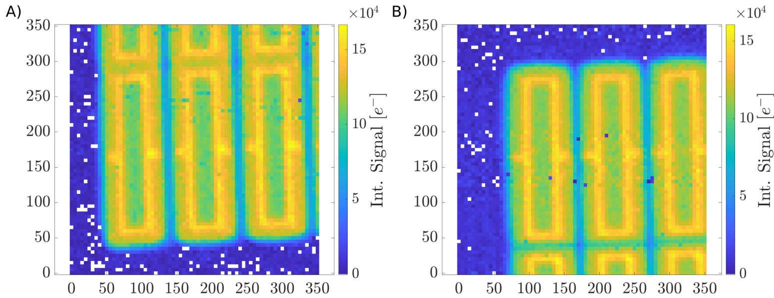


Figure 4.4.13: (A) Charge collection map for the PM 250 with layout A1. (B) Charge collection map for the PM 250 with layout A2. Pictures from [104].

nal integral profiles extracted from two different cross sections of the two signal integral maps. In the first case, the profiles reported in the plot represent the variation of the signal integral along the same horizontal cut plane considered above. Instead, the profiles reported in the second plot show the variation in the charge collection along a vertical cut plane parallel to the y-axis lying at the center of the collection electrodes. In this second case, since there are not n-guard rings running horizontally in the interpad regions, the charge collection at the pad borders highlights the differences in the performance in terms of charge multiplication for the different termination layouts and provides an experimental confirmation of the different behaviors expected from TCAD simulation.

Finally, a comparison of the timing response of the two pixel arrays is shown in Figure 4.4.15, where the time needed to

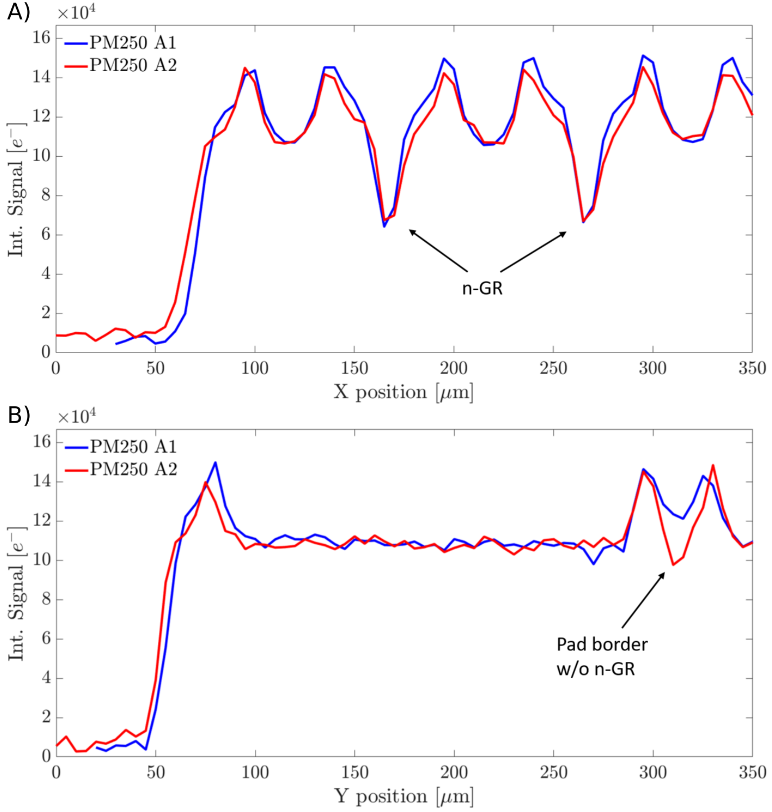


Figure 4.4.14: (A) Cross sections of the signal integral maps taken along a horizontal cutplane parallel to the x-axis. (B) Cross sections of the signal integral maps taken along a vertical cutplane parallel to the y-axis. Pictures from [104].

reach the 50% of the signal rising edge ($t_{rise_{50}}$) is reported as a function of the laser spot position. In these maps the faster and more uniform response at the pixel borders provided by

the array with layout A2 is evident. Namely, the extracted $t_{rise_{50}}$ results more than doubled at the interpad regions characterized by the presence of the guard ring for the pixels with termination layout A1. On the contrary, a much smaller increase in $t_{rise_{50}}$ can be observed in the same regions for the pixel array with layout A2.

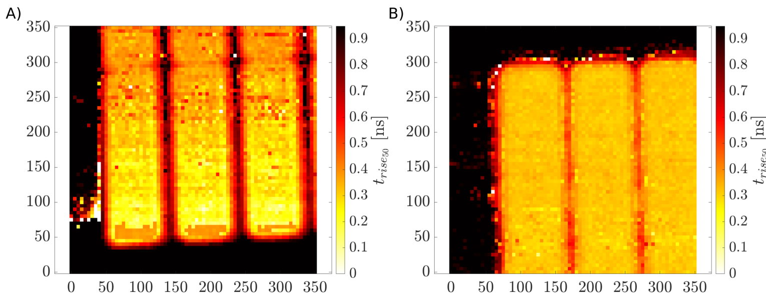


Figure 4.4.15: (A) $t_{rise_{50}}$ map for the PM 250 with layout A1. (B) $t_{rise_{50}}$ map for the PM 250 with layout A2. Pictures from [104].

The plot in Figure 4.4.16, showing the comparison of the profiles obtained considering the usual horizontal cross section in the $t_{rise_{50}}$ maps for the two different pixel arrays, proves that the layout without gap region is able to guarantee the best timing performance in terms of uniformity in the measured timing response. This lead to the conclusions that the proper layout design should be selected on the basis of the application needs: the layout A1 should be preferred when a higher charge multiplication is needed at the pixel borders and, in-

stead, layout A2 is the proper choice when a more uniform and faster timing response all over the matrix is needed.

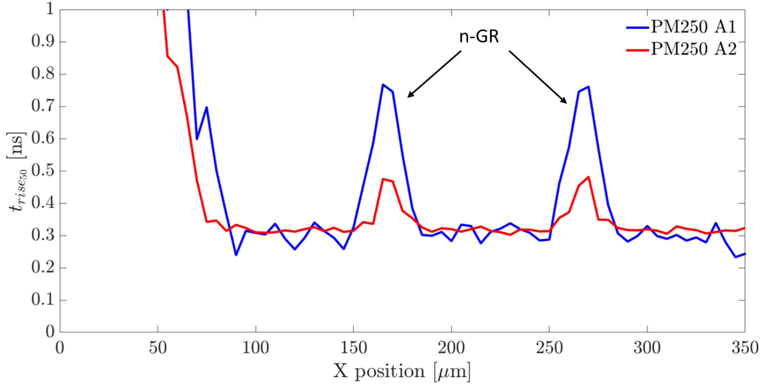


Figure 4.4.16: Cross sections of the $\mathrm{t_{rise_{50}}}$ maps taken along a horizontal cutplane parallel to the x-axis. Picture from [104].

The knowledge on the behavior of the designed monolithic LGAD acquired through these measurements will be exploited to select the termination layouts and the dose splittings for the new gain layer profile to be included in the test structures of a new silicon run, entirely dedicated to timing applications, that will be fabricated in 2024.

Chapter 5

COBRA sensor

The response of the COBRA sensor, a monolithic active sensor chip designed for dosimetry in High Dose Rate brachytherapy applications, has been tested employing both EM-radiations and charged particles [109]. A pad diode covering a total area of 460×340 μm^2 constitutes the sensing element of the chip, which was designed to work in full depletion condition. The frontend electronics is realized at the periphery of the chip active region using the 110 nm CMOS technology developed in the ARCADIA project and provides two possible operating modes of the embedded dual gain amplifier called High-Gain (HG) and Low-Gain mode (LG), respectively. The integrated electronics consists of a preamplifier followed by a buffer able to provide two nominal gain values equal to 1 in LG mode or 10 in HG mode. The two operating modes correspond to different signal time constants at the chip output with a reset time in the order of 4 μs and several hundreds of μs in HG and LG mode, respectively. The logic values of three configuration bits can be modified to switch between the two preamplifier and buffer operating modes. The default configuration sets the sensor electronics in HG mode and can be overwritten

connecting the pads of the configuration bits to V_{DD}, i.e. the nominal voltage equal to 3.3 V representing the logic high level or to the ground reference (GND) corresponding to the logic low level. A custom PCB was designed to properly apply the required analog and digital voltage bias to the dedicated chip electrodes that are shown in Figure 5.0.1. The chosen PCB layout gave the possibility to switch between the two chip operating modes simply changing the positions of three jumpers.

The tested chips were extracted from wafers produced in the first and second ARCADIA silicon run and characterized by nominal active thicknesses equal to 48 and 100 μm using epitaxial and high resistivity substrates, respectively. The negative voltage bias was applied to the p-type backside electrode in order to fully deplete the sensor substrate. The value of the bias voltage was selected using as a reference the operating voltage range measured on the passive pad diodes extracted from the same wafers of the tested COBRA chips and biased in the same conditions. A micrograph of the COBRA chip showing the frontside pads dedicated to the analog and digital bias voltages is reported in Figure 5.0.1. The picture shows the overall chip dimensions in comparison to the pad diode active area and of the compact design of the sensor, which made it suitable to be mounted on the tip of a prostate catheter.

The IR laser mounted in the optical setup and an IR LED were used to evaluate the response of the chip to an optical

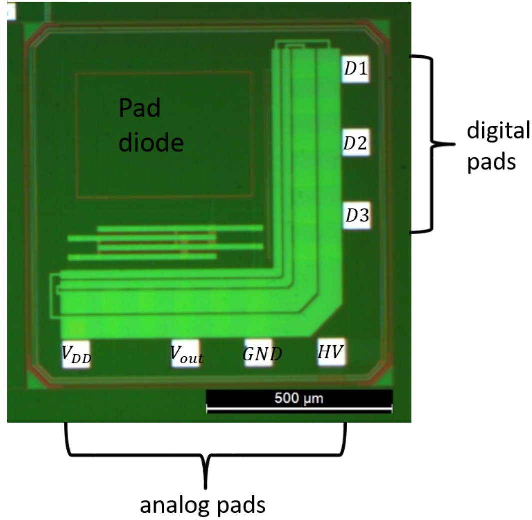


Figure 5.0.1: COBRA chip micrograph.

stimulus acquiring both the waveforms and the charge spectrum of the sensor at different light intensities. Acquisitions were performed with the sensors illuminated from the frontside or the backside surface. The waveforms obtained setting the frontend amplifier in HG and LG mode are reported in Figure 5.0.2A and Figure 5.0.2B, respectively. The signals were acquired with the Tektronix MDO3102 digital oscilloscope exploiting its full bandwidth equal to 1 GHz. The chip was reverse biased applying to the backside electrode a negative voltage equal to -34 V, higher than the full depletion voltage according to the preliminary measurements performed on the passive pad diodes. In order to avoid the saturation

of the frontend electronics and to limit possible space charge effects related to an excessive amount of optically generated charges, two different neutral density filters with optical densities equal to 4 and 2 were used to limit the optical power of the incident IR laser in the acquisitions in HG and LG mode, respectively.

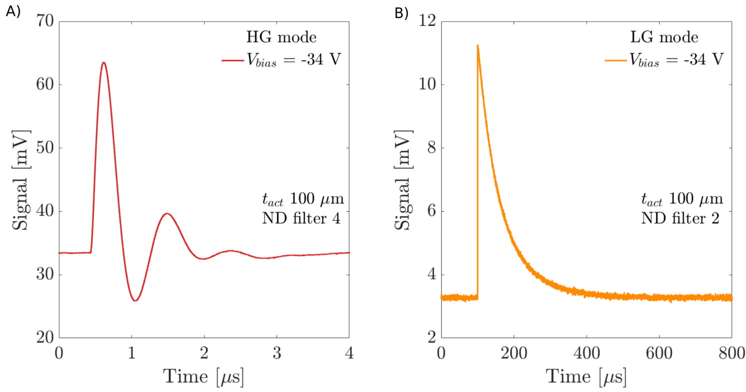


Figure 5.0.2: (A) HG mode signal measured on a COBRA chip with 100 μm substrate active thickness. (B) LG mode signal measured on a COBRA chip with 100 μm substrate active thickness.

The measured signals complied with the behavior expected from the simulations performed by the electronics designers. The signals acquired in HG mode showed a main signal peak with a rise time in the order of 200 ns followed by the expected undershoot and a damped oscillation, while the sensor response in LG mode was characterized by a fast rise time

around 10 ns and a recovery time in the order of hundreds of microseconds.

A CAEN 5780 MCA (Multichannel Analyzer) was employed to acquire the charge spectrum provided by the COBRA chips in the different test conditions. The MCA has a 14 bit resolution and adjustable input dynamic range, which was set equal to 0.6 V or 1.4 V according to the needs of the performed acquisition. An example of the acquired signal amplitude spectra obtained changing the current, and thus, the optical intensity provided by the IR LED, which was used to illuminate the chip on the frontside surface, is reported in Figure 5.0.3. In these acquisitions the HG mode of the sensor amplifier was selected and the input dynamic range of the MCA was set equal to 1.4 V. The plot showed that the sensor was able to provide a nearly linear response, with the mean values extracted from the gaussian fit of the acquired peaks that increased along with the increasing LED light intensity. The charge resolution of the detector estimated through the FWHM of the gaussian peaks improved for increasing light intensities. Namely, the ratio between the FWHM of the gaussian fits and the corresponding mean values showed a decrease from an initial value around 16% to approximately 11% for the increasing optical powers of the IR LED reported in the plot.

An X-ray tube with tungsten anode was used to irradiated the COBRA chip with 100 μm active thickness in order to test its performance in the detection of X-rays with energies

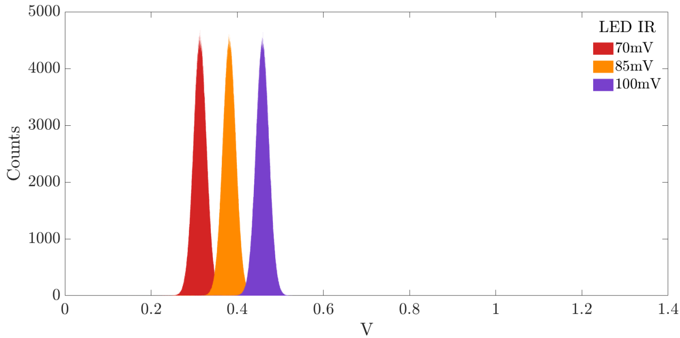


Figure 5.0.3: IR diode signal amplitude spectrum for increasing light intensity acquired with a COBRA chip having t_{act} equal to 100 μm.

up to 200 keV and, at the same time, to perform a reliable estimate of the amplifier gain exploiting the characteristic K_α and K_β emission lines of the tungsten anode. The CAEN Multichannel Analyzer was used to acquire the X-ray energy spectrum measured with the sensor configured in HG mode. Figure 5.0.4 shows the measured energy spectrum for the X-ray tube with a copper filter mounted in front of the tungsten anode for an applied anode voltage of 195 kV and an anode current of 1 mA. A total irradiation time of 2 minutes was considered in order to obtain a number of recorded events able to provide a good statistics. To better identify the characteristic K_α and K_β lines of W included in the energy spectrum, the background related to the Bremsstrahlung radiation was subtracted and the channels were binned together in groups

of 10. In this way, it was possible to improve the reliability of the gaussian fit performed on the data belonging to the K_α and K_β peaks.

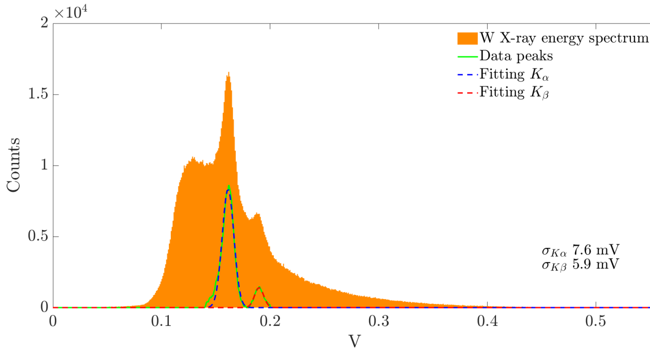


Figure 5.0.4: Energy spectrum of the X-ray tube with W anode for an applied anode voltage of 195 kV acquired with a COBRA chip having t_{act} equal to 100 μm.

The mean values extracted from the gaussian fits were in the order of 161 mV and 190 mV for the W K_α and K_β peaks with associated standard deviations σ_K in the order of 7.6 mV for the former and 5.9 mV for the latter. Using as a reference the tabulated mean energy values of the tungsten K-lines, in the order of 58.5 keV for the K_α line and around 67 keV for the K_β line, it was possible to estimate the corresponding number of electrons generated on average within the sensor active volume. Combining this information with the voltage values obtained from the gaussian fit of the two emission lines

identified in the acquired spectrum, it was possible to obtain an estimate of the sensor gain that was equal to 63 mV/fC with an associated uncertainty of 2 mV/fC.
The value of the feedback capacitance of the integrated preamplifier was computed as the inverse of the estimated gain value in HG mode, that was scaled by a factor 10 representing the nominal value of the buffer gain in this mode. As a consequence, the estimated amplifier feedback capacitance was equal to 159 $\pm$ 4 fF.

Chapter 6

TJ-Monopix2 chip

Calibration of the injection capacitance

This chapter describes a calibration activity performed on the depleted MAPS TJ-Monopix2. The knowledge of the injection capacitance value was needed to perform the calibration of the injection circuit, which is used to estimate the chip noise level and get comparable results between different detector technologies.

The TJ-Monopix2 chip represents an advanced fully depleted monolithic chip realized in the 180 nm TowerJazz CMOS technology, having a total area of 2×2 cm^2. The chip integrates an array composed of 512×512 pixels with a pitch of 33.04 μm [23], which has been subdivided in four vertical sectors characterized by different designs of the frontend electronics. The two sectors having frontend design called "normal" and "cascode normal" are both composed of 224 pixel columns, where the pixels are DC-coupled to the frontend electronics. The cascode frontends are characterized by an additional transistor in the preamplifier circuit that guarantees a higher gain value. Instead, the remaining front ends, called "High Voltage

(HV)" and "cascode HV" are used in 32 pixel columns, where the pixel collection electrodes are AC-coupled to the frontend preamplifiers [62]. The embedded electronics includes also a 3-bit tuning DAC that can be used to locally adjust the pixel threshold reducing the threshold dispersion within the matrix [22], [62]. A 7-bit gray counter, which works at a frequency of 40 MHz, is used to provide the BCID timestamp. The Time-over-Threshold (ToT) value is computed as the difference between the BCID timestamps associated to the Trailing Edge and to the Leading Edge [62]. As a consequence, the pixel and the cluster ToT can provide an information with a 7-bit resolution on the amount of charges collected by a single pixel and a cluster of pixels, respectively. These values are expressed as multiple of the BCID clock time period equal to 25 ns.

The tested chips have been extracted from wafers with two substrate types: a p-type epitaxial layer grown on top of a p^+ substrate or a thick Czochralski high resistivity p-type substrate both characterized by a resistivity larger than $1\,k\Omega \cdot cm$ [23]. To improve the charge collection at the pixel periphery, the pixels included in the TJ-Monopix2 chips have the two modified layouts shown in Figure 6.0.1 already tested in the TJ-Monopix1 chips, which reshape the electric field at the pixel borders. The devices extracted from the epitaxial wafers have pixels with gaps in the frontside low doped n-type implant at the pixel borders and, instead, an additional deep

pwell implant is realized below the deep pwell at the periphery of the pixels included in the chips with Czochralski substrate. Both design solutions, already tested in the TJ-Monopix1 chips, proved to be able to speed up the charge collection in the regions at the pixel borders, improving at the same time the charge collection efficiency after irradiation [23].

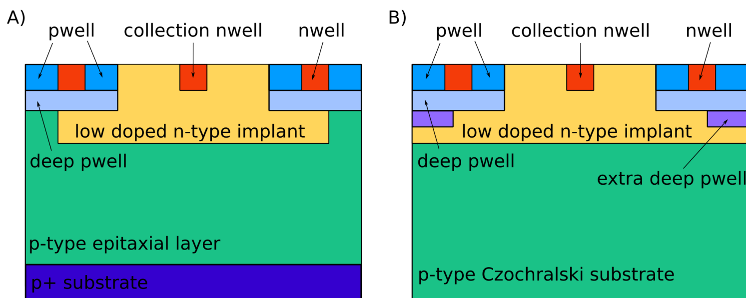


Figure 6.0.1: (A) Schematic cross-section of the TJ-Monopix 2 chip having p-type epitaxial layer and gaps in the frontside low doped n-type implant at the pixel borders. (B) Schematic cross-section of the TJ-Monopix 2 chip having p-type Czochralski substrate and extra deep pwell at the pixel borders.

The results presented in this Chapter will focus on the calibration of the injection capacitance performed on the pixels of the chip Sectors having DC-coupled frontends for two chips with different substrate types.

The characteristic $K_{\alpha,\beta}$ and $L_{\alpha,\beta}$ lines present in the X-ray

spectrum obtained by X-ray fluorescence induced on a group of targets made of different materials have been exploited to estimate the value of the injection capacitance C_{inj} included in the charge injection circuit of the TJ-Monopix2 chip. X-ray fluorescence represents the emission of secondary X-rays having specific energy levels, which change inducing this physical effect on targets made of different elements. A Hamamatsu microfocus X-ray tube with tungsten anode installed on the floor of a Phoenix X-ray bench|mate 90 cabinet has been employed to generate the primary X-rays, which hitting the target material resulted in the emission of the characteristic secondary X-rays exploited for the calibration. Targets made of seven different materials (Al, Ti, 90MnCrV8 steel, Cu, Nb, Mo and Ta) were available for the X-rays fluorescence setup. The targets were cylindrical plates made of pure materials with 1" diameter, that fit with the dimension of the hole in the target holder placed in an adjustable position above the X-ray microtube. Figure 6.0.2 shows a picture of the X-ray fluorescence setup, where it is possible to identify the target holder placed above the X-ray tube and the DUT mounted on the cabinet side wall.

According to the physical principles at the basis of X-ray fluorescence, the probability of emission of a secondary X-ray decreases for materials having lower Z-values due to the increasing contribution of the Auger effect, which leads to the emission of a secondary electron. Moreover, the prob-

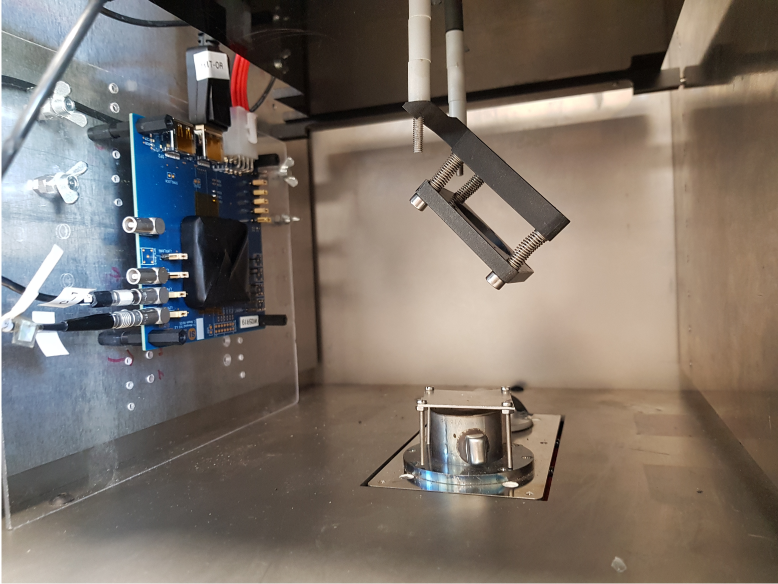


Figure 6.0.2: Picture of the X-ray setup employed for the calibration of the injection capacitance.

ability of a photon emission from an excited K-shell electron is higher than the corresponding emission probability of an X-ray photon belonging to the characteristic energy lines associated to the electrons in the material outer shells [110]. As a consequence, the acquired spectra showed only the characteristic K-lines for the targets made of low Z-elements and both the K- and L-lines for the target realized with high Z-elements. As expected, the acquired X-ray energy spectra included the unavoidable background component related to

Bremsstrahlung and the peak related to the tungsten anode characteristic emission lines. The cabinet itself represents a source of additional background components, which sum into the total background radiation, related to the scattering of the primary and secondary X-rays and to the emission of secondary X-rays from the cabinet materials.
The presence of the background radiation in the X-ray setup set a lower limit to the energy of the emission lines that can be exploited in the calibration procedure, since the K-lines of the available low Z-targets, i.e. Al and Ti, were masked by the background in the acquired spectra. Moreover, a saturation in the Time over Threshold (ToT) value, provided in output from the chip, was observed already for the X-rays energies associated to the characteristic K-lines of Mo and Nb in the order of 16.5 and 17.5 keV, respectively. As a consequence, only the K_α lines of Cu, of the iron contained in the steel target and the L-lines of Ta had an energy within the exploitable range and, therefore, could be employed in the capacitance estimate and were reported in Figure 6.0.4b. An additional point, that was exploited in the calibration, was provided from a ^{55}Fe source with an activity of 6 MBq, that emitted X-rays with the characteristic peak of Mn at an energy of 5.89 keV.
The calibration procedure can be summarized in the following steps, that were performed to estimate the value of the injection capacitance:

1. the so-called "global threshold tuning" and "local

threshold tuning" routines were executed in a sequential way on the pixels of the chosen number of columns within the considered matrix Sector. This routines provided the optimal values for the global and the local registers, which guarantee the possibility to reduce the threshold dispersion around the chosen threshold level and to minimize the pixel noise level.

2. a "threshold scan" was performed on the tuned pixel columns in order to get the S-curve and the related histogram of the pixel ToT response as a function of the applied injection voltage steps ΔVCAL for the pixels in the considered columns. During a "threshold scan", the ΔVCAL value applied to the injection circuit of the enabled pixels was varied within the chosen range of values. In this script a dedicated variable was used to define the number of repeated injections, that were performed on the pixels of the selected columns for each ΔVCAL value in the considered range.

3. the injection circuitry was able to provide a maximum charge limited to around 1.8 ke^-, which was even smaller than the lowest point available for the calibration corresponding to the characteristic peak in the ^{55}Fe charge spectrum. As a consequence, a fitting function was applied to the aforementioned histogram considering the weighted mean of the pixel ToT values as a function of

the applied injection voltage steps. The fitting function was then employed to get an estimate of the amplitude of the injection voltage difference needed to get a ToT value higher than the maximum one achievable with the injection circuit capability.

4. the K- and L-lines of the X-ray fluorescence spectra acquired in terms of cluster ToT response were fitted with a gaussian function. The mean value of the cluster ToT response obtained from the gaussian fit was linked to the mean value of the corresponding characteristic X-ray line energy expressed in keV. The simple relation existing between the energy of a photon and the resulting number of electrons generated on average in silicon was exploited to get the relation between cluster ToT values and number of collected charges.

5. the information on the number of collected charges for a specific ToT value and on the injection voltage difference needed to get the same ToT output were combined and the injection capacitance value was estimated.

Additional information on the script employed for the threshold tuning, the threshold scan and the following data analysis, that were developed by the members of the SiLab group, can be found in [111].

According to the procedures explained above, once executed the 'global' and 'local' threshold tuning routines, a 'threshold

scan' was performed on the enabled pixel columns to get information on the threshold dispersion and on the noise distribution for the considered pixels. The plot showing the histogram of the pixel ToT response as a function of the applied injection voltage steps (ΔVCAL) and the corresponding S-curve, showing the pixel occupancy as a function of ΔVCAL applying 100 injections, are reported in Figure 6.0.3 for the pixels in the first 32 columns of the Sector with normal front-end design for the tested sensor having Czochralski substrate.

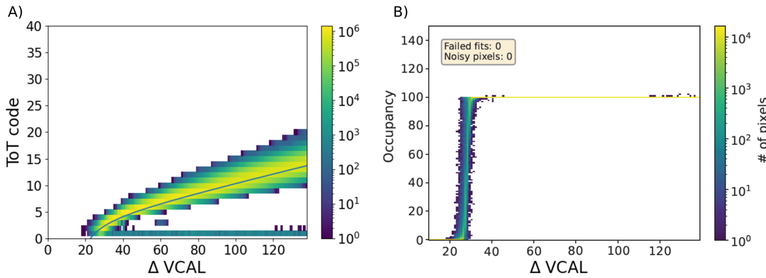


Figure 6.0.3: (A) Histogram of the ToT response as a function of the applied ΔVCAL. (B) Corresponding S-curve showing the pixel occupancy as a function of the applied ΔVCAL.

The histogram in Figure 6.0.3A shows clearly that the maximum amount of charges that can be generated exploiting the whole linear range of the charge injection circuit, in the range between 20 and 140 ΔVCAL steps, corresponds to a low ToT code around 20. Therefore, a fitting function able to represent the relation between ToT code and ΔVCAL for higher

ToT values was implemented. This enabled to extract the ΔVCAL values corresponding to the ToT codes obtained from the X-ray fluorescence spectra. At the same time, the S-curve displayed in Figure 6.0.3B, obtained after running the tuning algorithms, shows a low threshold dispersion for the selected pixels with the pixel occupancy that sharply increases around the selected threshold level.

Using the same register configuration employed in the 'threshold scan', the X-ray fluorescence spectra of the targets made of different material were collected in the X-ray setup. According to [110], the current and the voltage applied to the anode of the X-ray tube were changed on the basis of the target material trying to improve the detectability of the characteristic line peaks for the following gaussian fitting algorithm. An example of an acquired X-ray spectrum for the tuned pixel columns with normal FE design of the Czochralski substrate sensor is shown in Figure 6.0.4A, where it is possible to identify the characteristic peak associated to the K_α line generated by the induced X-ray fluorescence of the copper target. In this acquisition, an anode voltage of 50 kV and an anode current of 60 μA were applied to the X-ray tube for a total irradiation time of 350 s. The obtained ToT values representing the mean values extracted from the gaussian fit of the characteristic fluorescence peaks for the available target materials and the ^{55}Fe source have been reported in Figure 6.0.4B as a function of the corresponding characteristic emis-

sion line energies.

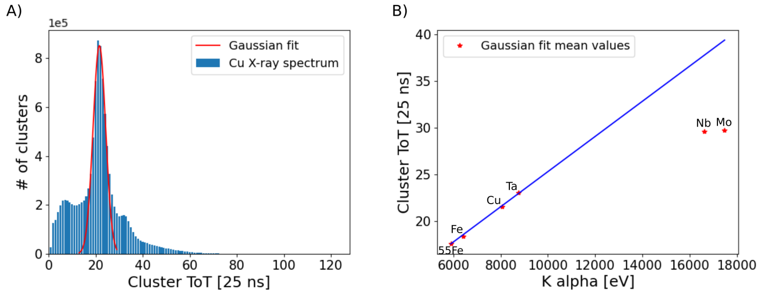


Figure 6.0.4: (A) Acquired fluorescence X-ray spectrum for the Cu target. (B) ToT mean values extracted from the gaussian fit of the characteristic fluorescence lines as a function of the corresponding line energies.

As can be clearly noticed in Figure 6.0.4B, the data points corresponding to the ToT values obtained from the gaussian fit of the K_α lines of Nb and Mo lie outside the linear region of the ToT response and therefore cannot be employed in the estimation of the injection capacitance.
The relationship between ToT code and ΔVCAL obtained by the fit of the histogram shown in Figure 6.0.3A was exploited to convert the ToT mean values extracted with the gaussian fit in the corresponding ΔVCAL values. The value of a single ΔVCAL step, equal to 7.03 mV according to [62], was then used to express the obtained ΔVCAL values in volt. In an analogous way, the considered characteristic emission line energies were converted in the mean number of electrons and,

then, in the corresponding amount of charge expressed in coulomb, that are generated within silicon from a photon with those specific energy levels. Finally, exploiting the information on the voltage and on the charge values associated to the emission lines of the different targets, the mean value of the injection capacitance of the considered pixel columns was estimated employing two different approaches, which provided slightly different results in agreement with respect to the error margins. A first estimate of the injection capacitance was obtained using the capacitance definition itself, i.e. the ratio between charge and electric potential. The injection capacitance mean value and the associated standard deviation were estimated from the C_{inj} values obtained for the different target materials and have been reported in Table 6.1 for the normal and cascode FE Sectors of the two tested chips.

Table 6.1: Estimated C_{inj} mean value and standard deviation for the pixels of the normal and cascode FE Sectors of the TJ-Monopix2 chips

Substrate	Normal FE [aF]	Cascode FE [aF]
Epitaxial	182 ± 7	201 ± 3
Czrochralski	215 ± 9	212 ± 7

An alternative estimate of C_{inj} was obtained considering the

angular coefficient of the linear fit passing through the data points considered above, representing the relation between the deposed charge and the injection voltage estimated for the considered characteristic emission lines of the targets. In this second case, an additional data point was considered to take into account the threshold level, expressed in ΔVCAL steps, that was chosen in the tuning phase. This additional point represents the positive offset in the injection voltage value associated to a ToT code equal to 0, that can be observed in Figure 6.0.3A. The C_{inj} values estimated through the angular coefficient of the linear fit and the associated uncertainty are reported in Table 6.2 for the considered columns of the normal and cascode FE Sectors of the two chips with epitaxial and Czochralski substrates, respectively.

Table 6.2: Estimated C_{inj} from the linear fit and associated uncertainty for the pixels of the normal and cascode FE Sectors of the TJ-Monopix2 chips

Substrate	Normal FE [aF]	Cascode FE [aF]
Epitaxial	200 ± 12	204 ± 9
Czrochralski	240 ± 17	238 ± 16

Looking at the C_{inj} values reported in the Tables, it is possible to notice the slightly higher capacitance values estimated

through the fitting function, which are closer to the one expected from the design equal to 230 aF [62]. This difference is related to the smaller angular coefficient obtained considering in the linear fit the additional data point representing the positive offset in the ΔVCAL values corresponding to a ToT output equal to 0.

Chapter 7

Conclusions

Several active and passive sensors together with a large-area monolithic active pixel sensor, representing the main derivable of the collaboration, have been designed and then fabricated using a commercial 110 nm CMOS production process with only a few needed add-ons in three different production runs within the INFN ARCADIA project. The produced wafers were characterized by three different nominal substrate thicknesses equal to 48, 100 and 200 μm in order to meet the different requirements in terms of material budget, charge collection speed and sensor active thickness set by the different application fields of the designed sensors.
Preliminary TCAD simulations were employed to design the sensing elements of the active and passive pixel and strip arrays, choosing only the most promising pixel or strip layouts and dimensions to be included in the produced wafers. TCAD simulations were also exploited to design the test structures and the process control structures that were used to characterize the developed sensor technology. These structures were also needed to verify the behavior of the frontside and backside terminations included to guarantee the application of the

voltage bias needed to deplete the sensor without breakdown or punch through issues for substrate thicknesses up to several hundreds of micrometers.

The characteristics of the backside interface in terms of surface generation velocity and concentration of positive charges trapped in the passivation layer were extracted from the measurements performed on gated diodes and MOS capacitors. Instead, frontside and backside diodes with different termination structure layouts were tested to identify the optimal guard ring number and geometry able to prevent the breakdown of the junction, where the voltage bias is applied, and at the same time avoid issues related to the early onset of punch through.

In parallel, the produced passive arrays with different strip and pixel layouts were characterized both electrically and optically using a pulsed IR laser. In particular, the IV and CV characteristics of the passive pixel arrays were measured to quantify the operating voltage range, the dark current and the capacitance value characterizing the different layouts and pitches. The extracted punch through and full depletion voltages, pixel dark current and capacitance values were compared with the ones predicted from TCAD simulations. The comparison showed an excellent agreement between the experimental data and the simulation results, which proved the reliability of the physical models employed in the design simulations. The estimated capacitance for the 25 μm pixels

included in the ARCADIA Main Demonstrator (MD) chip in the order of 4.5 fF is in line with the values reported in literature for the pixels included in the ALPIDE and TJ-Monopix2 chips, which represent two state-of-the-art MAPS with pixel sizes comparable with the MD pixels.

The radiation hardness of the different pixel layouts was evaluated through dedicated irradiation studies, where the sensors have been irradiated with X-rays following a precise sequence of dose steps up to a TID of 10 Mrad. The variation in the measured IV and CV curves for increasing X-ray doses was compared with the one expected from TCAD simulations, where the 'new Perugia' radiation damage model was implemented. The experimental data confirmed that the sensor technology was able to withstand the considered TID and, moreover, the measured increase in the pixel capacitance value after irradiation proved to be lower than the one predicted from TCAD simulations. Instead, a detailed study of the NIEL effects on the fabricated MD chips is still missing and will be required to assess the maximum fluence that the technology can withstand guaranteeing the proper chip functionality. This information will be fundamental to determine the potential cases in which the designed chip could be employed in future HEP experiments.

At the same time, the charge collection dynamics of the fabricated pixel arrays was assessed exploiting an external optical stimulus generated with fast sub-nanosecond pulsed laser di-

odes having red or IR wavelengths. Optical scans of the pixel arrays were also performed changing the position of the focused laser spot within the matrix active area and the acquired waveforms were used to disentangle the signal contributions related to the collection of the charges generated in different pixel regions. The obtained results showed charge collection times in the order of few ns or tens of ns depending on the considered pixel size and substrate thickness, which are in line with the goal of the project.

Also the test structures with integrated gain layer fabricated within the third ARCADIA production run were designed by means of TCAD simulations and characterized from the electrical and dynamic point of view. The data proved the feasibility of integrating a gain layer in the monolithic sensor technology, paving the path to a new wafer production, where the acquired knowledge has been exploited to fine tune the gain layer doping concentration, in order to achieve the timing resolution required by the timing layers of the ALICE 3 Upgrade. The signal dynamics of the sensors fabricated in the future production will be evaluated exploiting optical setups with fast pulsed laser sources and also particle beams in order to validate the TCAD simulation models and check the actual timing resolution that can be achieved with this novel technology.

The behavior of the COBRA chip, which represents a single-channel monolithic active sensor designed for brachytherapy,

has been evaluated exploiting different radiation and optical sources. The characteristic emission lines of an X-ray tube with tungsten anode were used to estimate the gain provided by the sensor in High Gain mode, which was in the order of $63\pm2\,\mathrm{mV/fC}$, and the value of the associated feedback capacitance of the dual gain preamplifier integrated within the chip, which was equal to $159\pm4\,\mathrm{fF}$.

Finally, the calibration of the injection capacitance of the TJ-Monopix2 chip, a full scale monolithic active pixel sensor realized in the TowerJazz 180 nm CMOS technology, was performed exploiting X-ray fluorescence techniques. The estimated capacitance values proved to be in agreement with the one expected from the chip design and provided a calibration of the charge injection mechanism, which will be exploited to obtain an accurate estimate of the chip noise level.

A detailed characterization of the noise level of the ARCADIA MD chip is still missing and represents one of the open tasks that should be completed in the near future in order to provide a complete picture of the chip performance.

Perspectives and future work

The realized Main Demonstrator chip showed the great potential of the developed sensor technology and represents a starting point for the future development of novel large area prototypes based on the modified 110 nm CMOS production process of LFoundry.

Reducing the pixel pitch in order to improve the space resolution as well as decreasing the chip power consumption w.r.t. the ones guaranteed by the MD chip can represent interesting developments of this large area prototype for particle tracking applications in HEP experiments and space applications, respectively.
Moreover, the possibility to reach the full depletion of substrate thicknesses in the order of $300-500\,\mu$m makes this technology appealing also for X-ray imaging applications requiring the detection of X-rays with energy up to $\sim 15\,$keV.
Looking at the possible application of this technology in the medical field the COBRA and the MD chips can be attracting solutions for the fabrication of compact probes for dosimetry monitoring in HDR brachitherapy treatments and of medical scans for Proton Computed Tomography (PCT), respectively.
Finally, the development of the monolithic LGAD concept will be pursued by the ALICE 3 timing layers WG trying to improve the achievable timing resolution by tuning doping concentration of the integrated gain layer and decreasing the active substrate thickness down to $25 - 15\,\mu$m. If the devices of the new production will be able to guarantee a timing resolution in the order of few tens of ps, they will become attractive also to implement time-tagging hodoscopes for protontherapy applications. In this case, the sensors will be exploited to perform time-of-flight measurements on the emitted protons and, as a consequence, retrieve information on the particle energy and the related particle range.

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