Dual Sequence Controller with Delayed Signal Cancellation in the Rotating Reference Frame

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***Abstract*—Dual-sequence current controllers of voltage source converters (VSCs) feature two separate rotating reference frames (RRFs), commonly named dq frames, and rely on techniques that isolate the positive and negative sequences of three-phase measurements. One of these techniques is the delayed signal cancellation (DSC). It is performed in the stationary reference frame (SRF), also known as $\alpha\beta$ frame. The DSC combines old values of one axis with new values of the other axis of the SRF. The results are, then, transformed into the RRFs for use in the current controller. This filtering process introduces an extra layer of complexity for dual-sequence current controllers, which could otherwise operate solely in the RRFs. This paper introduces a frequency adaptive DSC method that operates directly in the RRF. Moreover, an averaging of two of the proposed DSC filters with contiguous integer delays is employed for reducing discretization errors caused by grid frequency excursions. A formal proof of the equivalence between the $\alpha\beta$ and dq DSC methods is presented. Furthermore, computer simulations of a case study support the interpretation of the results.**

***Index Terms*—power electronics, power systems, power conditioning, power system control, current control, signal processing algorithms**

I. Introduction

The traditional control in the rotating reference frame (RRF) (dq) of three-phase voltage source converters (VSCs) assumes that grid voltages are reasonably balanced. However, unbalances appear frequently in practical applications of grid-connected power electronic converters. When the grid voltage is not balanced, a second harmonic component appears in the instantaneous active power and hence dc-link voltage of the converter [1]. This degrades the performance and stability of the VSC. The performance of a VSC operating under unbalanced, reduced voltage, or fault conditions can be improved by dual-sequence current controllers [2–5].

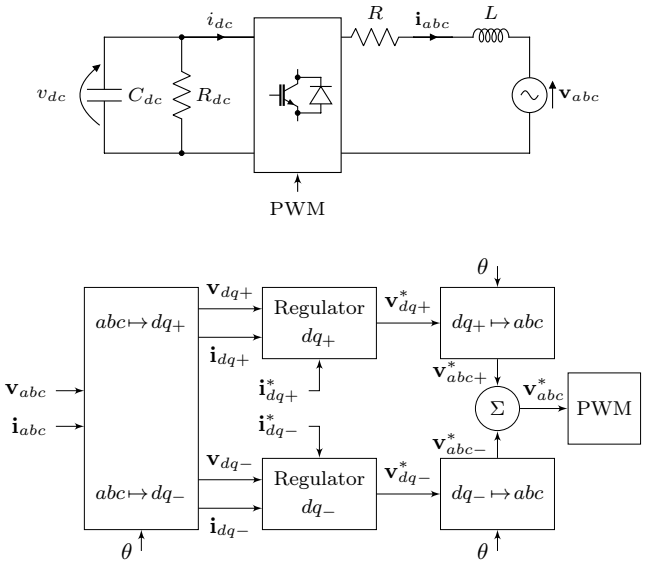

Fig. 1: VSC with dual-sequence current controller.

Fig. 1 shows a block diagram representation of a dual controller of a grid connected VSC. The controller operates with two RRFs and handles separately the positive and negative sequence of three-phase voltages and currents. The positive-sequence current references (i^*_{dq+}) are used as in a traditional single RRF controller [6] for regulation of the dc-link voltage and the reactive power exchange with the grid. The negative-sequence references (i^*_{dq-}), on the other hand, are calculated to reduce the second harmonic oscillations in the active power and dc-link voltage [2]. See Appendix A for the definitions of the reference-frame transformations used in this paper and Appendix B for the calculation procedure of the negative-sequence current references.

When an unbalanced three-phase measurement is transformed to a positive-sequence RRF, the positive-sequence

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content of the measurement becomes dc, whereas the negative-sequence component appears as second harmonic. The opposite happens when this same three-phase measurement is transformed to a negative-sequence RRF, namely the negative sequence becomes dc and the positive sequence becomes second harmonic. Different techniques have been employed in the literature of dual current controllers to isolate positive and negative sequences:

- notch filters tuned to the second harmonic were used in [2, 4, 7–9];
- the decoupled double rotating reference frame (DDRRF)[1] [10] was used in [5];
- the delayed signal cancellation (DSC) was employed in [3, 11].

The notch technique is applied directly to the RRF. The DDRRF, however, cross couples the outputs of low-pass filters from each RRF into the other one for cancelling the second harmonic. The DSC, on the other hand, is implemented in the stationary reference frame (SRF) [3, 11–13]. Both DDRRF and DSC add extra layers of complexity to the dual controller shown in Fig. 1.

This paper is an extension of the investigations presented in [14] on the performance of notch- and DDRRF-based dual-sequence current controllers operating in systems with high reactance-resistance ratio (X/R). In such systems, sudden changes at the ac voltage of the VSC induce non-negligible exponentially decaying dc currents. Those appear as the fundamental in both RRFs and have a detrimental effect in the stability of the VSCs. Therefore, conflicting requirements unfold when dual-sequence controllers operate in systems with high X/R. The controllers shall simultaneously 1) remove the second harmonic from the RRFs and 2) minimize phase shifts at the fundamental.

In this context, this work presents the following contributions:

1) a frequency adaptive discrete DSC algorithm for separation of positive and negative sequences directly in the RRF (DSC$_{dq}$). The proposed technique removes the intermediate step with filtering in the SRF demanded by the traditional DSC$_{\alpha\beta}$.
2) a mathematical proof of the equivalence between the DSC$_{\alpha\beta}$ and DSC$_{dq}$. To support the interpretation of the results, a computer simulation compares the performance of dual dq controllers operating in a system with high X/R and employing either DSC$_{\alpha\beta}$ or DSC$_{dq}$. Results show practically identical performances in the two implementations. Furthermore, the controllers using DSC are compared to a benchmark implementation using notch filters.
3) the application of a known technique [11] of averaging the outputs of two filters to reduce discretization errors and increase the robustness of the DSC$_{dq}$ algorithm to grid frequency variations. Contrary to the first intuition, this averaging demands the same amount of memory storage in the form of circular buffers as one single DSC.

[1]DDRRF was originally referred as DDSRF in [10]. In this paper, the "S" of synchronous is replaced by "R" of rotating to avoid confusion with stationary.

II. The Established DSC in the $\alpha\beta$ Frame

The DSC$_{\alpha\beta}$ combines old values from one axis of the SRF with new ones from the other axis. It is usually described with complex values in the literature [3, 11–13]. However, when expressed with vectors of real quantities, the DSC$_{\alpha\beta}$ becomes

$$\begin{bmatrix} m_{\alpha_+}(t) \\ m_{\beta_+}(t) \end{bmatrix} = \frac{1}{2}\left(\begin{bmatrix} m_\alpha(t) \\ m_\beta(t) \end{bmatrix} + \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} m_\alpha(t - T/4) \\ m_\beta(t - T/4) \end{bmatrix} \right), \tag{1}$$

where the vectors $[m_\alpha\ m_\beta]^{\mathrm{T}}$ are the representation in the SRF of the three-phase measurements, $[m_{\alpha+}\ m_{\beta+}]^{\mathrm{T}}$ contains the isolated positive sequence, and $T/4$ is the time delay, with T equal to the period of the fundamental frequency of the grid f. This thought process can be replicated for the negative sequence by inverting the sign of the grid angular frequency $\omega = 2\pi f$ [2] or swapping the measurements of phases b and c [14]. However, this is omitted for the sake of brevity.

From the perspective of the dq_+ frame, the negative sequence content is seen as a second harmonic. Therefore, it is a logical choice to use notch filters for separating the sequences as done in [2]. In this paper, a frequency-adaptive discrete notch filter [15] with a damping factor equal to $\sqrt{2}/2$ applied directly to the dq frame is used as benchmark for the DSC$_{\alpha\beta}$.

Fig. 2 shows the computer simulated response in dq_+ of the notch- and DSC$_{\alpha\beta}$-based methods to an ideal positive-sequence three-phase voltage with $1\,\mathrm{pu}$ amplitude supplied briefly for $0.39\,\mathrm{ms}$, i.e. a short pulse. The angle of the phase-to-neutral voltage v_a is available, therefore, it is used for the transformations between stationary and rotating frames. The outputs of the notch and DSC$_{\alpha\beta}$ methods shown at the bottom chart of Fig. 2 (red and blue) can be considered as filtered values of the ideal voltage measurement (dashed black). For the DSC$_{\alpha\beta}$, this is an indirect way of analyzing the method as it operates in the SRF and not in the RRF. Notwithstanding, an estimated frequency response can be obtained if the fast Fourier transform (FFT) of the outputs are divided, frequency by frequency, by the FFT of the ideal voltage measurement. This is known as empirical transfer function estimation [16].

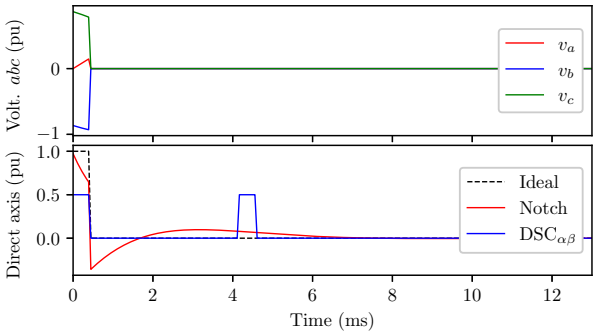


Fig. 2: Three-phase voltages (top) and d_+ axis measurements (bottom) of the notch and DSC$_{\alpha\beta}$ methods.

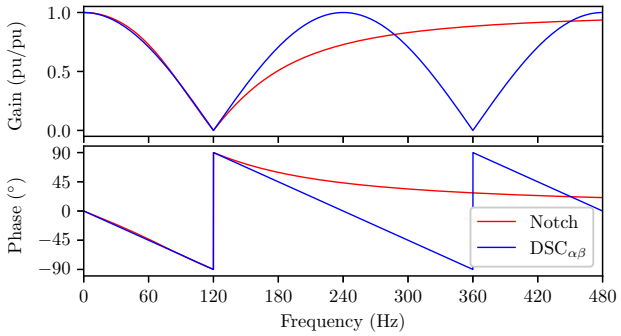


Fig. 3: Frequency responses on the d_+ axis of the notch and DSC$_{\alpha\beta}$ methods.

Fig. 3 shows the frequency responses on the d_+ axis of the notch and DSC$_{\alpha\beta}$ methods. Both methods have unitary gain and zero phase shift at dc. Between dc and the second harmonic, the gains begin to drop almost identically in conjunction with larger phase shifts. The behavior of the filters differs considerably after the second harmonic because the notch has an infinite impulse response whereas the DSC$_{\alpha\beta}$ has a finite impulse response (FIR). The notch technique removes only the second harmonic, whereas the DSC removes from the RRFs all harmonics equal to $4k-2$, with the integer $k \geq 1$. An analysis of the consequences of these differences in the higher part of the spectrum is considered beyond the scope of this paper.

III. The Proposed DSC Directly in the dq Frame

The output of a digital FIR filter is the weighted sum of the current input and a given number of previous (delayed) inputs [17]. It is interesting to remark that the number of delayed inputs of a FIR filter and their weights can be identified from the filter's response to a unit pulse. Hence, from Fig. 2, it is possible to deduce that the DSC$_{\alpha\beta}$ can be performed directly in the RRF as

$$\begin{bmatrix} m_{d_+}(t) \\ m_{q_+}(t) \end{bmatrix} = \frac{1}{2}\left(\begin{bmatrix} m_d(t) \\ m_q(t) \end{bmatrix} + \begin{bmatrix} m_d(t-T/4) \\ m_q(t-T/4) \end{bmatrix} \right), \tag{2}$$

where the vectors $[m_d\ m_q]^{\mathrm{T}}$ are the representation in the RRF of the three-phase measurements and $[m_{d+}\ m_{q+}]^{\mathrm{T}}$ contains the isolated positive sequence.

Differently from (1), the axes are independent from each other in (2). Despite that, (1) and (2) are mathematically equivalent. If the $\alpha\beta$ quantities of (1) are written on the dq frame with the inverse of the matrix $\mathbf{P}$ from (A.2) and both sides of the equation are multiplied by $\mathbf{P}$, the result is:

$$\begin{bmatrix} m_{d_+}(t) \\ m_{q_+}(t) \end{bmatrix} = \frac{1}{2}\left(\begin{bmatrix} m_d(t) \\ m_q(t) \end{bmatrix} + \right.$$
$$\left. + \mathbf{P}(\omega,t) \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \mathbf{P}^{-1}\left(\omega, t-T/4\right) \begin{bmatrix} m_d(t-T/4) \\ m_q(t-T/4) \end{bmatrix} \right). \tag{3}$$

Notice that the angular frequency of the grid is $\omega = 2\pi f$ and the period of the grid is $T = 1/f$, thus $\omega T/4 = \pi/2$. Consequently, the multiplication of the square matrices on the right-hand side of (3) can be written as

$$\mathbf{P}(\omega,t) \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \mathbf{P}^{-1}(\omega, t-T/4) =$$
$$\begin{bmatrix} \sin(\omega t) & -\cos(\omega t) \\ \cos(\omega t) & \sin(\omega t) \end{bmatrix} \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$$
$$\begin{bmatrix} \sin(\omega t - \pi/2) & \cos(\omega t - \pi/2) \\ -\cos(\omega t - \pi/2) & \sin(\omega t - \pi/2) \end{bmatrix} =$$
$$\begin{bmatrix} -\cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & -\cos(\omega t) \end{bmatrix} \begin{bmatrix} -\cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & -\cos(\omega t) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{4}$$

In summary, performing (1) in the $\alpha\beta$ frame and transforming the result to the RRF is mathematically equivalent to performing (2) directly in the dq frame.

IV. Frequency Adaptive DSC$_{dq}$

The grid frequency of low-inertia power systems is subject to large excursions specially during transients. Thus, the sequence separation algorithm of dual current controllers should not be unreasonably degraded by such variations. The digital implementation of a frequency adaptive DSC$_{dq}$ demands the discretization of the time-varying delay $T(t)/4$. In the discrete time domain, the number of samples $n(k)$ equivalent to $T(t)/4$ is given by

$$n(k) = \frac{T(k)}{4T_s} = \frac{f_s}{4f(k)}, \tag{5}$$

where f_s is the sampling frequency with which the DSC algorithm is processed, T_s is the sampling time, and the ever-increasing integer k represents the discrete time kT_s. Then, the discrete implementation of (2) in one of its axis becomes

$$y(k) = \frac{x(k)}{2}\left(1 + z^{-n(k)}\right), \tag{6}$$

where x denotes the input of the filter, y the output, and the operator z^{-n} fetches the value of the variable x at the instant $k-n$.

A time-varying grid frequency produces noninteger values of n which must be truncated or rounded. Fig. 4 shows a block diagram representation of a frequency adaptive DSC$_{dq}$ based on (6) that rounds $n(k)$ to the closest integer. To understand the consequences of this approximation, the calculated frequency responses of two filters are presented in Fig. 5. The filters run at $f_s = 18\,\mathrm{kHz}$ and have delays of $n_c = 75$ (red) and $n_f = 74$ (blue). The frequencies in which they have zero gain

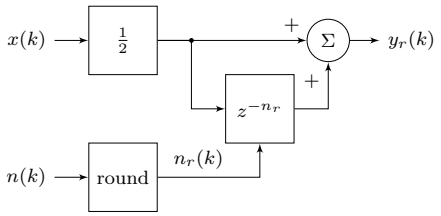


Fig. 4: Frequency adaptive DSC$_{dq}$ with rounded $n(k)$.

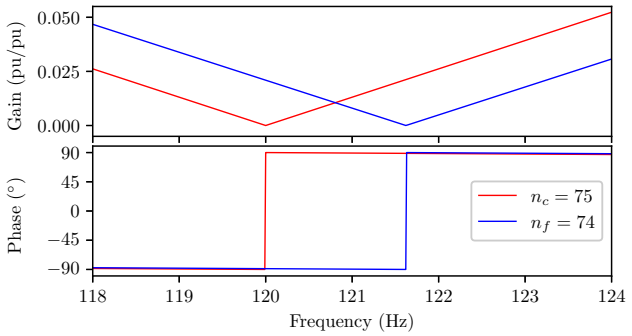


Fig. 5: Frequency responses of two DSC$_{dq}$ filters running at 18 kHz with delays of 74 and 75 samples.

are 120 Hz for n_c and 121.622 Hz for the given n_f. For any frequencies in between those ones, the gain is non-zero. As a result, a small content of the opposite sequence will pass through the DSC$_{dq}$ filters if the grid frequency is between 60 and 60.811 Hz. Remark that the lower f_s is, the wider is the gap between frequencies with zero gain of two DSC$_{dq}$ filters with contiguous delays.

The phases of the two filters with $n_c = 75$ and $n_f = 74$ in Fig. 5 are almost 180° apart between 120 Hz and 121.622 Hz. This fact is illustrated in the time domain by the results of a computer simulation shown in Fig. 6. On the top chart, a set of frequency-varying three-phase voltages with a positive sequence amplitude of 1 pu and a negative sequence amplitude of 0.1 pu is shown. The frequency of the three-phase voltages is known and is used for calculating the time delay n with its ceiling and floor values (middle chart). The angle of the positive sequence fundamental is also known and is used as input to the $abc \mapsto dq$ transformation. On the bottom chart, the d_+ measurements are shown. The amplitude of the second harmonic oscillations in the measurement with n_c, denoted by v_{d+c}, increases as the value of n drifts from n_c. Concurrently, the amplitude of the oscillations in the measurement v_{d+f} decreases as the value of n approaches n_f.

The responses observed in Figs. 5 and 6 allow the use of a weighted average method which combines the outputs of the filters as follows:

$$y_w(k) = \gamma(k) y_f(k) + (1 - \gamma(k)) y_c(k), \qquad (7)$$

where y_w is the weighted average output, y_f is the result of (6) with the floor of n, y_c is the result with the ceiling of n, and $\gamma(k) = n_c(k) - n(k)$. It is important to remind that n is constantly updated according to (5). This weighted average was proposed in [11] for the DSC$_{\alpha\beta}$ and was also used in [18] for adaptive moving averages. Remark that this method reduces but does not completely remove the second harmonic present in v_{d+w} in Fig. 6.

Fig. 7 shows a block diagram representation of (7). The delay operators z^{-n_c} and z^{-n_f} are typically implemented with circular buffers [17]. It is natural to assume that calculating $y_w(k)$ from Fig. 7 requires twice the amount of memory necessary for calculating $y_r(k)$ from Fig 4. Indeed, this is

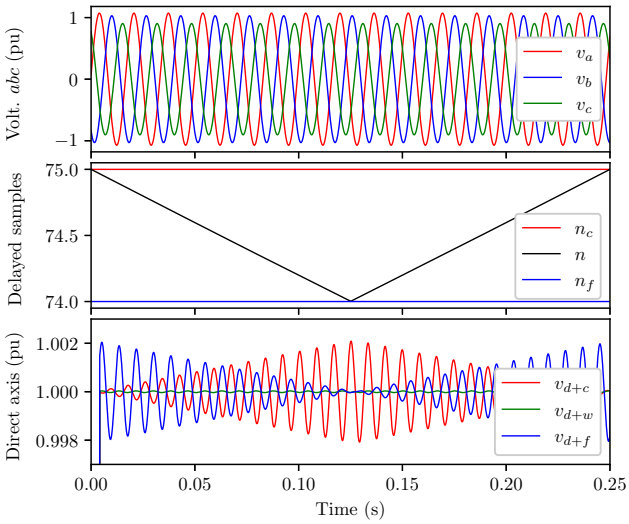


Fig. 6: Unbalanced three-phase voltages with varying frequency (top); n samples corresponding to $T/4$ and its ceiled n_c and floored n_f values (middle); d_+ measurements with the proposed frequency adaptive DSC$_{dq}$ algorithms (bottom).

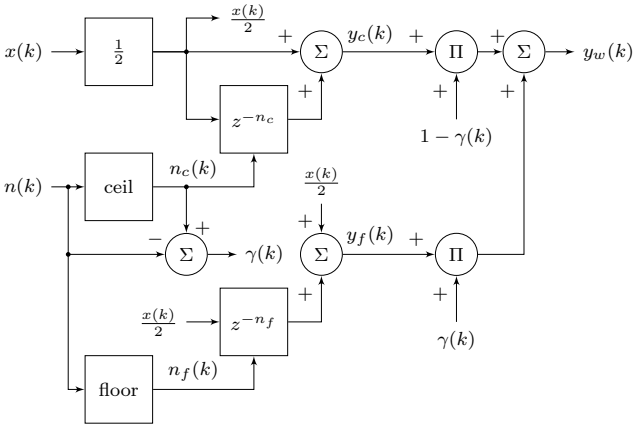
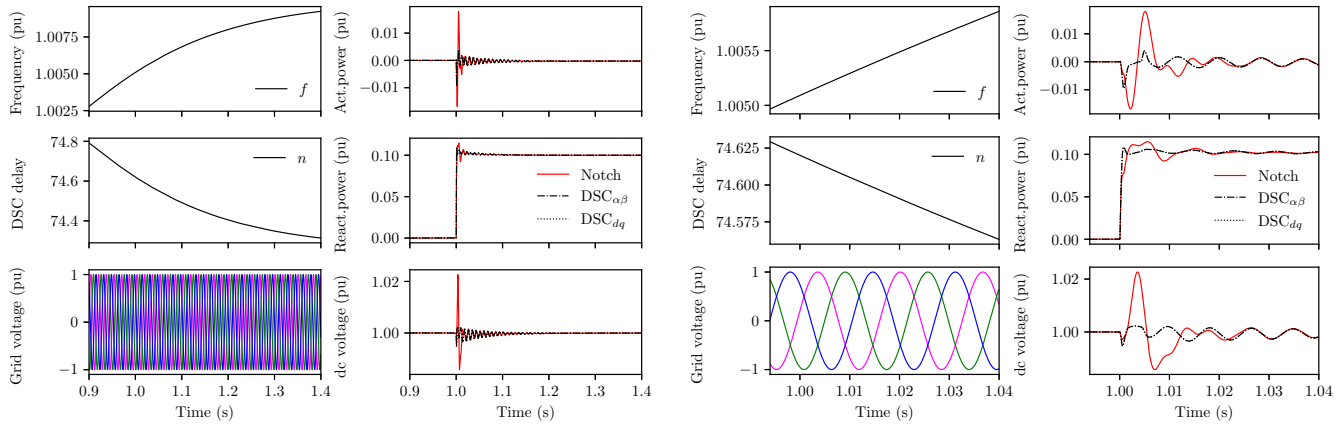


Fig. 7: Frequency adaptive DSC$_{dq}$.

not the case. The length of the DSC's circular buffers is determined by the longest expected delay, i.e., the lowest acceptable grid frequency. A pointer, which moves continuously forward through the circular buffer, indicates where the new value of $x(k)/2$ is to be stored replacing a value that became too old. This pointer can be called the insertion one. Other two pointers, the retrieval ones, lag behind the insertion pointer indicating from where the old values $x(k-n_c)/2$ and $x(k-n_f)/2$ are to be retrieved. The two filtered values y_c and y_f in (7) are, thus, calculated with one single circular buffer with two contiguous retrieval pointers running in parallel. The interested reader is invited to inspect the proposed algorithm in detail at [19].



(a) Complete transient.

(b) Detail of the transient.

Fig. 8: Comparison of the DSC$_{\alpha\beta}$, DSC$_{dq}$, and notch-based methods; balanced grid; step in i^*_{q+}.

V. Comparing the Performance of Dual Controllers with Notch, DSC$_{\alpha\beta}$, and DSC$_{dq}$

In this section, a comparison of the performance of dual controllers equipped with either DSC$_{\alpha\beta}$ or DSC$_{dq}$ is presented. This is done via computer simulations using the conceptual model of a VSC connected to a three-phase voltage source through a highly inductive impedance employed in [14], see more in Appendix C.

Two cases are analyzed, one with a balanced and one with an unbalanced grid voltage. The tuning [20] of the inner proportional and integral (PI) regulators and the outer dc-voltage regulator is identical in all cases. A reactive power regulator is not implemented. Dual controllers equipped with notch filters may present a more oscillatory behavior than controllers using DSC [3]. Despite that, notch filters are employed for sequence isolation by authors closely linked to the industry [4, 21]. For this reason, a controller with notch-based sequence isolation is used as benchmark in this section.

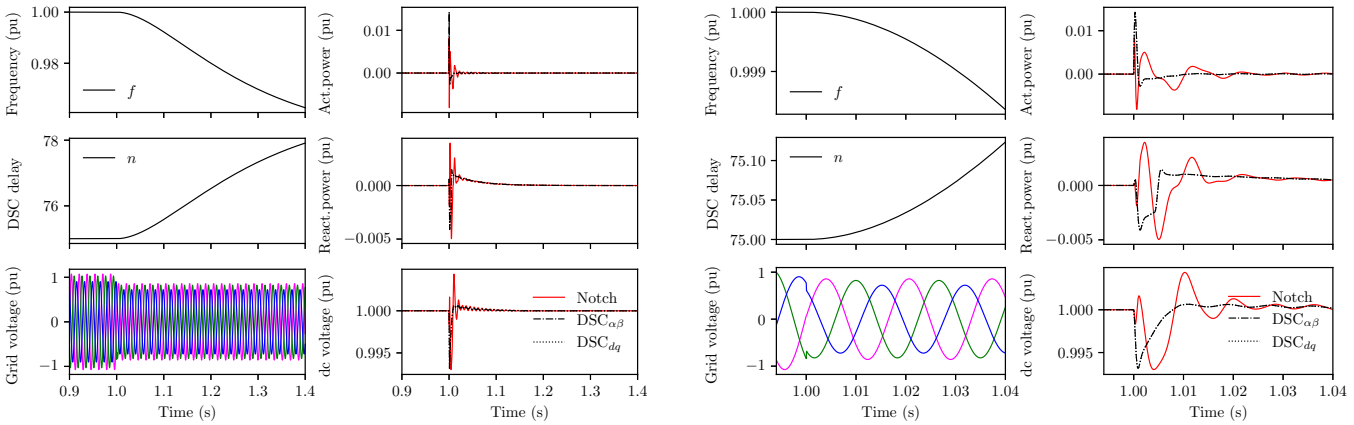
Fig. 8a shows the results of the simulations when the grid voltage is balanced and has an amplitude of $1\,\text{pu}$. A detail of the transient is shown in Fig. 8b. The grid frequency f increases during the simulations, thus, the resulting delay n for the DSC filters decreases. The frequency measurement is ideal, hence, there are no delays caused by the phase-locked loop (PLL). At the instant $t = 1\,\text{s}$, a $-0.1\,\text{pu}$ step is applied at i^*_{q+}. All three regulators respond quickly and the reactive power rises to $0.1\,\text{pu}$ within $2\,\text{ms}$. A small and damped second harmonic oscillation is observed after the transient in the active and reactive powers, as well as in the dc voltage. Remark that the response of the controller with notch filters is more oscillatory in the first grid period after the step in i^*_{q+}. Note also that the responses of the regulators with DSC$_{\alpha\beta}$ and DSC$_{dq}$ are practically identical. The maximum difference between the dc-voltages of the controllers with DSC in the balanced grid case is $18.4 \times 10^{-6}\,\text{pu}$ at $t = 1.005\,\text{s}$.

Fig. 9 presents the unbalanced case. Initially, the amplitude of the positive sequence of the grid voltage is equal to $1\,\text{pu}$ and the amplitude of the negative sequence is equal to $0.1\,\text{pu}$. The outer dc-link voltage regulator and the inner dual-sequence current controller manage to maintain a constant dc voltage at $1\,\text{pu}$ despite the unbalance. At the instant $t = 1\,\text{s}$, the positive and negative sequence amplitudes of the grid voltage drop to $0.8\,\text{pu}$ and $0.08\,\text{pu}$, respectively. Simultaneously, the frequency f begins to drop causing the delay n of the DSC filters to increase. The transient in the grid voltage prompts oscillations in the active and reactive powers in the first $25\,\text{ms}$. An oscillation in the dc voltage is also observed after the drop in the grid voltage, however, the dc controller manages to dampen it. The maximum difference between the dc-voltages of the controllers with DSC in the unbalanced grid case is $30.0 \times 10^{-6}\,\text{pu}$ at $t = 1.061\,\text{s}$.

TABLE I: Integral of the absolute error (IAE) of the dc-link voltage from times $1\,\text{s}$ to $2\,\text{s}$ of the cases shown in Figs. 8 and 9.

Case	**Notch** IAE (pu × s)	**DSC$_{\alpha\beta}$** IAE (pu × s)	**DSC$_{dq}$** IAE (pu × s)
Balanced	227.4×10^{-6}	141.1×10^{-6}	140.0×10^{-6}
Unbalanced	73.9×10^{-6}	49.4×10^{-6}	50.0×10^{-6}

It is interesting to use the integral of the absolute error (IAE) of the dc voltage to compare the simulation results in Figs. 8 and 9, see Table I. For that, the absolute value of the error between the measured dc-link voltage and the reference was integrated between $t = 1\,\text{s}$ and $t = 2\,\text{s}$. These are the times where the disturbance is applied to the system and a new steady-state is achieved. The dc-link voltage reference is equal to $1\,\text{pu}$ in all cases. Note that the lower the IAE, the better the performance of the regulator is. As expected from the results in Figs. 8 and 9, the controller with notch filters features the highest IAE in both balanced and unbalanced cases. The controller with DSC$_{dq}$ is marginally better than the one with DSC$_{\alpha\beta}$ in the balanced case, whereas the DSC$_{\alpha\beta}$ is



(a) Complete transient.

(b) Detail of the transient.

Fig. 9: Comparison of the DSC$_{\alpha\beta}$, DSC$_{dq}$, and notch-based methods; unbalanced grid; drop in the voltage.

marginally better in the unbalanced case.

In Section III, the equivalence between DSC$_{\alpha\beta}$ and DSC$_{dq}$ was formally proven. The computer simulations in this section corroborate this fact. The performance of the controllers employing the two DSC methods are, with the exception of negligible errors, identical.

VI. Conclusions

This paper introduced a new discrete, frequency adaptive DSC algorithm to separate positive and negative sequence measurements directly in the RRF. The proposed technique simplifies the practical implementation of dual-sequence current controllers for grid-connected VSCs, as it eliminates an intermediate filtering step in the SRF. Consequently, the controller can operate solely with two RRFs.

The established DSC method in the SRF was reviewed and its performance compared on time and frequency domains to a benchmark discrete notch filter via computer simulations. This comparison was used as base to derive the proposed algorithm and the mathematical equivalence between the DSC in the SRF and RRF was formally proven.

In addition, a known technique of averaging the outputs of two filters with contiguous integer delays was employed to reduce discretization errors caused by excursions of the grid frequency. Contrary to the first intuition, this averaging demands the same circular buffer size as a single DSC.

Finally, computer simulations of a VSC connected to the grid via a highly inductive impedance showed a practically identical behavior of dual-sequence controllers employing DSC in the SRF or the RRF. Under the same conditions, those also displayed less oscillatory behavior during transients than the benchmark controller with notch filters.

Appendix A
Transformations and Reference Frames

The three-phase VSCs considered in this paper are connected to the grid via an ungrounded delta-wye transformer. Therefore, the zero sequence is disregarded.

The $abc \mapsto \alpha\beta_+$ transformation is performed with the matrix

$$\mathbf{C}_+ = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}. \tag{A.1}$$

The $\alpha\beta \mapsto dq$ transformation uses the matrix

$$\mathbf{P}(\omega, t) = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) \\ \cos(\omega t) & \sin(\omega t) \end{bmatrix}, \tag{A.2}$$

where ω is the angular frequency of the grid. The complete $abc \mapsto \alpha\beta_+ \mapsto dq_+$ transformation is given by

$$\begin{aligned} \begin{bmatrix} m_{d+}(t) \\ m_{d+}(t) \end{bmatrix} &= \mathbf{P}(\omega, t) \begin{bmatrix} m_{\alpha+}(t) \\ m_{\beta+}(t) \end{bmatrix} \\ &= \mathbf{P}(\omega, t) \left(\frac{2}{3} \mathbf{C}_+(t) \begin{bmatrix} m_a(t) \\ m_b(t) \\ m_c(t) \end{bmatrix} \right), \end{aligned} \tag{A.3}$$

where $[m_a \ m_b \ m_c]^{\mathrm{T}}$ are the instantaneous phase-to-neutral voltages or line currents. Moreover, the phase of the grid voltage between phase a and the neutral is adopted as zero, i.e., $v_a(t) = V \sin(\omega t)$.

The transformation to the negative RRF is performed by swapping the measurements of the phases b and c. This is equivalent to swapping two columns of (A.1):

$$\mathbf{C}_- = \mathbf{C}_+ \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}. \tag{A.4}$$

The complete $abc \mapsto \alpha\beta_- \mapsto dq_-$ transformation is given by

$$\begin{aligned} \begin{bmatrix} m_{d-}(t) \\ m_{d-}(t) \end{bmatrix} &= \mathbf{P}(\omega, t) \begin{bmatrix} m_{\alpha-}(t) \\ m_{\beta-}(t) \end{bmatrix} \\ &= \mathbf{P}(\omega, t) \left(\frac{2}{3} \mathbf{C}_-(t) \begin{bmatrix} m_a(t) \\ m_b(t) \\ m_c(t) \end{bmatrix} \right). \end{aligned} \tag{A.5}$$

TABLE C.I: Conceptual Model Data.

Parameter	Value
Rated frequency	60 Hz
Controller sampling frequency	18 kHz
Rated ac voltage (peak phase-to-ground)	1 V
Rated ac current (peak line)	1 A
Rated dc voltage	$\sqrt{3}$ V
Rated dc current	$\sqrt{3}/2$ A
Main reactor inductance L	1.326 mH
Main reactor resistance R	2.5 mΩ
DC-link capacitance C_{dc}	0.5305 mF
DC-link parasitic shunt resistance R_{dc}	1 MΩ
Proportional gain K_i	4 pu/pu
Integrator time T_i	53.05 ms
Proportional gain K_v	0.5 pu/pu
Integrator time T_v	150 ms

APPENDIX B
NEGATIVE-SEQUENCE CURRENT REFERENCES

The negative-sequence current references are calculated to minimize the second harmonic in the active power exchange between converter and grid [22]. When the transformations in Appendix A are considered, the negative-sequence current references are given by

$$\begin{bmatrix} i^*_{d-} \\ i^*_{q-} \end{bmatrix} = -\begin{bmatrix} -v_{d+} & v_{q+} \\ v_{q+} & v_{d+} \end{bmatrix}^{-1} \begin{bmatrix} -v_{d-} & v_{q-} \\ v_{q-} & v_{d-} \end{bmatrix} \begin{bmatrix} i^*_{d+} \\ i^*_{q+} \end{bmatrix}. \quad \text{(B.6)}$$

APPENDIX C
SIMULATION DATA

The computer simulations presented in this paper are based in a conceptual model introduced in [14]. The simplified block diagram of the model is shown in Fig. 1. A two-level insulated-gate bipolar transistor converter is connected to an ideal three-phase voltage source through a highly inductive impedance. The dc link of the converter consists of a capacitor with a parasitic shunt resistance. The frequency of the grid voltage is known and is used in the simulation, therefore, no delays due to the PLL are introduced in the comparisons of the performance of the different sequence-separation methods. Moreover, an average model of the converter is employed, i.e., the effects of the converter switching frequency are disregarded. Table C.I summarizes the model data.

Fig. C.1 shows a simplified structure of the PI regulators used in this paper. For clarity, the anti-windup structures are not represented. An outer loop controls the dc voltage generating the positive-sequence current reference i^*_{d+}. The reference i^*_{q+} controls the positive-sequence reactive current delivered by the converter to the grid. The negative-sequence current references are calculated with (B.6). The tuning of the PI controllers of the inner current regulators is identical. A feed-forward scheme of the grid voltage is employed, and the decoupling between d and q frames is performed by the ωLi terms. Note that a discussion of different decoupling schemes is considered outside the scope of this paper. Notwithstanding, models, parameters, and resulting data are available at [19].

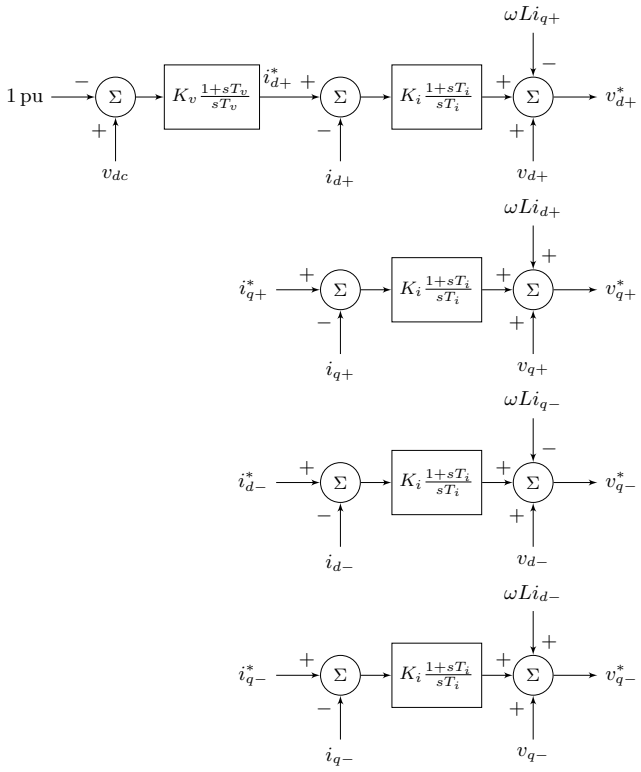


Fig. C.1: PI controllers.

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