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Design and Analysis of a Reconfigurable Gilbert Mixer for Software-Defined Radios

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Abstract: A reconfigurable g_m-boosted, image-rejected downconversion mixer is presented in this paper using the SiGe 8 HP technology. The proposed mixer operates within 0.9–13.5 GHz that is suitable for software-defined radio applications. The conversion mixer comprises of resistive biased radio frequency (RF) section, double balanced Gilbert cell mixer core sections divided as per I and Q stages for image-rejection purpose, inductively peaked g_m-boosting section and tunable filter section, respectively. In comparison to previous works in the scientific literature, the design shows enhanced conversion gain (CG), noise figure (NF), and image-rejection ratio (IRR). For the entire band of operation, the mixer attains a good return loss $|S_{11}|$ of <-10 dB. Additionally, the design accomplishes an excellent CG of 22 dB, NF of 2.5 dB, and an image-rejection ratio of 30.2 dB at maximum frequency. Finally, a third-order intercept point (IP3) of -3.28 dBm and 1 dB compression point (CP1) of -13 dBm, respectively, shows moderate linearity performance.

Keywords: software-defined radio; mixer; image-rejection ratio; impedance matching

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1. Introduction

Wireless communications have become increasingly popular due to the wide range of potential applications. In recent years, this industry has experienced tremendous development leading to many wireless standards. Therefore, it is desired to have a radio front end that is capable of handling multiple standards and applications [1–3]. For developing such receiver circuits, especially within high-frequency bands, proper radio frequency (RF) and baseband blocks must be available to perform downconversion operation. Ideally, distinct radio front ends can be used for different standards and applications. However, this is not possible due to frequency sensitivity [4,5]. Hence, RF-front-ends are compatible with distinct standards operating at specific frequencies. In addition, one must develop advanced systems with modern blocks with the emergence of the latest wireless standards. Reconfigurable blocks can be reused to accommodate multiple wireless standards, and thus lower development time and cost [6]. Software-defined radios (SDRs) offer this flexibility by allowing multiple band operations inside a single circuitry [7,8], whereas cognitive radios (CRs) take care of spectrum crowding and congestion hurdles [9,10]. Although most of the research is based on single-band cognitive radio, multiband cognitive radio has greater potential in the efficient implementation of cognitive networks. It is expected that multiband cognitive radios improve the throughput and lower handoff frequency for better channel maintenance. However, wideband front end and access to multiband spectrum present several challenges [11]. Thus, the best is to have CR with SDR features, which can sense the electromagnetic spectrum environment, tracking and responding to the variations and findings in a smart way. Moreover, the cost and power consumption are significant while talking about reconfigurable receiver architectures [12]. Earlier receivers were using analog-to-digital converters. Signal processing is carried out in the digital domain that

consumes high power and attains inaccurate RF signals, which limits the use of SDRs. Thus, to overcome that, mixers must be used [13].

Mixers are used for frequency conversion purposes. Upon mixing, the frequency of the output signal is in the form of a sum or difference of those of the input signals. Within the receiver, mixers can perform frequency downconversion to shift RF to IF [14]. For good performance with low NF, high linearity, polarity switching through local oscillator (LO) input is required. Such a mixer will have radio frequency (RF) signals divided into in-phase and out-of-phase parts; the conversion switch operated by LO signal can alternatively choose in-phase and out-of-phase signals. Ideally, mixers will introduce the minimum amount of noise and have good linearity [15]. Moreover, they should be independent of LO amplitude and intermodulation products. However, practical mixers have the following limitations: non-negligible NF, limited CG, and linearity [16]. Mixers are broadly classified as passive mixers and active mixers. Passive mixers introduce signal attenuation and mixing is achieved through passive switches. Therefore, the switches are turned on and off depending on the LO signal, which is compared to a reference voltage and mixing is achieved through the multiplication operation of RF and LO frequency signals (in terms of square wave or sinewave). These mixers are widely used because of their simplicity, zero power consumption, high IP3, and good NF at the expense of port isolation. However, its main drawback is the high LO power requirement [14]. In contrast to passive mixers, active mixers can provide high CG, good port isolation, low NF, and low LO power requirements. However, it is difficult for them to achieve good linearity. Thus, based on the advantages, active mixers are preferred over passive mixers. Among active mixers, Gilbert mixer is the most commonly used architecture that follows a double balanced structure. This configuration shows high isolation [17]. The mixer also attains high performance in terms of CG, NF at the expense of linearity [18]. The systematic approach can be used further to improve the overall performance that estimates the proper width-to length (W/L) ratio to attain the required design specifications. This approach shows a good trade-off among different performance parameters [19].

For SDR, a single mixer operating within a wideband would be able to convert multiple RF signals to a single IF signal, reducing the design complexity and overall cost [20]. In general, the overall performance of the receiver depends on various metrics such as dynamic range, IP3, NF, CG, IRR, filtering, signal-noise ratio, and spurious-free dynamic range, respectively. Nevertheless, there are no industrial standards defined for SDRs, but they should be able to attain at least high CG, high IRR, and low NF, respectively [21]. Additionally, SDR mixers should be able to provide linear operation while maintaining stability. However, there are a limited number of SDR mixers that provide good reconfiguration, cover a wide bandwidth, and attain high IP3 due to additional circuitry requirements [22,23]. The design complexity should also be low while consuming low power to prolong the battery lifespan [24].

Reconfigurable SDR mixers can be either switchable or tunable. In case of switchable SDR mixers, reconfiguration is possible using switches along with other components such as inductors, transformers. However, tunable mixers use tunable resonators for reconfiguration. With strict bandwidth requirements, analog or discrete tuning can be opted. Numerous techniques exist for possible tuning of operating frequency, among which typical techniques include transmission line-based designs with limited frequency of operation [25,26], transformer dependent inductors with variable frequency of operation [27], analog bias tuning with limited tuning range, array arranged filters, charge domain discrete-time filters [28], and polyphase networks [29], respectively. Tuning is important to lower the RF front-end section area for multifunctional, multiple frequency, and multistandard applications. Moreover, easy reconfiguration will be done as per the parameters' necessity with respect to the standards, band of operation and overall performance. Thus, it is expected to have a single tunable filter that can replace the large and expensive filter banks, has a wide operating band, and can be easily optimized as per the standards, band or requirements. Moreover, it should cover a small chip area and consumes less power [30].

Hence, for proper reconfiguration to occur, it is important to have perfect tuning based on the above-mentioned approaches.

Gilbert mixer is quite common among SDR receiver architectures as they can provide high bandwidth and broadband performance without degradation in the performance parameters [31]. Several mixer designs have been discussed in [32–37]. As in [38], improved Gilbert mixer design is proposed that attains reasonable CG and high port isolation while operating within a wideband. Likewise, in [39] a reconfigurable Gilbert mixer is proposed that employs a passive switchable network (a combination of switched capacitor and inductors) for tuning purposes, resulting in a highly flexible design. The design attained high CG, moderate IP3 at the expense of NF. To overcome the issues within the above-mentioned designs, a joint LNA + mixer-based design can be used. The proposed design maintains a small chip size and consumes less power [40]. Noise-cancelling plays an important role for such a front-end topology. However, it depends on the proper metric matching based on I/Q mixer topology. Another common approach is to use partial noise-cancelling with a folding mixer architecture with no current reuse, specifically for wideband and low power operation. In this case, g_m-boosting is the better option, which is independent of performance metrics matching as used in LNA section. Finally, in [5], a g_m-boosted technique is employed in the RF stage of the mixer that helps in CG improvement with low power consumption.

Based on the above-mentioned approaches, a novel Gilbert mixer is proposed that employs g_m-boosting technique with high image rejection. For tuning purposes, the ninth-order tunable resonator has been developed using varactors and inductors, where the varactors are responsible for providing tuning behavior within the mixer. In this paper, we discuss the design and analysis of the mixer achieving tunable input-output matching from 0.9 GHz to 13.5 GHz. The rest of the paper is organized as follows: Section 2 focuses on motivation. Section 3 presents the mixer design, followed by the analyses of the proposed mixer in Section 4. Section 5 discusses about the simulation results and the layout of the proposed mixer. The proposed mixer's reliability performance is analyzed using Relxpert software as discussed in Section 6 and finally Section 7 concludes the paper.

2. Motivation

A merged LNA and mixer circuitry is shown in Figure 1. It consists of g_m-boosting section, and a source inductor at the input end. At the output end capacitors and inductors (ignoring parasitic resistance) are connected to the LNA section. LNA and mixer employ g_m-boosting and current bleeding techniques, which makes the design capable of attaining high CG, low NF, and low power consumption. The design also employs the current peaking approach for wideband operation [40]. Therefore, the input and output impedance can be expressed using a small signal model as shown in Figure 2.

Input impedance, Z_{in} can be expressed as:

$$Z_{in} = \frac{sL_1}{1 + (G_{m1} + sC_{gs1})sL_1} \tag{1}$$

where C_{gs1} refers to the gate to source capacitance at the input end. G_m-boosting helps in overall gain improvement as it improves the overall transconductance in the stage to which it is connected by the factor $(-A)$ as shown in Figure 1. Upon analysis, it can be expressed as

$$G_{m1} = \frac{r_{01} + Z_L}{1 + 2g_{m1}r_{01}} \tag{2}$$

where G_{m1} refers to g_m-boosting term; g_{m1}, r_{01}, and Z_L refer to the transconductance, transistor impedance, and load impedance, respectively. Similarly, the output impedance, Z_L can be expressed as:

$$Z_L = \frac{1}{sC_1}||[sL_3 + (\frac{1}{sC_2})||sL_5||(\frac{1}{g_{m3}}||\frac{1}{g_{m4}})] \tag{3}$$

where C_1, C_2 refers to the interstage parasitic capacitance. g_{m3} and g_{m4} refer to the transconductance of M_3 and M_4 transistors. As per the input network, the resonant frequency depends on C_{gs1} and L_1. The resonant frequency at which the input impedance, Z_{in} will be real can be defined as

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_{gs1}}} \tag{4}$$

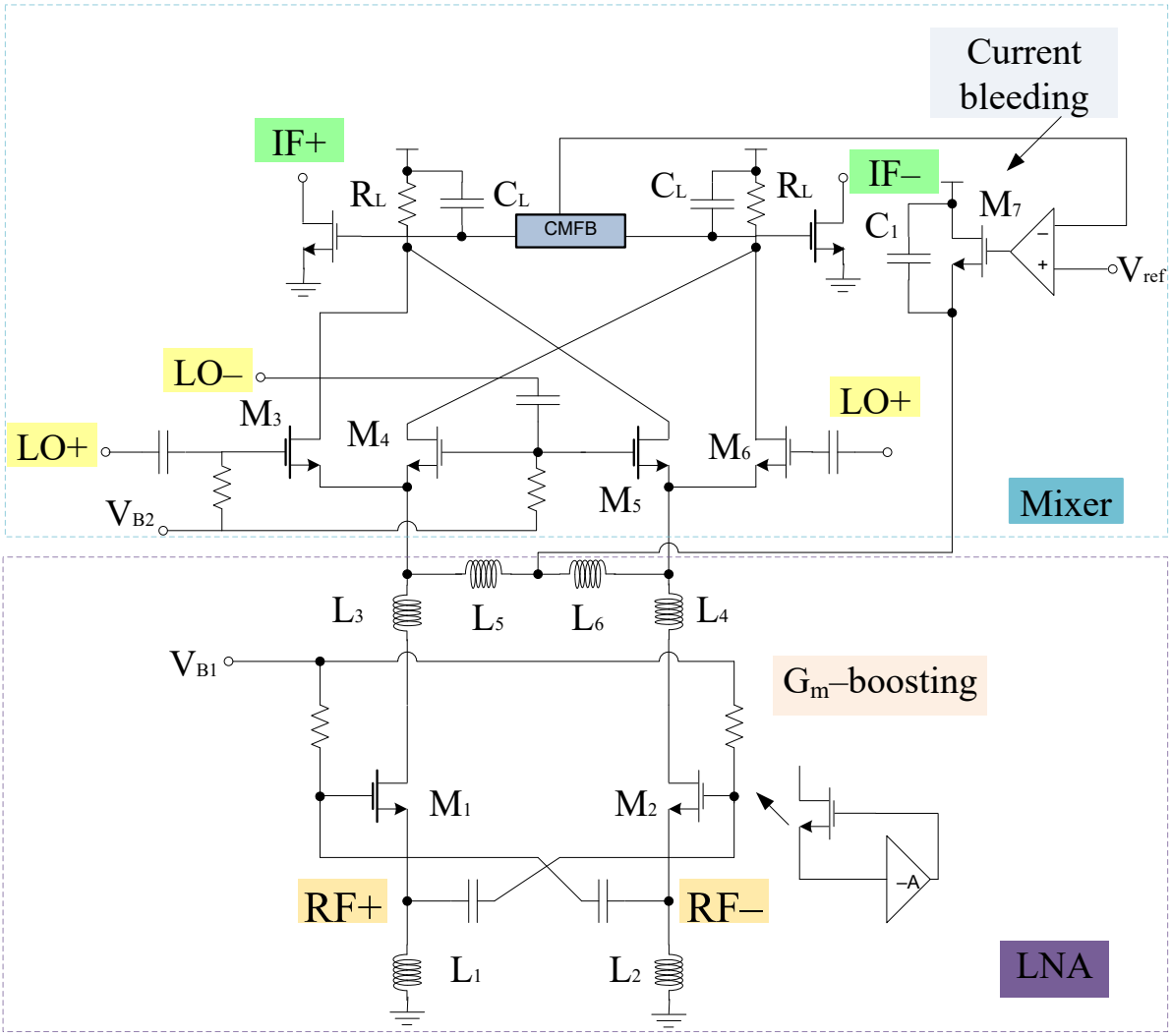

Figure 1. Merged LNA and mixer.

Therefore, to attain the tunable frequency, f_0 and input impedance, it is desired for Z_{in} to use the tunable filter components. This will enhance not only the overall chip area and power consumption but also the performance metrics such as noise figure. In this paper, we propose an active mixer with a tunable filter, comprising of variable capacitors and inductors. Therefore, in order to attain the minimum return loss, S_{11} at each centered frequency, the input impedance can be varied with the variation in the current. To improve the performance of the circuitry, the design also employs the g_m-boosting technique.

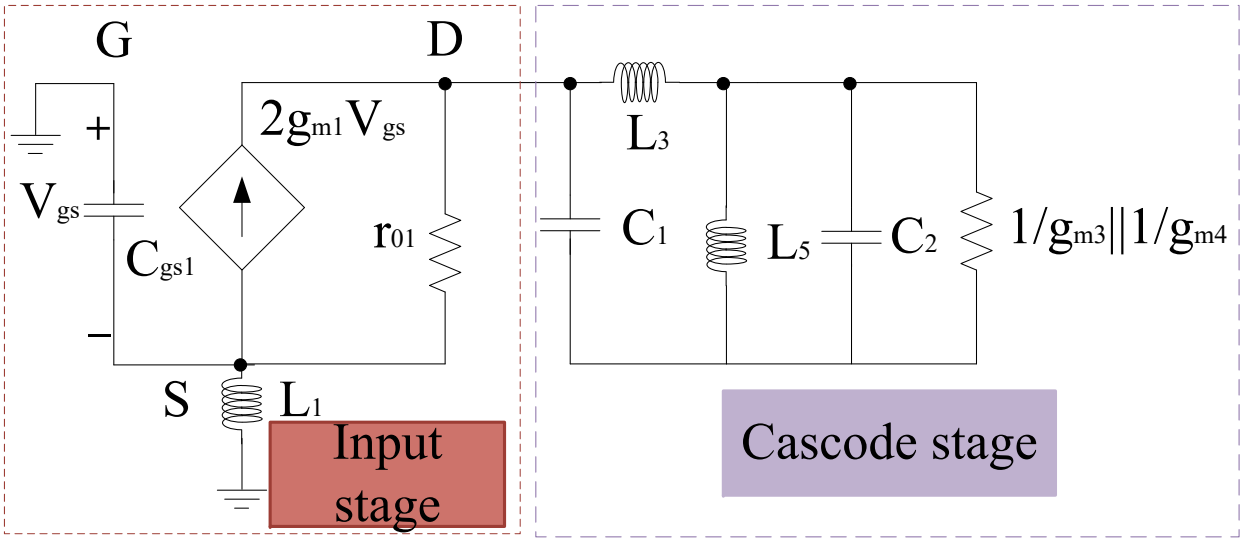

Figure 2. Small signal model.

3. Proposed Mixer Topology

Figure 3 shows the block representation of the proposed mixer with different stages. Starting from the bottom, Stage I refers to the transconductance stage that follows a common source configuration. Stage II refers to the core section categorized into LOI (local oscillator in-phase) and LOQ (local oscillator out-of-phase) stages where input signals are in 90 degree phase shift with respect to each other. For coupling, transconductance and core stages, coupling capacitors have been used. The third stage refers to the g_m-boosting stage and finally, stage IV discusses the filters, i.e., first-order filter for avoiding leakage from the power supply and the ninth-order tunable filter for impedance matching at RF and IF stages. For a better understanding of the proposed circuit topology, the design and analysis of all stages have been discussed as follows.

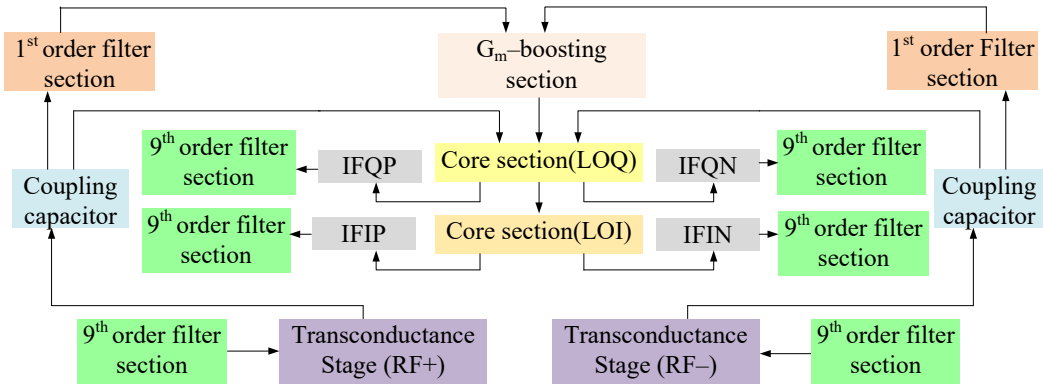

Figure 3. Block diagram of the proposed mixer.

3.1. Tranconductance Stage

Figure 4 shows the complete circuit diagram of the proposed mixer. Based on the design, the transconductance stage follows the common source configuration and is categorized into different sections, i.e., RF+ and RF− stage, respectively. Both RF+ and RF− stages consist of resistors arranged in a shunt configuration with RF+ stage that consists of input resistors R_1, R_2, and R_3. Similarly, RF− consists of input resistors R_5, R_6, and R_7, respectively. R_1 and R_5 resistors are responsible for the overall input resistance of each stage and can alter the input voltage and hence the overall gain performance. R_4 and R_8 refer to the load resistors opted while keeping the desired drain current I_D. Filters are also

linked to the input end of these stages for impedance matching purposes. Transistor W/L ratio is in such a way that it satisfies the core stage transistor saturation region operating conditions. The input, output impedance, and gain expression of the RF stages can be obtained with the help of the equivalent small signal model. Figure 5 shows the small signal model while ignoring the filter whose analysis is discussed in the filter section. Therefore, for the RF+ stage R_{in} is the internal resistance, R_G refers to the gate resistance, which is the parallel combination of R_1, R_2, and R_3 respectively. Input impedance of RF+ stage

$$Z_{in} = R_G = R_1||R_2||R_3 \tag{5}$$

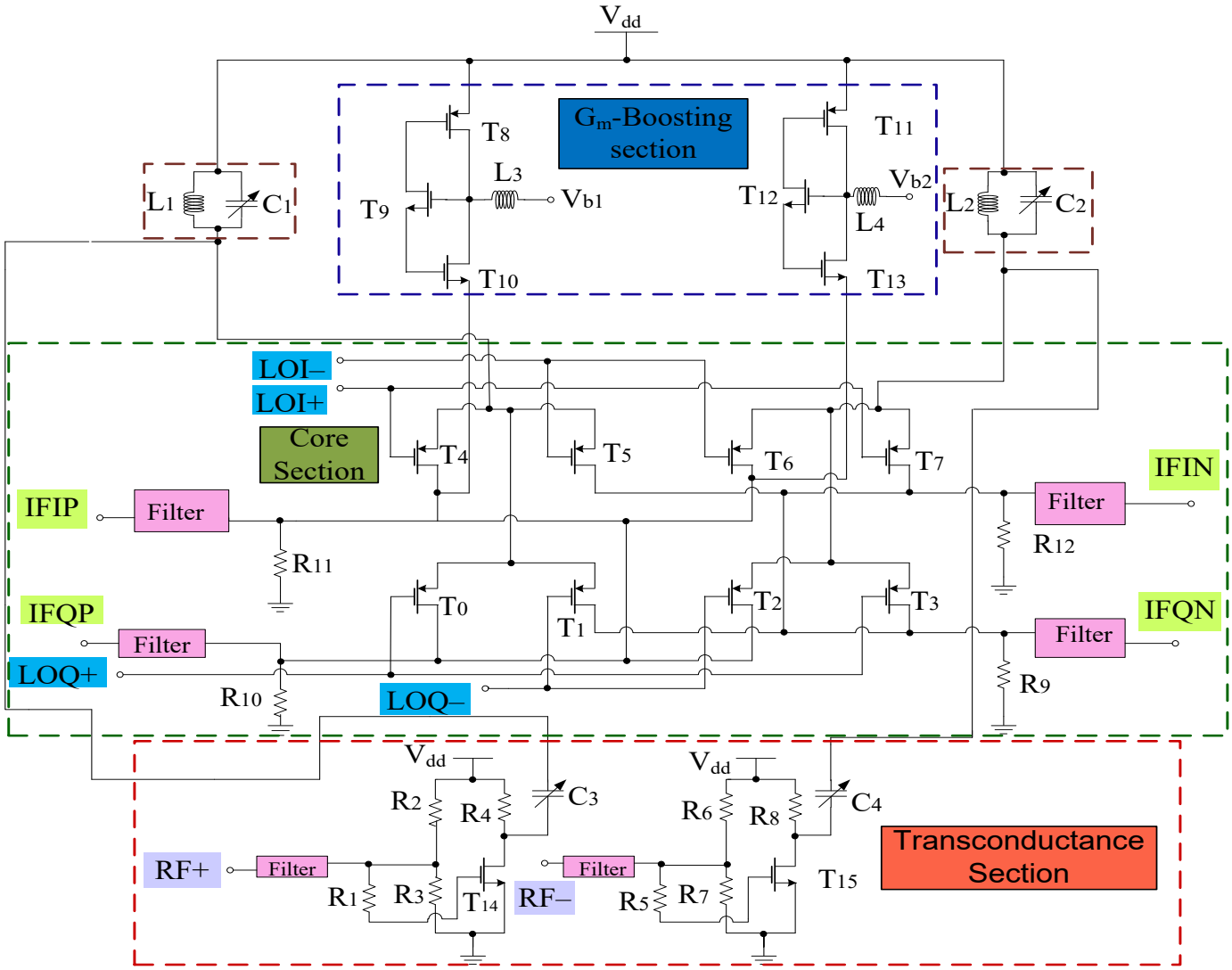

Figure 4. Proposed mixer.

Output impedance of RF+ stage

$$Z_{out} = R_1||\frac{1}{jwC_1} = \frac{R_1}{(R_1)(jwC_1)+1} = \frac{R_1}{(R_1)(sC_1)+1} \tag{6}$$

where $R_1 = r_{ds_{14}} = R_4$, $sC_1 = sC_{db14} + sC_3$. Similarly, the input impedance of RF- stage can be represented as

$$Z_{in} = R_G = R_5||R_6||R_7 \tag{7}$$

Output impedance of RF− stage

$$Z_{\text{out}} = R_2 || \frac{1}{jwC_2} = \frac{R_2}{(R_2)(jwC_2)+1} = \frac{R_1}{(R_2)(sC_2)+1} \tag{8}$$

where $R_2 = r_{\text{ds}_{15}} = R_8$, $sC_2 = sC_{\text{db15}} + sC_4$. Therefore, to obtain the frequency response of the small signal circuit, nodal analysis can be done. The first term should be the node at which the currents are added. If node voltages are multiplied, it refers to all admittances being connected to a node. Next terms will have negative signs which are actually neighboring node voltages and each of these terms uses a multiplication operation on the connecting admittance. The final terms refer to the current sources having a positive sign that is considered only if current sources are flowing out of that node [41]. Based on this, we have

$$V_1(G_{\text{G}} + sC_{\text{gs14}} + sC_{\text{gd14}}) - V_{\text{in}}G_{\text{G}} - V_{\text{out}}sC_{\text{gd14}} = 0 \tag{9}$$

$$V_{\text{out}}(G_1 + sC_1 + sC_{\text{gd14}}) - V_1 sC_{\text{gd14}} + g_{\text{m14}}V_{\text{gs14}} = 0 \tag{10}$$

As $V_1 = V_{\text{gs}}$, then from Equation (10), we get;

$$V_1 = \frac{V_{\text{out}}(G_1 + sC_1 + sC_{\text{gd14}})}{-g_{\text{m14}} + sC_{\text{gd14}}} \tag{11}$$

By substituting (11) in (9), we get;

$$\begin{aligned} V_{\text{out}}[G_1G_{\text{G}} + s[G_1(C_{\text{gs14}} + C_{\text{gd14}}) + G_{\text{G}}(C_{\text{gd14}} + C_1) + g_{\text{m1}}C_{\text{gd14}}] + s^2[(C_{\text{gs14}} + C_{\text{gd14}})(C_1 + C_{\text{gd14}}) \\ -C^2{}_{\text{gd14}}]] = V_{\text{in}}G_{\text{G}}(-g_{\text{m14}} + sC_{\text{gd14}}) \end{aligned} \tag{12}$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-g_{\text{m14}}(1 - s\frac{C_{\text{gd14}}}{g_{\text{m14}}})R_1}{1 + sa + s^2b} \tag{13}$$

$$a = R_{\text{G}}[C_{\text{gs14}} + C_{\text{gd14}}(1 + g_{\text{m14}}R_1)] + R_1(C_{\text{gd14}} + C_1) \tag{14}$$

R_{in} is not used and upon simplification and converting G_{G}, G_1 to R_{G}, R_1, we get;

$$b = R_{\text{G}}R_1(C_{\text{gd14}}C_{\text{gs14}} + C_{\text{gs14}}C_1 + C_{\text{gd14}}C_1) \tag{15}$$

If s = 0, the low frequency gain is obtained as mentioned below:

$$A_{\text{v}} = -g_{\text{m14}}R_1 \tag{16}$$

When the poles are real and

$$w_{\text{p1}} << w_{\text{p2}} \tag{17}$$

The denominator of Equation (13) becomes

$$D(s) = (1 + \frac{s}{w_{\text{p1}}})(1 + \frac{s}{w_{\text{p2}}}) = 1 + \frac{s}{w_{\text{p1}}} + \frac{s^2}{w_{\text{p1}}w_{\text{p2}}} \tag{18}$$

Comparing Equation (13) with Equation (18), we get

$$w_{\text{p1}} = \frac{1}{a} \tag{19}$$

$$w_{\text{p2}} = \frac{1}{bw_{\text{p1}}} \tag{20}$$

Similarly, for RF− stage, the simplified gain can be expressed as mentioned below:

$$A_{\text{v}} = -g_{\text{m15}}R_2 \tag{21}$$

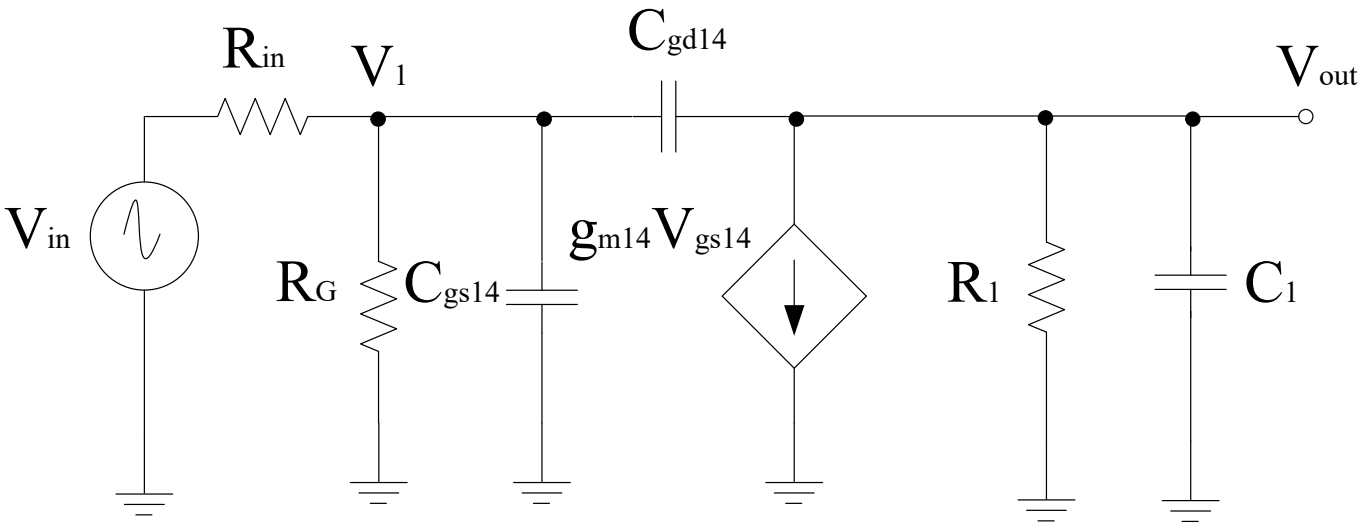

Figure 5. Equivalent small signal model for the RF+ stage.

3.2. Core Stages

It is well known that the image signal is an unwanted input signal to the mixer. Its frequency will be above or below the local oscillator (LO) frequency by an amount which is equal to the IF frequency. Suppose if f_{R1} is the frequency of the desired input signal, then f_{R2} is for its image. Thus, both image and actual input signals mix with the LO and will downconvert to the same frequency. This is problematic for the mixer as both downconverted products interfere with each other as they exit at the IF port together. Thus, by using separate LO stages will overcome this problem and the outputs will be obtained at different IF stages. Based on this phenomenon, two core stages have been developed for the proposed mixer whose outputs will be obtained at different IF stages. The switching stages steered by LO inputs are classified as in-phase (I) and quadrature-phase (Q) stages for image-rejection purposes. Both LO stages contain p-type field effect transistors (FETs) for flicker noise reduction purpose, the transistors T_0–T_3,T_4–T_7 are the part of LOQ and LOI stages, respectively. Alternate transistors in each stage form a differential pair and operate alternatively when LO pulse is applied. Hence, differential outputs will be obtained and the current switch between outputs. The output current is directly proportional to the input current and the signal that is applied at the gate terminals. For determining the output voltage, the current flowing through load resistors is considered along with the load resistors itself. In the design, coupling capacitors are used to couple RF and LO stages. The small signal model for obtaining the output voltage with respect to the current obtained from the RF stage is shown in Figure 6. The model uses Kirchoff's current law (KCL) for analysis. Therefore,

$$i_{\mathrm{IF}} = i_1 + i_2 \tag{22}$$

$$i_{\mathrm{IF}} = \frac{V_{\mathrm{IF}}}{R_{10}} + \frac{V_{\mathrm{IF}}}{R_{11}} \tag{23}$$

$$i_{\mathrm{IF}} = V_{\mathrm{IF}}\left(\frac{1}{R_{10}} + \frac{1}{R_{11}}\right) \tag{24}$$

$$i_{\mathrm{IF}} = V_{\mathrm{IF}}\left(\frac{R_{10} + R_{11}}{R_{10}R_{11}}\right) \tag{25}$$

$$\frac{V_{\mathrm{IF}}}{i_{\mathrm{IF}}} = \frac{R_{10}R_{11}}{R_{10} + R_{11}} \tag{26}$$

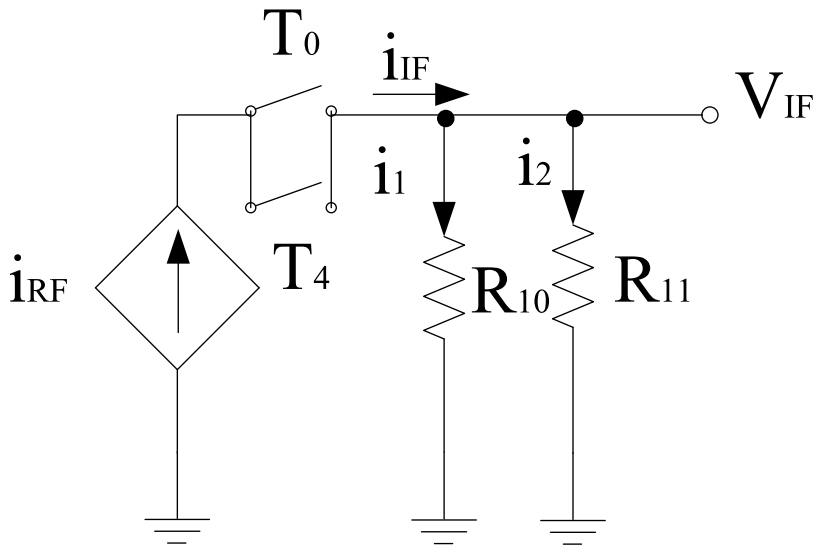

Figure 6. Equivalent small signal model for LO stage.

3.3. Gm-Boosting Section

G_m-boosting circuitry is connected to core stages, which is responsible for the transconductance improvement. Hence, the conversion gain will be enhanced while controlling the power consumption [5]. The proposed design employs peaking inductors at the gate of the transistors. These inductors resonate with the parasitic capacitances and are responsible for avoiding current leakage. The design also employs P-type FETs (T_8 and T_{11}) connected to V_{dd}. However, (T_9–T_{12}) are N-type FETs. The design follows the stacking structure, where transistors T_9 and T_{12} act as an amplifier that improves g_m and overall gain by a factor of $(-A)$. Transistors T_{10} and T_{13} are responsible for delivering the current to the connecting stages. All transistors are operating in the saturation region. The drain current will start flowing in the core stages, the current obtained from this stage will bleed to transconductance stage. Hence, the current will be reused by the transistors T_{14} and T_{15}, respectively. The equivalent circuit for the g_m-boosting stage is shown in Figure 6.

When the transistors T_8, T_{10}, T_{11}, and T_{13} are operating in the saturation region, the current flowing through that stage is given by:

$$i_{GM+} = I_{D8} + I_{D10} - (1 + A)g_{m8}g_{m10}v_{RF} \tag{27}$$

Similarly, for the other section

$$i_{GM-} = I_{D11} + I_{D13} - (1 + A)g_{m11}g_{m13}v_{RF} \tag{28}$$

The LO switches are considered ideal. Therefore, during the positive half of LO pulse, the output current will be positive; during the negative half cycle, the current obtained will be negative. The total current due to the half LOI stage is represented as:

$$i_0 = I_{D4} - I_{D5} = I_{D11} + I_{D13} - (1 + A)g_{m11}g_{m13}v_{RF} \tag{29}$$

This current is transferred to the LOQ stage, then the current within this stage will be due to LOI and the stage itself

$$i_1 = i_0 + I_{D0} - I_{D1} \tag{30}$$

As the coupling capacitors connect the LO stages to the RF stage, the overall boosting can be observed in terms of CG, where the g_m stage is acting in parallel with the load at the IF end. Moreover, g_m-boosting inductor L_3 or L_4 present within the design are responsible for gain improvement. The design analysis is explained as per the positive feedback theory

whose model is shown in Figure 7 . For using this principle, the T_9 signal paths are taken into consideration and output impedance has been ignored for simplicity. Thus, due to presence of L_3 or L_4 a non-zero impedance can be observed at the gate terminal of T_9. The feedforward and feedback paths are considered using parasitic capacitances such as gate-source capacitance (Cgs) and the gate-drain capacitance (Cgd), respectively. Thus, gate-source voltage of T_9 becomes $V_{g,T9}$ while considering new signal paths. The next step is to calculate the open-loop voltage gain as per voltage-voltage feedback configuration. Hence, the voltage at the drain terminal is expressed as

$$V_{nB} = -g_{m9}V_{gs9}Z_{nB} = g_{m9}(V_{nA} - \alpha V_{nA})Z_{nB} \tag{31}$$

where V_{gs9}, g_{m9} and Z_{nB} refers to the gate to source voltage of T_9, transconductance of T_9 and output impedance at node nB that includes the duplicate, respectively. where

$$Z_{nB} = Z'_{nB}||(sL_3 + \frac{1}{sC_{gd9}}) \tag{32}$$

$$Z'_{nB} = \frac{1}{sC_{gd9}}||\frac{1}{sC_{gd8}}||(\frac{1}{g_{mLOI} + g_{mLOQ}}) \tag{33}$$

where Z'_{nB}, α, C_{gd9} and C_{gd8} refer to the output impedance excluding the duplicate, voltage ratio from source to gate, parasitic capacitances for T_8 and T_9, respectively. Thus, the open-loop gain is represented as

$$A_0 = (1 - \alpha)g_{m9}Z_{nB} \tag{34}$$

where

$$\alpha = \frac{sL_3||\frac{1}{sC_{gd9}}||\frac{1}{sC_{gd8}}}{(\frac{1}{sC_{gs9}}||\frac{1}{sC_{gd10}}) + sL_3||\frac{1}{sC_{gd9}}} \tag{35}$$

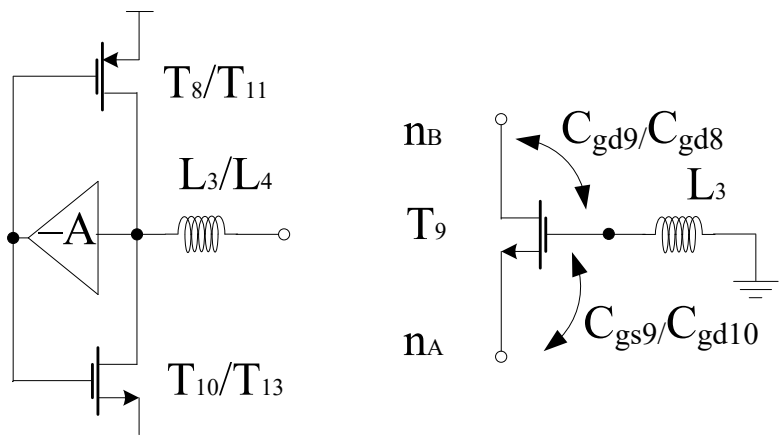

Figure 7. Gm stage model.

Finally, the voltage gain (A_{V0}) without the feedback inductor and the closed-loop voltage gain (A_{Vf}) can be expressed as

$$A_{v0} = \frac{V_{nB}}{V_{nA}}|_{(w/o)L_3} = g_{m9}Z_{nB}|_{(w/o)L_3} \tag{36}$$

$$A_{vf} = \frac{V_{nB}}{V_{nA}}|_{(w)L_3} = \frac{A_0}{1 + \beta A_0} \tag{37}$$

where

$$Z_{nB}|_{(w/o)L_3} = Z'_{nB}||\frac{1}{sC_{gd9}} \tag{38}$$

$$\beta = \frac{sL_3}{(\frac{1}{sC_{gd9}}||\frac{1}{sC_{gd9}}) + sL_3} \tag{39}$$

where β is the feedback factor from drain to gate Hence, it has been verified from the above equations that the gain has been boosted in the presence of the inductor.

3.4. Filter Section

Filters present at the input and output stages are responsible for impedance matching at various frequencies within a band. However, the ones near the core stage prevents signal leakage from the power supply. Various filters have been proposed and the most common techniques are transmission lines, transformer dependent programmable or spiral inductors, and dual-behavior resonator topology [42–45]. However, these filters are limited to some extent and may cover a large area. Therefore, off-chip filters can be used but easy integration is not possible and they are expensive as well. Hence, the most convenient approach is to develop an image-rejected mixer that employs different filters. We propose ninth-order band pass tunable filters for impedance matching purpose which are present at the RF and IF stages of the mixer as shown in Figure 8. Moreover, Figure 9 shows the design of first-order bandpass filter present at the source terminals of the LOI stage transistors at one end and the power supply at the other end to avoid leakage from the power supply.

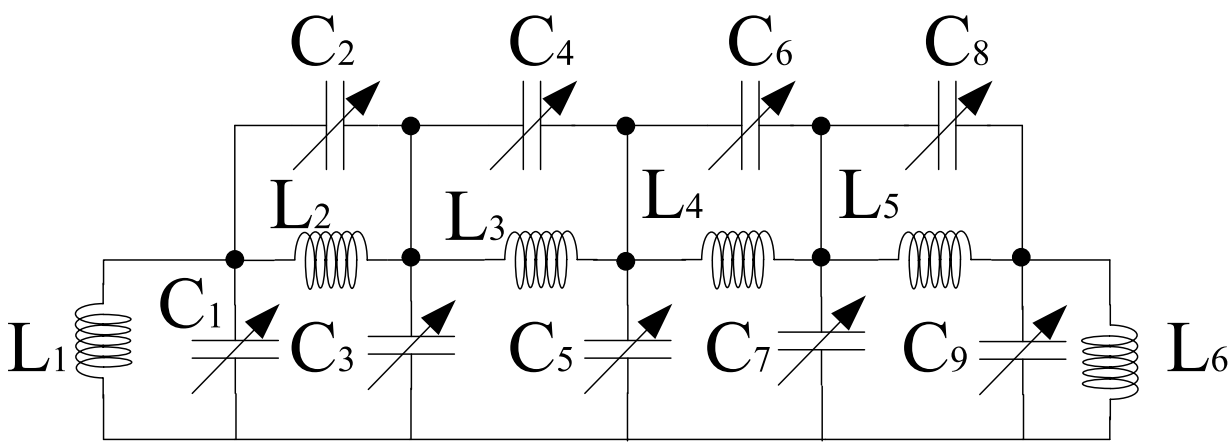

Figure 8. Ninth-order filter.

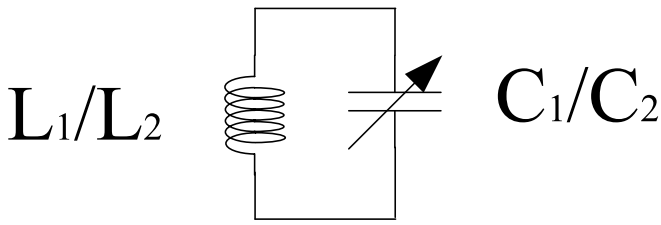

Figure 9. First-order filter.

The input and output impedance of the ninth-order filter section can be expressed as a combination of series and parallel LC sections within the design. The filter order depends on the number of LC pairs. The input impedance, Z_{in} is expressed as:

$$Z_{in} = [[[[[(sL_1||\frac{1}{sC_1} + sL_2||\frac{1}{sC_2})||\frac{1}{sC_3}] + sL_3||\frac{1}{sC_4}]||sC_5] + sL_4||\frac{1}{sC_6}]||\frac{1}{sC_7}] + sL_5||\frac{1}{sC_8}]||sL_6||\frac{1}{sC_9}] \tag{40}$$

$$Z_{in} = (Y + F)||G \tag{41}$$

$$Y = (X + D)||E \tag{42}$$

$$X = (A + B)||C \tag{43}$$

$$A = (sL_1||\frac{1}{sC_1} + sL_2||\frac{1}{sC_2})||\frac{1}{sC_3} \tag{44}$$

$$B = sL_3||\frac{1}{sC_4} = \frac{sL_3}{s^2L_3C_4 + 1} \tag{45}$$

$$C = \frac{1}{sC_5} \tag{46}$$

$$D = sL_4||\frac{1}{sC_6} = \frac{sL_4}{s^2L_4C_6 + 1} \tag{47}$$

$$E = \frac{1}{sC_7} \tag{48}$$

$$F = sL_5||\frac{1}{sC_8} = \frac{sL_5}{s^2L_5C_8 + 1} \tag{49}$$

$$G = sL_6||\frac{1}{sC_9} = \frac{sL_6}{s^2L_6C_9 + 1} \tag{50}$$

For simplicity, different letters have been used to represent the LC combinations. The output impedance, Z_{out} is expressed as:

$$Z_{\text{out}} = sL_6||\frac{1}{sC_9} \tag{51}$$

Similarly, the first-order impedance depends on the parallel combination of L and C.

$$Z_{\text{P}} = Z_{\text{L}}||Z_{\text{C}} = \frac{Z_{\text{L}}Z_{\text{C}}}{Z_{\text{L}} + Z_{\text{C}}} \tag{52}$$

The resonant frequency at which the impedance, Z_{P} will be real can be defined as

$$f_0 = \frac{1}{2\pi\sqrt{L_1C_1}} \tag{53}$$

or

$$\frac{1}{2\pi\sqrt{L_2C_2}} \tag{54}$$

where Z_{P} refers to the parallel circuit impedance. The resonant frequency varies depending on the selected filter circuit within the design.

4. Mixer Design Analysis

Figure 4 shows the complete structure of the designed mixer with g_{m}-boosting, common source configured transconductance stage and Gilbert cell core stage. The first step is to determine the band of operation. The next step is choosing the design topology and filters for successful reconfiguration. The design uses Gilbert topology responsible for improving the overall CG, NF. To further enhance this performance, g_{m}-boosting with inductive peaking is employed. The design is structured to provide good image rejection as well without affecting performance of the design.

4.1. Conversion Gain

Figure 10 shows the complete small signal model used for obtaining the overall CG within the design. The CG, A_{v} is represented by the expression below:

$$A_{\text{v}} = \frac{V_{\text{IF}}(s_{\text{IF}})}{i_{\text{IF}}(s_{\text{IF}})}\frac{i_{\text{IF}}(s_{\text{IF}})}{i_{\text{RF}}(s_{\text{RF}})}\frac{i_{\text{RF}}(s_{\text{RF}})}{V_{\text{gs14}}(s_{\text{RF}})}\frac{V_{\text{gs14}}(s_{\text{RF}})}{V_{\text{in}}(s_{\text{RF}})} \tag{55}$$

where all expressions in Equation (55) are obtained using the small signal model except $i_{IF}(s_{IF})/i_{RF}(s_{RF})$ which can be obtained using Fourier series analysis by approximating LO signal just like a square wave.

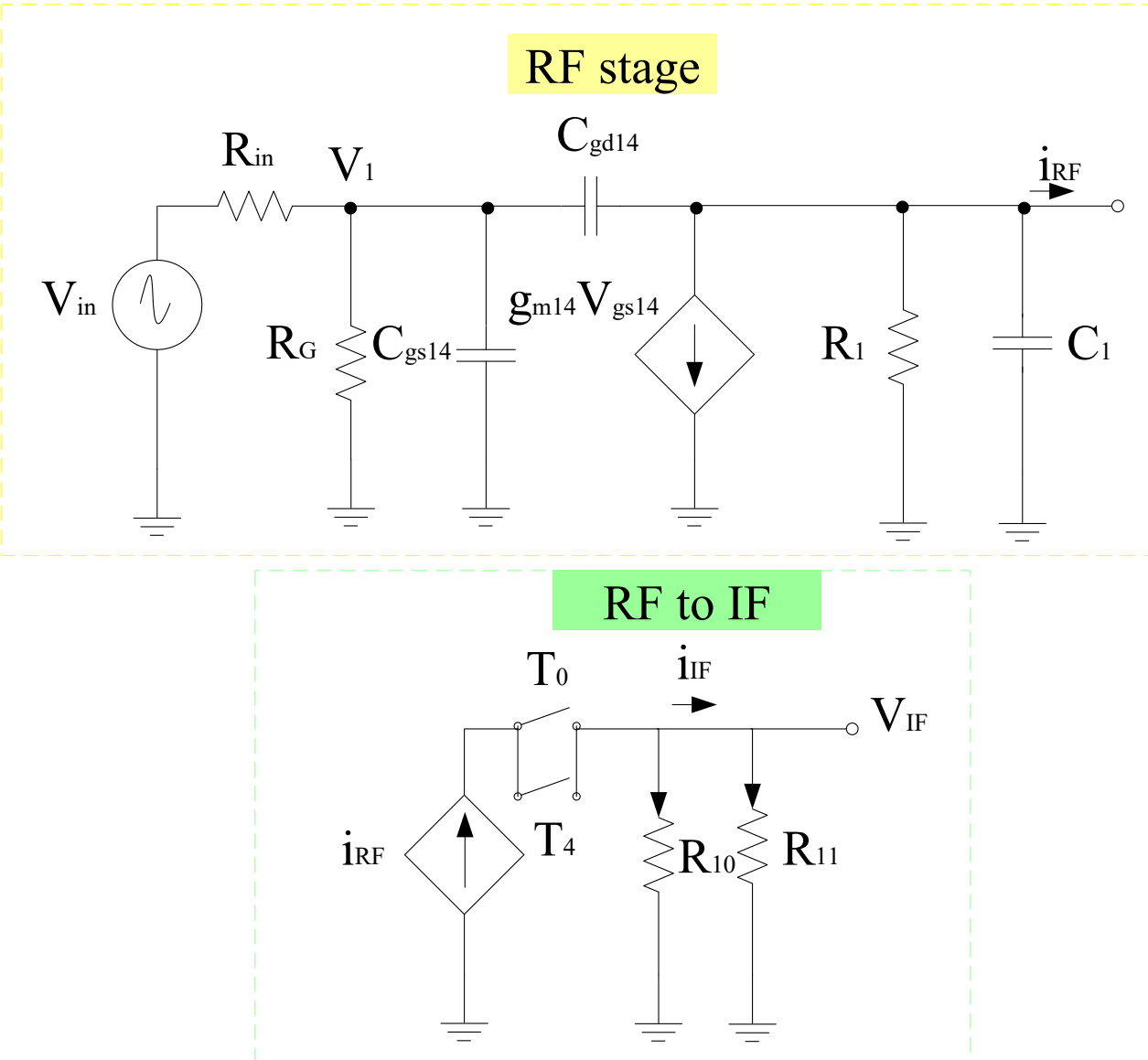

Figure 10. Complete small signal model.

$$\frac{V_{gs14}(s_{RF})}{V_{in}(s_{RF})} = \frac{1}{(1+\frac{R_{in}}{R_G}) + sC_{gs14}R_{in}} \tag{56}$$

$$\frac{V_{IF}(s_{IF})}{i_{IF}(s_{IF})} = \frac{R_{10}R_{11}}{R_{10}+R_{11}} \tag{57}$$

$$\frac{i_{IF}(s_{IF})}{i_{RF}(s_{RF})} = \frac{2}{\pi} \tag{58}$$

For determining $i_{RF}(s_{RF})/V_{gs14}(s_{RF})$ ratio KCL is applied, and we obtain the expression below:

$$V_{gs14}(s_{RF})[s(C_{gs14}+C_{gd14}] = g_{m14}V_{gs14} + i_{RF}(s_{RF})[\frac{1}{R_1} + sC_1] \tag{59}$$

Rearranging the above equation, we get;

$$V_{gs14}(s_{RF})[sC_{gs14} + sC_{gd14} - g_{m14}] = i_{RF}(s_{RF})(\frac{1}{R_1} + sC_1) \tag{60}$$

$$\frac{i_{RF}(s_{RF})}{V_{gs14}(s_{RF})} = \frac{sC_{gs14} + sC_{gd14} - g_{m14}}{\frac{1}{R_1} + sC_1} \tag{61}$$

By substituting (56)–(61) into (55), the overall CG can be obtained.

4.2. Noise Figure

Figure 11 shows the noise model for the proposed circuit. In the circuitry, all passive elements are considered ideal, and the most important noise source is thermal noise, based on which the power spectral density of each stage is obtained. The design consists of resistors and transistors, respectively [41,46].

Equation (62) defines the power spectral density, which is the combination of the power spectral density obtained from all stages present within the design.

$$\overline{V^2{}_n} = \overline{V^2{}_{n,RF}} + \overline{V^2{}_{n,LOI}} + \overline{V^2{}_{n,LOQ}} + \overline{V^2{}_{n,GM}} \tag{62}$$

The power spectral density for all stages is obtained based on the resistors and transistors present within each stage. Thus, the power spectral density for the RF+ stage is expressed as

$$\overline{V^2{}_{n,RF+}} = \overline{V^2{}_{n,R_1}} + \overline{V^2{}_{n,R_2}} + \overline{V^2{}_{n,R_3}} + \overline{V^2{}_{n,R_4}} + \overline{V^2{}_{n,T_{14}}} = \frac{4kT\gamma}{g_{m14}} + 4kTR_3 + 4kTR_2 + 4kTR_4 + 4kTR_1 \tag{63}$$

Likewise, the power spectral density for RF- stage is defined below

$$\overline{V^2{}_{n,RF-}} = \overline{V^2{}_{n,R_5}} + \overline{V^2{}_{n,R_6}} + \overline{V^2{}_{n,R_7}} + \overline{V^2{}_{n,R_8}} + \overline{V^2{}_{n,T_{15}}} = \frac{4kT\gamma}{g_{m15}} + 4kTR_5 + 4kTR_6 + 4kTR_7 + 4kTR_8 \tag{64}$$

Moreover, the power spectral densities for LOI and LOQ stages are expressed as

$$\overline{V^2{}_{n,LOI}} = \overline{V^2{}_{n,T_4}} + \overline{V^2{}_{n,T_5}} + \overline{V^2{}_{n,T_6}} + \overline{V^2{}_{n,T_7}} + \overline{V^2{}_{n,R_{11}}} + \overline{V^2{}_{n,R_{12}}} \tag{65}$$

$$\overline{V^2{}_{n,LOI}} = 4kTR_{11} + 4kTR_{12} + \frac{4kT\gamma}{g_{m4}} + \frac{4kT\gamma}{g_{m5}} + \frac{4kT\gamma}{g_{m6}} + \frac{4kT\gamma}{g_{m7}} \tag{66}$$

$$\overline{V^2{}_{n,LOQ}} = \overline{V^2{}_{n,T_0}} + \overline{V^2{}_{n,T_1}} + \overline{V^2{}_{n,T_2}} + \overline{V^2{}_{n,T_3}} + \overline{V^2{}_{n,R_9}} + \overline{V^2{}_{n,R_{10}}} \tag{67}$$

$$\overline{V^2{}_{n,LOQ}} = 4kTR_9 + 4kTR_{10} + \frac{4kT\gamma}{g_{m0}} + \frac{4kT\gamma}{g_{m1}} + \frac{4kT\gamma}{g_{m2}} + \frac{4kT\gamma}{g_{m3}} \tag{68}$$

$$\overline{V^2{}_{n,GM}} = \overline{V^2{}_{n,GM+}} + \overline{V^2{}_{n,GM-}} \tag{69}$$

Finally, the power spectral densities for GM stages are expressed as

$$\overline{V^2{}_{n,GM+}} = \overline{V^2{}_{n,T_8}} + \overline{V^2{}_{n,T_9}} + \overline{V^2{}_{n,T_{10}}} = \frac{4kT\gamma}{g_{m9}} + \frac{4kT\gamma}{g_{m8}} + \frac{4kT\gamma}{g_{m10}} \tag{70}$$

$$\overline{V^2{}_{n,GM-}} = \overline{V^2{}_{n,T_{11}}} + \overline{V^2{}_{n,T_{12}}} + \overline{V^2{}_{n,T_{13}}} = \frac{4kT\gamma}{g_{m11}} + \frac{4kT\gamma}{g_{m12}} + \frac{4kT\gamma}{g_{m13}} \tag{71}$$

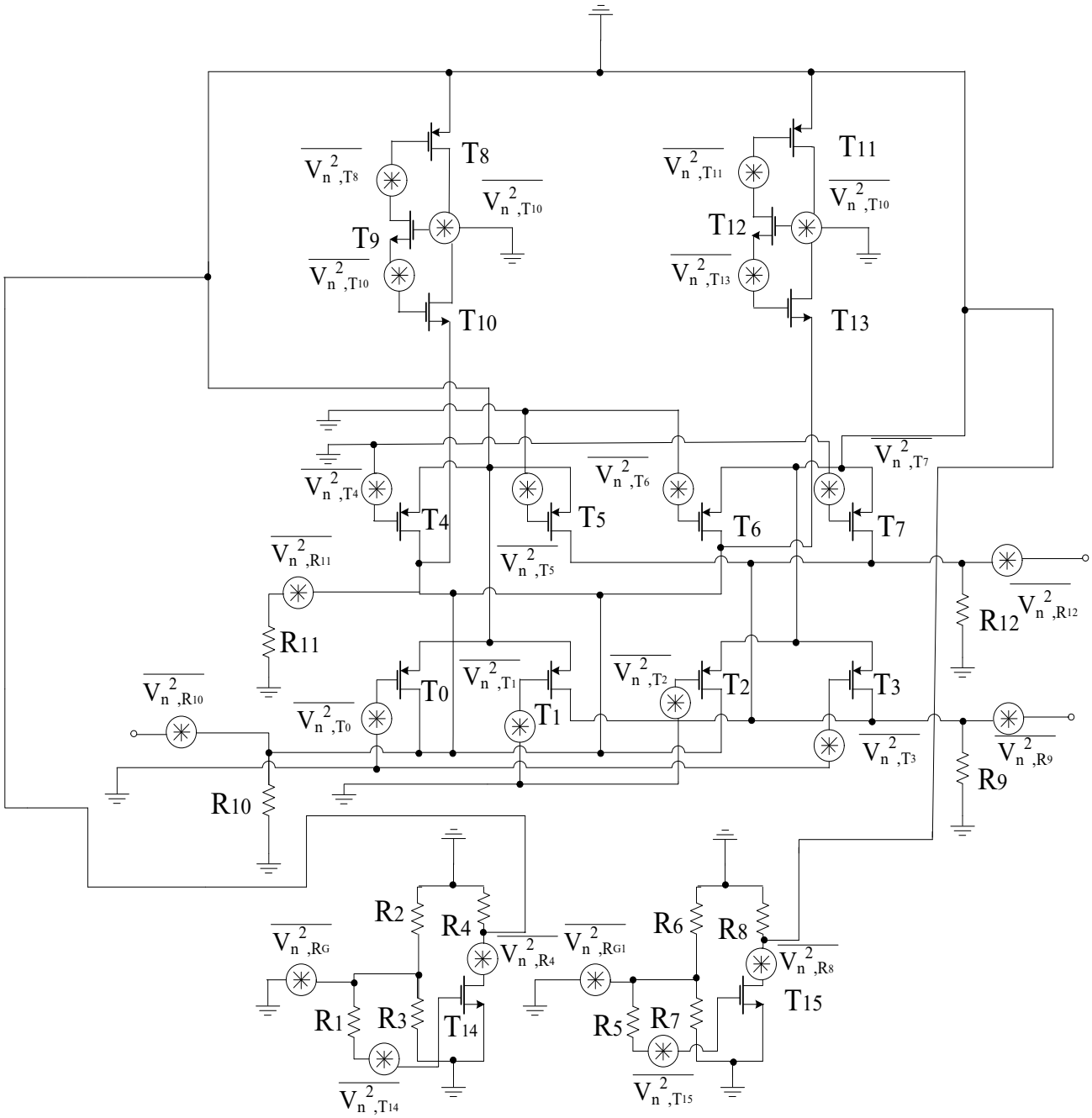

Figure 11. Proposed mixer noise model.

Hence, the noise figure of the proposed mixer is expressed as

$$NF = 1 + \frac{\overline{V^2{}_{\mathrm{n}}}}{A_{\mathrm{v}}{}^2} \tag{72}$$

Moreover, for analyzing the high-frequency noise in the proposed mixer, the thermal noise due to resistors, the thermal noise due to drain, and gate of FETs are considered [47]. The noise contribution due to RF, LOI, LOQ and output stages are considered for the proposed mixer.

Starting with the noise contribution from the RF stage as per Figure 12, the noise signal at the output of the transconductor when multiplied with the switching pair's instantaneous current gain $p_{1(t)}$ results in a current noise , $i_{o14(t)}$ as

$$i_{o14(t)} = n_{o14(t)} p_{1(t)} \tag{73}$$

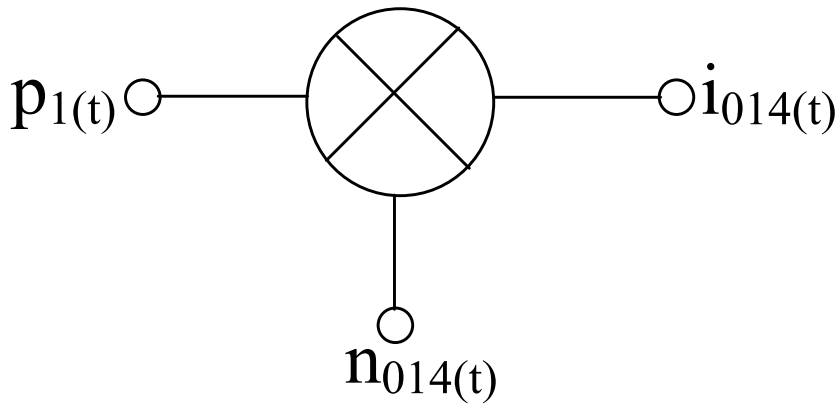

Figure 12. Mixer operation for transconductance noise.

By considering the above process as a time-average wide sense stationary process, the power spectral density of the noise current is expressed as

$$< S^0{}_{n014}(\omega t) > \; = \sum_{n=-\infty}^{\infty} |p_{1,n}|^2 S_{n014}(\omega - n\omega_{LO}) \tag{74}$$

For the overall analysis of power spectral density at the RF stage, both correlated and uncorrelated power spectral density factors have to be considered. Thus, the uncorrelated power spectral density is expressed as

$$S^{(u)}{}_{n014}(\omega)|_{\overline{V^2{}_{n,rg014}}+\overline{V^2{}_{n,RG014}}} = (\overline{V^2{}_{n,rg014}} + \overline{V^2{}_{n,RG014}}) \frac{g^2{}_{m14}}{[\omega(C_{gs14} + C_{gd14})R_{GG014}]^2 + 1} \tag{75}$$

where R_{G014}, r_{g014} refer to the external gate resistance (parallel combination of the resistors) and internal gate resistance.

$$S^{(u)}{}_{n014}(\omega)|_{i_{ng014,u}} \approx \overline{I^2{}_{ng014,u}} \frac{g^2{}_{m14}}{[\omega(C_{gs14} + C_{gd14})R_{GG014}]^2 + 1} \tag{76}$$

Likewise, the correlated power spectral density can be expressed as

$$S^{(c)}{}_{n014}(\omega) = [(k_c + 1)^2 + k^2{}_c |H_T 14(\omega)|^2 - 2k_c(k_c + 1)Re[H_{T14}(\omega)]]\overline{I^2{}_{nd014}} \tag{77}$$

Thus, the overall power spectral density is expressed as

$$S_{n014}(\omega) = S^{(u)}{}_{n014}(\omega) + S^{(c)}{}_{n014}(\omega) = (k_c + 1)^2 A_{s014} \overline{I^2{}_{nd014}} [\frac{1 + \frac{1}{A_{s014}}(\frac{\omega}{\omega_{z014}})^2}{1 + (\frac{\omega}{\omega p014})^2}] \tag{78}$$

Next, the power spectral density due to LO stages is expressed as

$$\begin{aligned} S_{n01}(\omega) + S_{n45}(\omega) = 2[S^{(u)}{}_{n01}(\omega) + S^{(c)}{}_{n01}(\omega) + S^{(u)}{}_{n45}(\omega) + S^{(c)}{}_{n45}(\omega)] = \\ 2[(k_c + 1)^2 As_{01} \overline{I^2{}_{nd01}} [\frac{1 + \frac{1}{A_{s01}(\frac{\omega}{\omega_{z01}}{}^2)}}{1 + (\frac{\omega}{\omega_{p01}}{}^2)}] + (k_c + 1)^2 As_{45} \overline{I^2{}_{nd45}} [\frac{1 + \frac{1}{A_{s45}(\frac{\omega}{\omega_{z45}}{}^2)}}{1 + (\frac{\omega}{\omega_{p45}}{}^2)}]] \end{aligned} \tag{79}$$

Considering the noise present at LO ports are stationary. Thus, time-averaged power spectral density of current noise at the output of the proposed mixer due to LO stages is expressed as

$$< S^0{}_{\mathrm{nLO}}(\omega t) >= 4kT(R_{\mathrm{LOI}} + 2r_{\mathrm{G1}})\overline{G^2}(t) + 4kT(R_{\mathrm{LOQ}} + 2r_{\mathrm{G2}})\overline{G^2}(t) \tag{80}$$

where R_{LOI}, R_{LOQ} refer to equivalent noise resistances and r_{G1}, r_{G2} refer to poly gate resistances. As the image signal does not carry any important information, therefore the single sideband noise figure is considered over the double sideband noise figure as

$$\begin{aligned} NF_{\mathrm{SSB}} &= \frac{\int_0^\infty < S^0{}_{\mathrm{n014}}(\omega,t) > d\omega}{|g_{\mathrm{c}}(\omega)|^2}\frac{1}{4kTR_{\mathrm{G}}} \\ &= \frac{< S^0{}_{\mathrm{n014}}(\omega,t) > + S^0{}_{\mathrm{n01}}(\omega,t) + S^0{}_{\mathrm{n45}}(\omega,t) + < S^0{}_{\mathrm{nLO}}(\omega,t) > + (4kTR_{10} + 4kTR_{11}||G_{\mathrm{M}})}{|g_{\mathrm{c}}(\omega)|^2} \end{aligned} \tag{81}$$

The above expression is defined for a single balanced mixer. Similarly, for the double balanced mixer, NF can also be defined which is almost twice the one obtained for a single balanced mixer.

5. Results and Discussion

The proposed mixer is designed and simulated in the SiGe 8HP process technology. To boost the transconductance within the RF stage, g_{m}-boosting technique has been used in the design, which leads to good CG performance. Figure 13 shows the pre-and post-layout simulation results for the conversion gain performance of the proposed mixer. As depicted in Figure 13, the CGmin and CGmax values are quite similar for both simulations. However, variation can be observed at other frequencies within a band that can be discussed by considering the parasitic effects. The pre-layout CG at the center frequency, 7 GHz is 18.39 dB and after layout, it degrades to 17.7 dB. Due to the parasitic effects of passive components within the circuitry, the CG degrades after the final layout. In particular, the quality factors of the inductors within the circuitry are responsible for the gain performance degradation. Moreover, the parasitic resistance within the inductors can also lower the voltage gain within the circuitry.

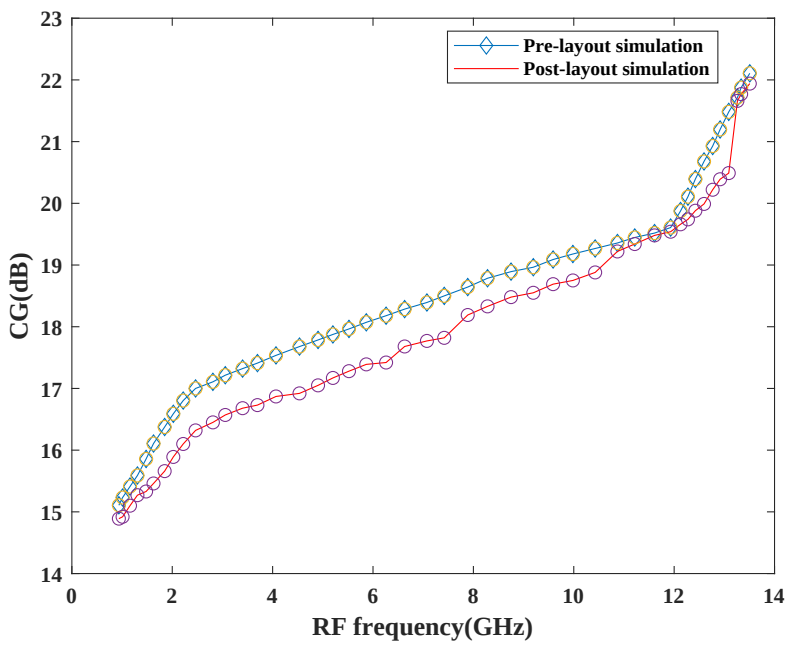

Figure 13. Variation of CG versus frequency.

Figure 14 depicts the NF of the mixer with the variation in frequency. The simulation results show that NF is less than 3 dB before pre-layout simulation and raised by 0.8 dB upon post-layout simulation at the maximum frequency. This performance has also been affected by the parasitic effects of passive components. It also has dependency on the number of resistive components, transistors, and conversion gain performance of the design. This mixer exhibits good NF with a variation of ±1 dB across the entire frequency range.

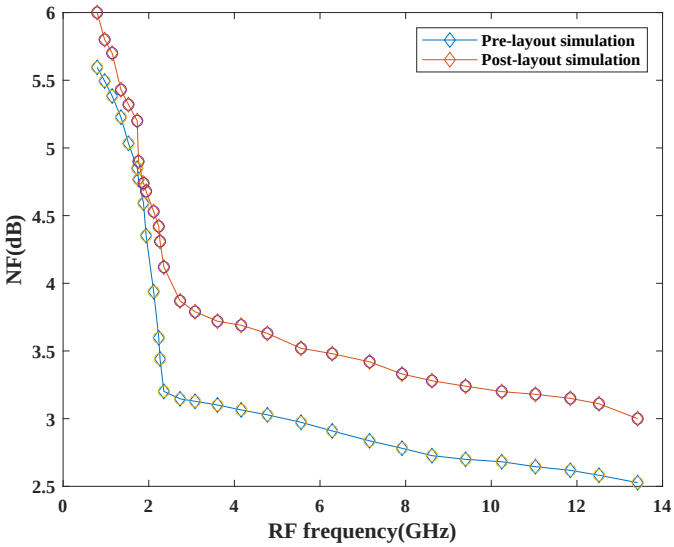

Figure 14. Variation of NF with RF frequency.

The linearity performance of the mixer has been shown in Figures 15 and 16, respectively. The design is considered linear if it shows proportional behavior within the input and output. This behavior can be observed using third-order input intercept points (IP3) and 1dB compression point (CP1). The actual behavior of the mixer is well depicted in terms of pre-and post-layout simulation results. As per the simulation results, it has been observed that the design attained moderate linearity behavior when observed at different frequencies in a band where IP3 is 10 dBm higher than CP1.

The image-rejection ratio is an important aspect while designing the mixer as depicted in Figure 17. When desired and image signals enter the input together, it degrades the overall performance of the circuitry and waste power. Therefore, to overcome this problem, the image signal must be rejected which is done in the proposed design. The mixer attains a good IRR of 28.91 dB at 10.46 GHz upon performing pre- and post-layout simulations. The maximum IRR is around 30 dB, which is within the normal specified IRR range of 20–40 dB.

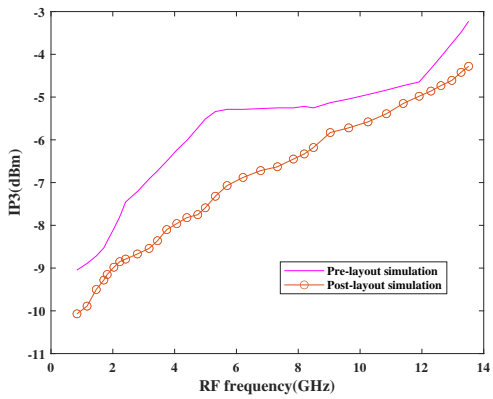

Figure 15. Variation of IP3 with RF frequency.

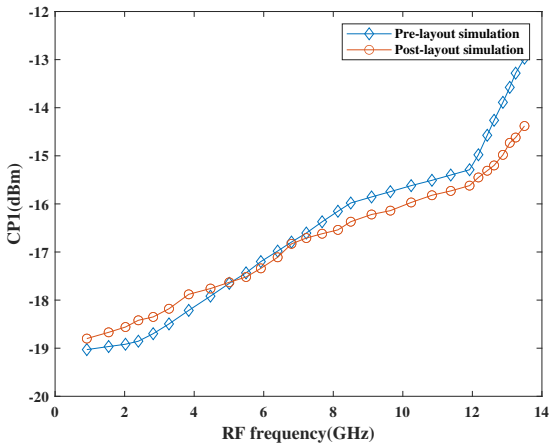

Figure 16. Variation of CP1 with RF frequency.

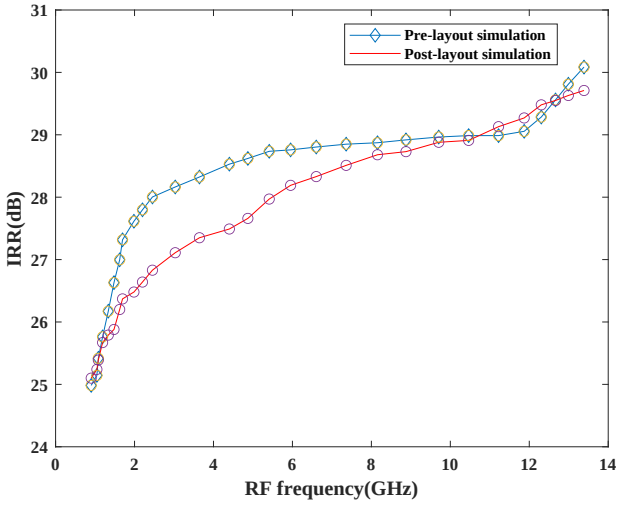

Figure 17. Variation of IRR with RF frequency.

Figure 18 shows the return loss performance with respect to frequency. As per simulation results, the $|S_{11}|$ is below 10 dB at each centered frequency for the entire tuning band, which is as low as −22.42 dB at 11.91 GHz and 13.22 GHz, respectively.

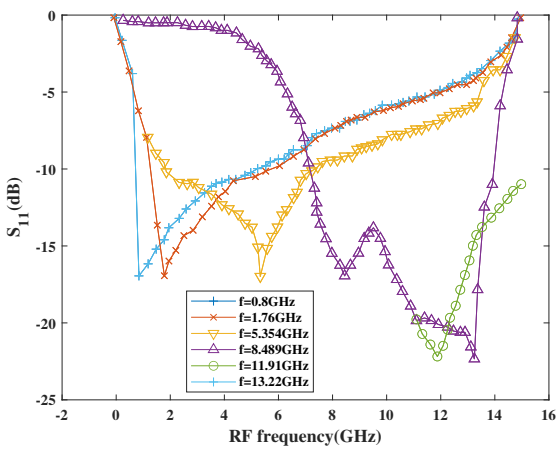

Figure 18. Variation of S_{11} with RF frequency.

Figure 19 shows the layout of the proposed mixer designed in 8 HP process technology covering around 1.98 mm^2 area. The design consists of different sections as discussed in detail in Section 3. The filter section consists of spiral inductors and capacitors. Inductors used provide accurate inductance values and are capable of achieving the maximum Q at a desired operating frequency. Additionally, variable capacitors, i.e., varactors, are used to attain the tuning capacitance.

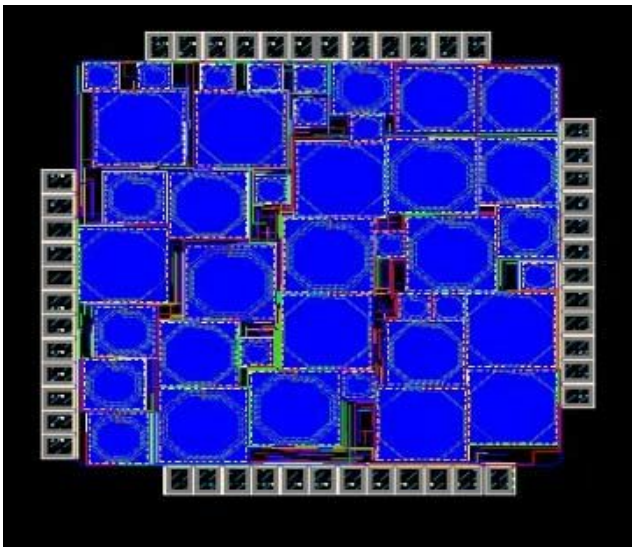

Figure 19. Designed Mixer Layout.

Table 1 summarizes the performance of the proposed mixer and provides a comparison of the circuit with the recent works. As per Table 1, the achievable NF is as less as 2.5 dB and the maximum S_{11} is −20 dB. As CG increases, the IP3 gets degraded due to CG-IP3 trade-off. Moreover, the maximum IRR is 36 dB. The overall area of the proposed mixer is higher than the other reported designs. However, the design attains high performance in terms of CG, NF, IRR and S_{11} simultaneously at the expense of IP3 which is the best among all reported works in the literature.

Table 1. Performance Comparison Summary.

Ref.	Tech.	Area (mm^2)	Freq. (GHz)	S_{21} (dB)	NF (dB)	IRR (dB)	IP_3 (dBm)	S_{11} (dB)
This work	SiGe 8HP	1.8	0.9–13.5	15.1–22.1	2.5–5.6	24.9–30.2	−3.28–9.05	−17.14–22.7
[42]	0.25 um	Nil	0.9	5	8	30	1	−15
[8]	0.065 um	0.19	0.9, 1.8–2.5	9.2–13	13.6–18.3	Nil	≥10.8	Nil
[48]	0.18 um	Nil	2.42–2.48	10.73	Nil	Nil	−7.31	Nil
[49]	0.18 um	Nil	2.4	9.3	7.4	Nil	8	Nil
[26]	0.18 um	Nil	2.4	17	11	Nil	1	Nil
[34]	0.18 um	Nil	2.44	18.6	7.15	Nil	−8.1	Nil
[50]	0.18 um	<1	3.1–10.6	≥10	10	Nil	4	−25
[5]	0.18 um	1.4	5.1	18	13.2	Nil	−5.85	−14.5
[44]	SiGe	0.9	5.1–5.8	14	6.8	36	−5.5	−11
[32]	0.13 um	0.85	7.2–8.4	23.8	4.3	30	−10.5	Nil
[51]	0.18 um	0.11	1.8–2.4	23–26	16–20	Nil	−2	Nil
[52]	0.18 um	0.61	0.5–7.5	5.7	15	Nil	−5.7	Nil
[53]	0.18 um	1.14	3–5	19.8–20.6	7.7–8.7	Nil	>−6	−10.5–15.2
[25]	0.065 um	0.21	1–10.5	10–14.5	6.5–10	Nil	Nil	−20
[54]	0.13 um	0.31	1–5.5	17.5	3.9	Nil	0.84	<−8.8
[55]	0.09 um	0.57	80–110	4.1–11.6	15.8–18.1	Nil	3	−8.7–22
[56]	0.065 um	0.5	17–43	−0.1 ± 1.5	12.4	Nil	3.4	Nil
[57]	0.13 um	0.13	0.87–3.7	13.5–14	2.9–6.5	Nil	−10–13	Nil

6. Design Reliability

Conventional designs were less focused on reliability analysis due to the process and design guide limitations. However, in recent years it is important to consider reliability of the designs due to time, budget, scaling and demanding profile constraints. Relxpert tool developed by Cadence is used to simulate PFET and NFET devices for determining the device degradation performance where performance is evaluated as a function of stress time and biases. Relexpert output can be observed as a "corner in time" that moves towards slow corners in case of simulation from a typical corner. This process helps the designers in analyzing the degradation in circuit behavior during the initial design flow stages [58]. Degradation performance has been evaluated in terms of all performance parameters such as CG, CP1, IP3, NF and IRR ratio. Figure 20 shows the performance of the proposed mixer in terms of IRR and NF with 5 years of aging. From the plots it has been observed that both IRR and NF show degradation; however, more degradation can be observed in NF in comparison to IRR.

Figure 21 shows the performance of the proposed mixer in terms of linearity parameters and it has been found that the linearity will degrade as expected as such variation is observed after post-layout simulation results as well. However, the NF is still $\leq$ 5 dB within the entire band, which is expected for a mixer.

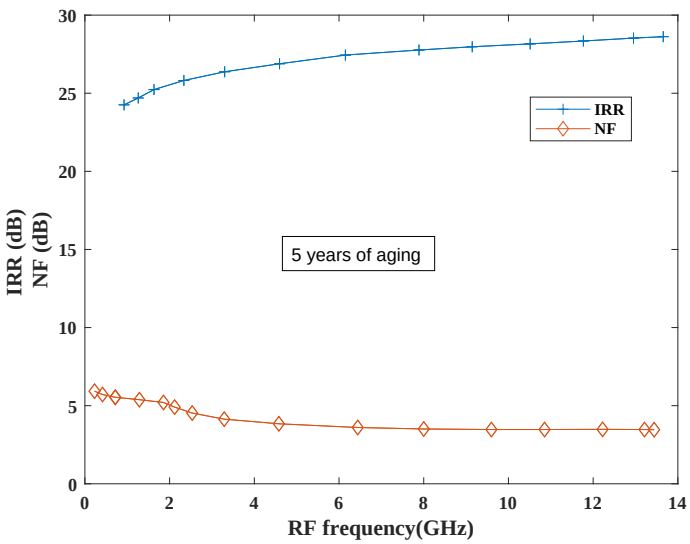

Figure 20. IRR and NF degradation performance.

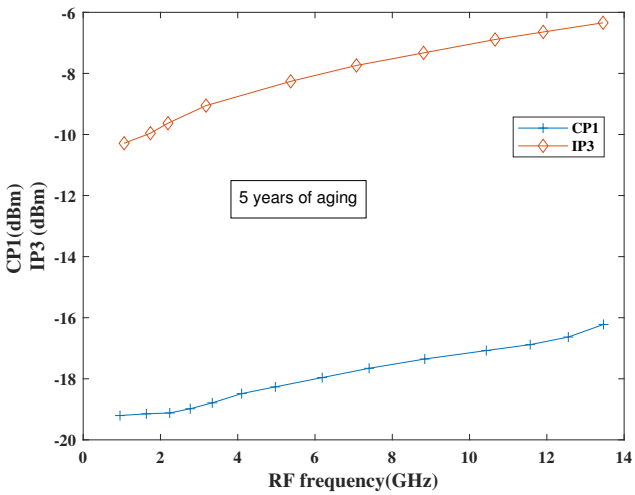

Figure 21. CP1 and IP3 degradation performance.

The behavior of the gain can be observed from Figure 22 which shows the performance of the proposed mixer in terms of gain. Based on the curve, it has been found that the gain degradation is very less as it reaches to 21.5 dB after 5 years and at present it is around 22.1 dB. Thus, the proposed mixer is reliable for future SDR applications.

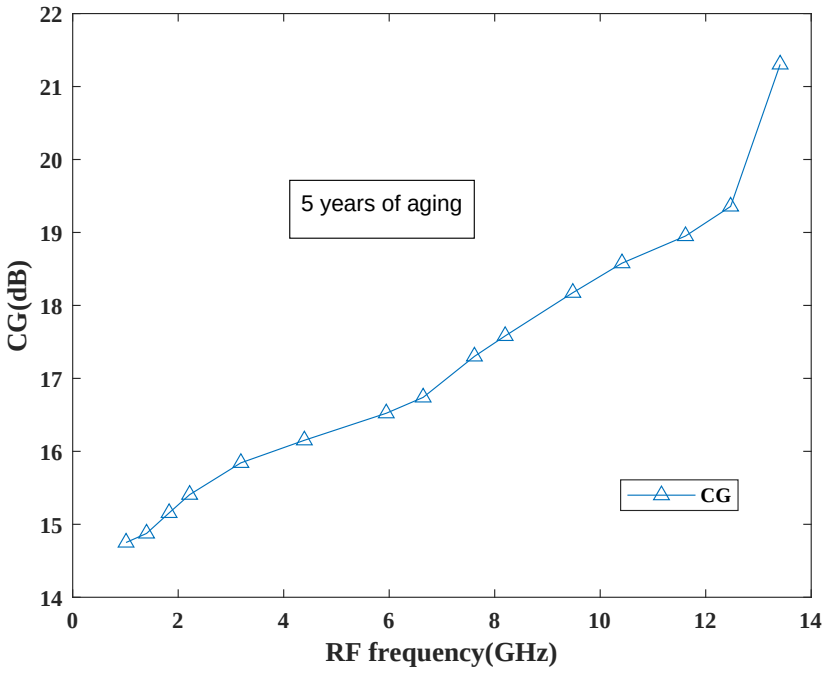

Figure 22. CG degradation performance.

7. Conclusions

In this paper, a novel reconfigurable I/Q Gilbert mixer has been proposed, which is designed and simulated in SiGe 8HP process technology. ninth-order tunable LC filters are embedded at the RF and IF ports for port matching and NF improvement. Moreover, a first-order tunable filter is employed to avoid the leakage through the power supply. The proposed design shows improved transconductance by using G_m-boosting technique. Additionally, the employment of peaking inductors compensates for the gain reduction at high frequencies, while extending the overall bandwidth and hence results in a high gain. Based on the simulation results, with a 1.2 V power supply, the design attains a maximum gain of 22.1 dB. The input return loss is <-10 dB and achieves a minimum of -22.7 dB at 11.9 GHz and 13.22 GHz, respectively. Furthermore, NF ranges between 2.5 and 5.6 dB. The design also shows good IRR within the entire band. Thus, the proposed mixer is compatible enough to meet the future demands of software-defined radios.

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References

1. Brandolini, M.; Rossi, P.; Manstretta, D.; Svelto, F. Toward multistandard mobile terminals - fully integrated receivers requirements and architectures. *IEEE Trans. Microw. Theory Tech.* **2005**, *53*, 1026–1038. [CrossRef]
2. Karanicolas, A.N. A 2.7 V 900 MHz CMOS LNA and mixer. In Proceedings of the 1996 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 10 February 1996; pp. 50–51.
3. Vahidfar, M.B.; Shoaei, O.; Svelto, F. A high dynamic range multi-standard CMOS mixer for GSM, UMTS and IEEE802.11b-g-a applications. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium, Atlanta, GA, USA, 15–17 June 2008; pp. 193–196.
4. Bao, K.; Fan, X.; Li, W.; Wang, Z. A wideband current-commutating passive mixer for multi-standard receivers in a 0.18 um CMOS. *J. Semicond.* **2013**, *34*, 1–3. [CrossRef]
5. Wu, C.; Lin, Y. Design of down-conversion mixer with gm-boosted stage combining low phase noise oscillator. In Proceedings of the International Symposium on Signals, Systems and Electronics, Nanjing, China, 17–20 September 2010; Volume 2, pp. 1–4.
6. Kim, C.; Jang, Y.K.; Yoo, H.J. System Level Design of Multi-standard Receiver Using Reconfigurable RF Block. *J. Semicond. Technol. Sci.* **2004**, *4*, 174–181.
7. Akeela, R.; Dezfouli, B. Software-defined Radios: Architecture, state-of-the-art, and challenges. *Comput. Commun.* **2018**, *128*, 106–125. [CrossRef]
8. Chen, Y.; Yan, N.; Xu, J.; Chen, Q.; Sun, J. Low power, high linearity multi-mode downconversion mixer for SDR. In Proceedings of the 2013 IEEE International Symposium on Circuits and Systems, Beijing, China, 19–23 May 2013; pp. 737–740.
9. Liu, X.; Zhang, X. Multiband Spectrum Access: Great Promises for Future Cognitive Radio Networks. *IEEE Trans. Ind. Inform.* **2020**, *16*, 5379–5388. [CrossRef]
10. Kalathil, D.M.; Jain, R. Spectrum Sharing through Contracts for Cognitive Radios. *IEEE Trans. Mob. Comput.* **2013**, *12*, 1999–2011. [CrossRef]
11. Hattab, G.; Ibnkahla, M. Multiband Spectrum Access: Great Promises for Future Cognitive Radio Networks. *Proc. IEEE* **2014**, *102*, 282–306. [CrossRef]
12. Djoumessi, E.E.; Wu, K. *White Space Communication Technologies*; Cambridge University Press: Cambridge, UK, 2014.
13. Davis, M.D.; Chris. Sampling Mixer for Software Defined Radio Applications using 0.18 um RF CMOS Technology. Undergraduate Thesis, Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, 2013.
14. Asad, B.Z.J. Low-Noise 24 GHz 0.15 um GaAs pHEMT Gilbert Cell Mixer for Intelligent Transportation System Radar Receiver. Master of Applied Science Thesis, Ottawa-Carleton Institute for Electrical and Computer Engineering, Electrical and Computer Engineering, Ottawa, ON, Canada, 2014.
15. Zumbahlen, H. *Linear Circuit Design Handbook*; Newnes/Elsevier: Wilmington, MA, USA, 2008.
16. Siddiqi, A.A. Design Methodology and investigation of GHz range CMOS RF mixers. Master of Engineering Thesis, Carleton University, Ottawa, ON, Canada, 2000.
17. Arun, J.; Ezra, K.; Nithin, M.; Ravi, S. Design and Analysis of Double Balanced Gilbert Cell CMOS Mixer for Heterodyne receivers. *Int. J. Appl. Eng. Res.* **2013**, *8*, 2413–2416.
18. Hu, X. RF CMOS Tunable Gilbert Mixer with Wide Tuning Frequency and Controllable Bandwidth: Design Sythesis and Verification. Master of Science Thesis, Department of Electrical Engineering, Wright State University, Dayton, OH, USA, 2017.
19. Piccinni, G.; Avitabile, G.; Coviello, G.; Talarico, C. Gilbert cell mixer design based on a novel systematic approach for nanoscale technologies. In Proceedings of the 2017 IEEE 18th Wireless and Microwave Technology Conference, Cocoa Beach, FL, USA, 24–25 April 2017; pp. 1–4.
20. Liu, B.; Fan, F.; Zhang, H.; Zeng, C. A wideband down conversion mixer with dual cross-coupled loops for software defined radio. In Proceedings of the 2015 IEEE International Symposium on Circuits and Systems, Lisbon, Portugal, 24–27 May 2015; pp. 990–993.
21. Mehta, S.; Li, X.J.; Aneja, A. A Low Noise Image-Rejection Gilbert Mixer for Software Defined Radios. In Proceedings of the 2020 IEEE International Conference on Electronics, Computing and Communication Technologies, Bangalore, India, 2–4 July 2020; pp. 1–6.
22. Chrisben Gladson, S.; Bhaskar, M. A low power high-performance area efficient RF front-end exploiting body effect for 2.4 GHz IEEE 802.15.4 applications. *AEU-Int. J. Electron. Commun.* **2018**, *96*, 81–92. [CrossRef]
23. Huang, W.H.; Huang, I.Y.; Tseng, Y.S.; Hsieh, C.H.; Wang, C.C. A 19.38dBm OIP3 gm-boosted up-conversion CMOS mixer for 5–6GHz application. *Microelectron. J.* **2017**, *60*, 38–44. [CrossRef]
24. Tomar, V.S.; Bhatia, V. Low Cost and Power Software Defined Radio Using Raspberry Pi for Disaster Effected Regions. *Procedia Comput. Sci.* **2015**, *58*, 401–407. [CrossRef]
25. Hampel, S.K.; Schmitz, O.; Tiebout, M.; Rolfes, I. Inductorless Low-Voltage and Low-Power Wideband Mixer for Multistandard Receivers. *IEEE Trans. Microw. Theory Tech.* **2010**, *58*, 1384–1390. [CrossRef]
26. Vidojkovic, V.; Tang, J.V.D.; Leeuwenburgh, A.; Roermund, A.V. Mixer topology selection for a 1.8–2.5 GHz multi-standard front-end in 0.18 um CMOS. In Proceedings of the 2003 International Symposium on Circuits and Systems, Bangkok, Thailand, 25–28 May 2003; Volume 2, pp. II301–II303.

27. Vahidfar, M.B.; Shoaei, O. A CMOS high IIP2 mixer for multi-standard receivers. In Proceedings of the 2008 IEEE International Symposium on Circuits and Systems, Seattle, WA, USA, 18–21 May 2008; pp. 656–659.
28. Kitsunezuka, M.; Hori, S.; Maeda, T. A Widely-Tunable Reconfigurable CMOS Analog Baseband IC for Software-Defined Radio. In Proceedings of the 2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers, San Francisco, CA, USA, 3–7 February 2008; pp. 66–595.
29. Peng, Y.; Zhang, L.; Fu, J.; Wang, Y. Analysis and Design of a Broadband SiGe HBT Image-Reject Mixer Integrating Quadrature Signal Generator. *IEEE Trans. Microw. Theory Tech.* **2016**, *64*, 688–698. [CrossRef]
30. El-Nozahi, M.; Sanchez-Sinencio, E.; Entesari, K. A CMOS Low-Noise Amplifier With Reconfigurable Input Matching Network. *IEEE Trans. Microw. Theory Tech.* **2009**, *57*, 1054–1062. [CrossRef]
31. Othman, A.; Barrak, R.; Mabrouk, M. A tunable RF filter for multistandard GSM/UMTS/WiFi/LTE receiver. In Proceedings of the 2014 Mediterranean Microwave Symposium, Marrakech, Morocco, 12–14 December 2014; pp. 1–5.
32. Lee, J.; Yun, T. High-gain mixer using cascode current bleeding and gm-boosting techniques. *Microw. Opt. Technol. Lett.* **2016**, *59*, 1–5. [CrossRef]
33. Raja, R.; Venkataramani, B. A Current Injection Folded-Switch Mixer for Direct Conversion Receiver. In Proceedings of the International Conference on Communication Systems, Haryana, India, 18–20 October 2013; B K Birla Institute of Engineering and Technology: Haryana, India, 2013; pp. 36–44.
34. Wei, B.; Dai, Y.; Lu, Y.; Zhang, X.; Liu, H. A Sub 1V High-Gain Low-Noise CMOS Downconversion Folded Mixer for 2.4 GHz ISM Band Applications. In Proceedings of the 2008 International Symposium on Intelligent Information Technology Application Workshops, Shanghai, China, 21–22 December 2008; pp. 689–692.
35. Wei, H.; Hsiao, C. A 1 V bulk-controlled gm-boosted CMOS mixer for LTE-A applications. In Proceedings of the 2013 IEEE 2nd Global Conference on Consumer Electronics, Tokyo, Japan, 1–4 October 2013; pp. 239–242.
36. Vahidfar, M.B.; Shoaei, O.; Hassanzadeh, M.R. CMOS mixer enhanced for multi-standard receivers. In Proceedings of the 2007 50th Midwest Symposium on Circuits and Systems, Montreal, QC, Canada, 5–8 August 2007; pp. 1010–1013.
37. Yan, J.; Lim, K.M.; Gu, J.; Wang, K.; Lim, W.M.; Ma, K.; Yeo, K.S. A double-quadrature down-conversion mixer in 0.18 um SiGe BiCMOS process. In Proceedings of the 2011 International SoC Design Conference, Jeju, Korea, 17–18 November 2011; pp. 246–249.
38. Zhang, C. Reconfigurable RF Front End Components for Multi-Radio Platform Applications. Doctor of Philosophy Thesis, Electrical Engineering, University of Tennessee-Knoxville, Knoxville, TN, USA, 2009.
39. Kim, J.H.; Jang, Y.K.; Yoo, H.J. Design of reconfigurable RF front-end for multi-standard receiver using switchable passive networks. *Analog Integr. Circuits Signal Process.* **2007**, *50*, 81–88. [CrossRef]
40. Hu, B.; Yu, X.; He, L. A Gm-boosted and current peaking wideband merged LNA and mixer. In Proceedings of the 2010 IEEE International Conference on Ultra-Wideband, Nanjing, China, 20–23 September 2010; Volume 1, pp. 1–4.
41. Carusone, T.C.; Johns, D.A.; Martin, K.W. *Analog Integrated Circuit Design*; Wiley: Hoboken, NJ, USA, 2012.
42. Tang, S.l. A new impedance matching method of CMOS mixer with common-source input stage. In Proceedings of the 2005 6th International Conference on ASIC, Shanghai, China, 24–27 October 2005; Volume 1, pp. 512–515.
43. Zhiqun, L.; Zhigong, W.; Wei, C.; Li, Z. Image rejection low noise amplifier for WLAN 802.11a application. In Proceedings of the 2005 Asia-Pacific Microwave Conference Proceedings, Suzhou, China, 4–7 December 2005; Volume 5, pp. 1–4.
44. Long, J.R. A low-voltage 5.1–5.8-GHz image-reject downconverter RF IC. *IEEE J. Solid-State Circuits* **2000**, *35*, 1320–1328. [CrossRef]
45. Heijningen, M.V.; Hoogland, J.A.; Hek, A.P.D.; Vliet, F.E.V. 6–12 GHz double-balanced image-reject mixer MMIC in 0.25 um AlGaN/GaN technology. In Proceedings of the 2014 9th European Microwave Integrated Circuit Conference, Rome, Italy, 6–7 October 2014; pp. 65–68.
46. Razavi, B. *RF Microelectronics*; Pearson Education: Boston, MA, USA, 2012.
47. Heydari, P. An analysis of high-frequency noise in RF active CMOS mixers. *Analog Integr. Circuits Signal Process.* **2006**, *48*, 199–209. [CrossRef]
48. Yadav, V.S.; Chaturvedi, A. 2.4 GHz active CMOS mixer for Bluetooth and Zigbee receiver systems. In Proceedings of the International Conference on Recent Advances and Innovations in Engineering, Jaipur, Rajasthan, India, 9–11 May 2014; pp. 1–6.
49. Chen, J.; Lin, Z. 2.4 GHz High IIP3 and Low-Noise Down-conversion Mixer. In Proceedings of the 2006 IEEE Asia Pacific Conference on Circuits and Systems, Singapore, 4–7 December 2006; pp. 37–40.
50. Motieifar, A.; Pour, Z.A.; Bridges, G.; Shafai, C.; Shafai, L. An ultra wideband mixer with integrated impedance-matching circuit. In Proceedings of the 2006 12th International Symposium on Antenna Technology and Applied Electromagnetics and Canadian Radio Sciences Conference, Montreal, QC, Canada, 17–19 July 2006; pp. 1–4.
51. Tedjini-Bailiche, S.A.; Trabelsi, M.; Slimane, A.; Belaroussi, M.T.; Haddad, F.; Bourdel, S. Ultra low power and high gain switched CMOS gm-boosted current reused mixer for wireless multi-standard applications. *Microelectron. J.* **2014**, *45*, 1575–1582. [CrossRef]
52. Liang, K.; Chang, H.; Chan, Y. A 0.5–7.5 GHz Ultra Low-Voltage Low-Power Mixer Using Bulk-Injection Method by 0.18- um CMOS Technology. *IEEE Microw. Wirel. Comp. Lett.* **2007**, *17*, 531–533. [CrossRef]
53. Wu, C.; Hsieh, H.; Lai, L.; Lu, L. A 3–5 GHz Frequency-Tunable Receiver Frontend for Multiband Applications. *IEEE Microw. Wirel. Comp. Lett.* **2008**, *18*, 638–640. [CrossRef]

54. Ho, S.S.K.; Saavedra, C.E. A CMOS Broadband Low-Noise Mixer With Noise Cancellation. *IEEE Trans. Microw. Theory Tech.* **2010**, *58*, 1126–1132. [CrossRef]
55. Lin, Y.; Lan, K.; Wang, C.; Chi, C.; Lu, S. 6.3 mW 94 GHz CMOS Down-Conversion Mixer With 11.6 dB Gain and 54 dB LO-RF Isolation. *IEEE Microw. Wirel. Comp. Lett.* **2016**, *26*, 604–606. [CrossRef]
56. Zhu, F.; Wang, K.; Wu, K. A Reconfigurable Low-Voltage and Low-Power Millimeter-Wave Dual-Band Mixer in 65-nm CMOS. *IEEE Access* **2019**, *7*, 33359–33368. [CrossRef]
57. Na, D.; Kim, T.W. A 1.2 V, 0.87–3.7 GHz Wideband Low-Noise Mixer Using a Current Mirror for Multiband Application. *IEEE Microw. Wirel. Comp. Lett.* **2012**, *22*, 91–93. [CrossRef]
58. Mahajan, D.; Ruparelia, V. Reliability Simulation and Analysis of Important RF Circuits Using Cadence Relxpert. In Proceedings of the 2018 IEEE International Conference on Electronics, Computing and Communication Technologies, Bangalore, India, 16–17 March 2018; pp. 1–6.