IL NUOVO CIMENTO **43 C** (2020) 74
DOI 10.1393/ncc/i2020-20074-7

COLLOQUIA: IFAE 2019

Development of a particle tracker for space applications

G. GEBBIA, E. RICCI, B. DI RUZZA, R. IUPPA, F. NOZZOLI and P. ZUCCON

University of Trento and Trento Institute for Fundamental Physics and Applications (TIFPA) Trento, Italy

received 8 June 2020

Summary. — Astroparticle physics is often concerned with the observation of phenomena normally shielded by the Earth's atmosphere or taking place in the exosphere, and so demands lightweight detectors suitable for space missions hosted on satellites. In this context particle tracking is concerned with the direct measurement of the trajectory of charged particles. Currently microstrip detectors are the typical technology used in space missions, but pixel detectors, with their higher resolution and a lower material budget, represent an interesting alternative. This paper gives a brief overview of a possible design of a 3-layers particle tracker based on the ALPIDE MAPS chip. With a total of around 100 chips and the stringent constraints imposed by a space mission, the deployment and readout of such detector requires careful optimizations to limit the power consumption but at the same time maintain useful performances. Such task is approached with a custom parallel readout architecture implemented on Field Programmable Gate Arrays (FPGA), with the aim of using a single low-power FPGA chip for the entire detector.

1. – Introduction

Tracking detectors based on pixel technology have inherent advantages in terms of low material budged, with thickness in the order of a hundred micrometers or less, very high angular resolution, better discrimination of concurrent events, and a good degree of modularity which allows to easily tile a custom surface and possibly read-out only a particular area of interest. A low material budget is sometimes critical for the observation of particles in the exosphere, since the particle energy might be relatively small (a few MeV) compared to other HEP experiments.

For the work presented in this paper, the CMOS ALPIDE Monolithic Active Pixels Sensor (MAPS) chip, developed for the ALICE experiment at LHC [1], resulted to be the best candidate available for a spaceborne tracking detector. The sensor is composed by a 1024×512 pixel matrix with binary output and chip-wise programmable threshold covering a $15 \times 30\,\mathrm{mm}^2$ area. The monolithic design, which

places the active area of the sensor and the digital readout circuitry in the same silicon substrate, leads to the very small total sensor thickness of 50 μm. The power consumption of the chip is between 34 and 18.5 mW/cm^2 depending on the particular configuration.

2. – The tracker

The tracker is composed by 150 ALPIDE chips organized in 5 towers of 3 staves, with 10 sensor for each stave. On a stave, the chips are connected in a multi-drop configuration to a single bidirectional data bus. The plots in fig. 1 were generated from a GEANT4 simulation to compare the performances of the pixel-based design with microstrip-based solution for the case of incident electrons.

ALPIDE runs on an external 40 Mhz clock and has two external interfaces: a control line mainly intended for control and triggering but also offering a readout side-channel, and a fast serial line with speeds up to 1.2 Gbps. In this work, in order to limit the power consumption as much as possible, the fast serial line is disabled and the clock is provided to the sensor only when required. Reading from the control line greatly limits the readout speed and so the detector dead time, but considering the small event size and trigger rate ($\leq$4 KHz) expected on a single module this is not a major concern.

Figure 1 illustrates the readout firmware architecture of the tracker, implemented in a single FPGA chip with power consumption of $\sim$1 W; the slow readout speed of the chip is partially compensated reading multiple staves in parallel, a task executed by a readout state machine (labelled "CTRL"). Each tower has its dedicated trigger signal, so

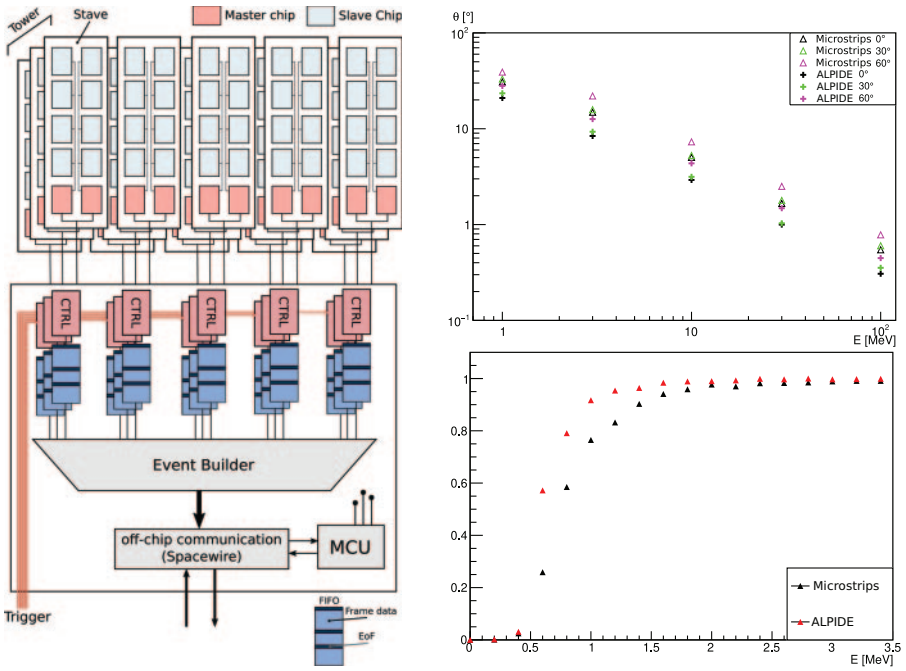

Fig. 1. – (Left) Tracker and readout system architecture. (Right) Simulation of energy threshold and angular resolution for incident electrons.

only the staves in a region of interest need to be activated and read. The data are stored in dedicated FIFO buffers and are then read and packaged by an event builder module before being transmitted off-chip. A Microcontroller Unit (MCU) is also implemented in the FPGA for calibration procedures and general housekeeping.

REFERENCES

[1] ALICE Collaboration (Šuljić M.), *Nuovo Cimento C*, **41** (2018) 91.