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Characterization of the Outer Barrel Modules for the upgrade of the ALICE Inner Tracking System

B. DI RUZZA(1)(2)(*)

(1) *INFN, Sezione di Padova - Padova, Italy*
(2) *Dipartimento di Fisica e Astronomia, Università di Padova - Padova, Italy*

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Summary. — The Inner Tracking System (ITS) Upgrade of the ALICE detector at CERN is one of the major upgrades that will take place in 2019–2020. This paper regards the construction procedure and the electrical characterization of the Outer Barrel Module. This is the building element of the four outer layers of the ITS and it is realized assembling together fourteen Monolithic Active Silicon Pixel Sensors with a space precision of the order of few microns. The challenge of the production chain, the characterization test procedure and the results of the first produced prototypes will be shown.

1. – Introduction

ALICE (A Large Ion Collider Experiment [1]) is a CERN experiment, located in one of the interaction point of the LHC collider, designed to address the physics of heavy ions and strongly interacting matter, using nucleus-nucleus (A-A) collisions. For these studies baseline proton-proton (p-p) collision analyses are also required as baseline reference, and proton-nucleus (p-A) to discriminate between initial and final state effect. Despite the success already reached in achieving these physics goals, there are several measurements still to be finalized, like high precision measurements of rare probes (D mesons, Lambda baryons and B mesons decays) over a broad range of transverse momenta. The achievement of these goals requires a wide upgrade plan of the ALICE experiment combined with a significant increase of luminosity of the LHC collider. This upgrade plan was already approved and will enhance the ALICE physics capabilities enormously allowing the achievement of these fundamental measurements. The ALICE Inner Tracking System (ITS) detector will play a key role in these studies, and for this detector a wide upgrade program was designed and already started. The plan is to replace completely the present ITS detector with a new one in 2019–2020 during the Long Shutdown 2 (LS2) using a innovative Monolithic Active Pixel silicon Sensor (MAPS), called ALPIDE. The main features of the new ITS are a low material budget, high granularity and low power consumption. All these peculiar capabilities will allow the full reconstruction of rare heavy

(*) E-mail: benedetto.diruzza@gmail.com

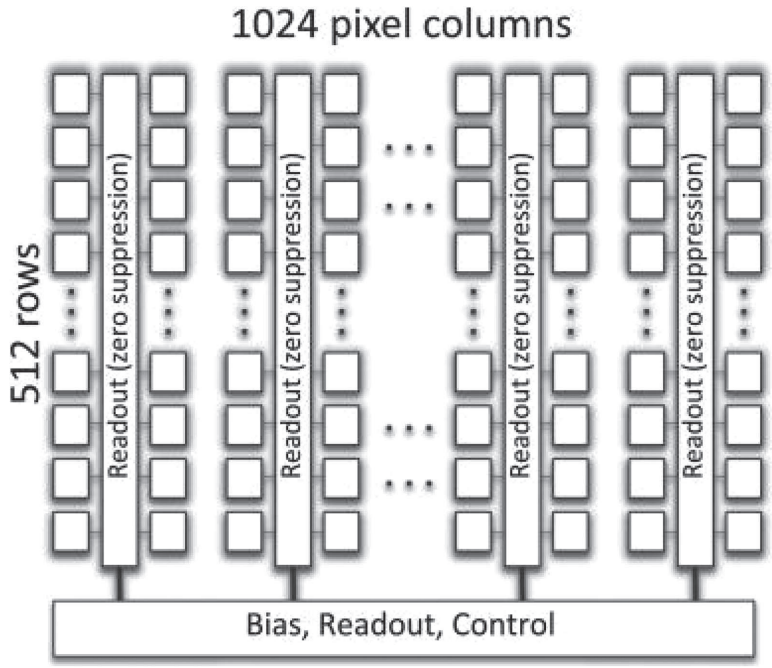

Fig. 1. – Architecture of the ALPIDE chip.

flavour decays and the achievement of the planned physics goals. In this contribution there is an overview of the whole ITS upgrade project focusing mainly in the construction and functional characterization procedure of one the basic building block of the new detector, namely the Outer Barrel Hybrid module (OB-HIC).

2. – The ALPIDE chip

The new ALICE ITS detector will be realized using a innovative MAPS chip sensor suitably designed for this upgrade. The Pixel Chip of the upgraded ALICE ITS will be produced in the TowerJazz 180 nm CMOS imaging process using a of a high-resistive epitaxial layer on a p-substrate. Being a quadruple-well process, it offers a deep PWELL, which can be used to shield the NWELL of PMOS transistors. This makes the use of full CMOS circuitry in the pixel area possible without the drawback of parasitic charge collection by those NWELLs. The application of a moderate negative voltage (around $-3\,\mathrm{V}$) to the substrate can be used to increase the depletion zone around the collection diode improving in this way both the charge collection and the signal-to-noise ratio by decreasing the pixel capacitance. The interconnections between transistor and diodes will be realized using six metal layers allowing the integration in the single pixel of a large number of control functions. Data can be transmitted using two different readout ports. A 1.2 Gb/s serial output port with differential signaling is intended to be the largest capacity data readout interface. A bidirectional parallel data port with single-ended signaling is also present, with a capacity of 320 Mb/s. The ALPIDE chip measures 15 mm by 30 mm and includes a matrix of 512×1024 pixel cells, each one measuring roughly $30 \times 30\,\mu\mathrm{m}^2$. Analog biasing, control, readout and interfacing functionalities are implemented in a peripheral region of $1.2 \times 30\,\mathrm{mm}^2$ (see fig. 1).

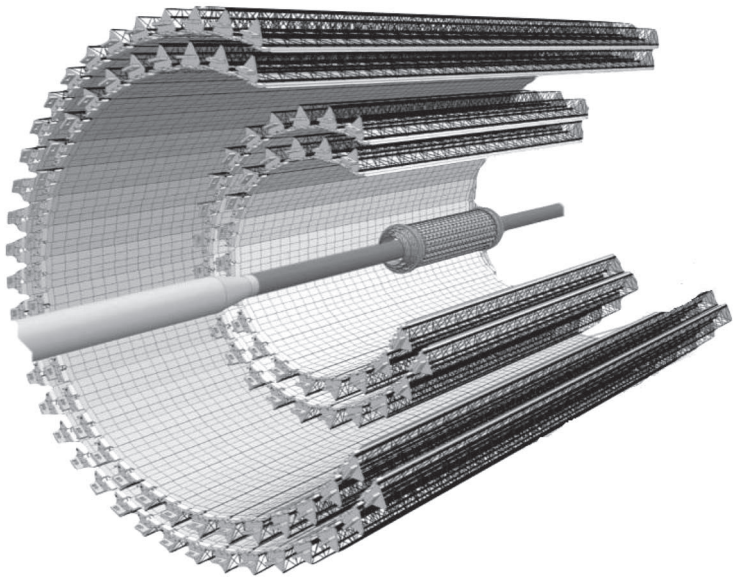

Fig. 2. – The 7-layers ITS structure (3 inner layers, 2 middle layers, 2 outer layers).

TABLE I. – *ITS coverage in eta, R and Z coordinates.*

Eta Coverage	$\|\eta\| \leq 1.22$		
R Coverage	22 mm–400 mm		
Z Coverage	Inner Layer	Middle Layer	Outer Layer
	290 mm	900 mm	1500 mm

3. – The new ALICE ITS structure

The new ALICE ITS will have a cylindrical structure organized in seven different layers, as described in fig. 2, and a coverage described in table I. The R coordinate is the radial distance from the beam-line, the Z coverage is the length along the beam-line with the interaction point as center. The seven ITS layers will be organized in modules or HIC (read-out units) and staves (mechanical units). The three innermost layers will be composed by staves, each one is composed by one Inner Barrel Module (IB-HIC). Each IB-HIC will be organized in a row of nine chips. The two outer (middle) layers will be composed by staves built by two rows of seven (four) Outer Barrel Modules (OB-HIC). Each OB-HIC will be composed by two rows of seven chip. In table I there is a summary of the elements in each layers. Each module (both inner and outer) will be realized gluing the chips on expressly designed Flexible Printed Circuit (FPC) containing the data and control buses. Chips pad will be wire bonded to the FPC bus. In the three inner layers, where a high hit density is expected, all the chips in every module will have the same role, while in the four outer layers, where the hit density will be lower, the architecture will be different. For the OB-HIC, only a chip in every row, the master, will collect the data from the other six slaves, sending the output to the external DAQ using a unidirectional High Speed Data (HSD) serial line.

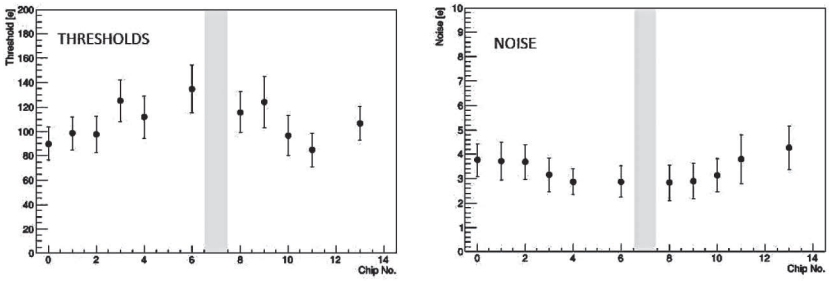

Fig. 3. – Prototype Outer Barrel Module chip average threshold and noise measurements.

TABLE II. – *Number of elements in different layers.*

Layer #	0	1	2	3	4	5	6
Chips	108	144	180	2688	3360	8232	9408
Modules	(IB)12	(IB)16	(IB)20	(OB)192	(OB)240	(OB)588	(OB)672
Staves	(IL)12	(IL)16	(IL)20	(ML)24	(ML)30	(OL)42	(OL)48

4. – The prototype module construction and test

The outer (inner) module construction will be realized in a four-step operation: at first fourteen (nine) ALPIDE chips are aligned with a expressly designed automatic machine called Alicia, with a space precision below 5 μm. After that glue balls are deposited on the corresponding FPC trough a laser drilled mask and then the FPC is glued on the aligned chips.

After the glue polymerization, the interconnections between the FPC bus and the chip pad is performed with a vertical wire bonding connection. For redundancy protection every FPC ring is bonded to the corresponding chip pad with at least 2 wires. Between May and July 2016 a first series of few OB-HIC was realized and tested in order to define the module assembling procedure. After the operation of gluing and bonding the modules were tested using a setup expressly realized. The test set-up is based on a high speed communication board called MOSAIC that, using a specific software, acts as DAQ interface with the modules. The ALPIDE chip is designed with a special feature that allows a charge self injection in the collection diode using a capacitor located inside the pixel. Using this feature it is possible to test all the collection electronic chain without the irradiation with charged particles. At the end of the module assembling procedure this function is used to test the inter-chip connections and to perform threshold scan and dynamic noise measurements on every single pixel of the whole module. In fig. 3 the result of the chip average threshold scan and noise measurements realized in one prototype module is shown.

5. – Conclusion

The ALICE ITS upgrade program requires the mass production of ∼1700 Outer Barrel Modules, spares included. A procedure was defined in order to perform a fast functional characterization of the produced modules. This procedure will be implemented in the production of the next final version of the modules.

REFERENCES

[1] ALICE COLLABORATION, *JINST*, **3** (2008) S08002.