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MATISSE: A Low power front-end electronics for MAPS characterization

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In recent years Monolithic Active Pixel Sensors are becoming increasingly attractive for High Energy Physics experiments. Several R&D activities are ongoing worldwide to improve the performance of conventional monolithic pixels in terms of speed and radiation tolerance. These improvements come both from the optimization of the substrate material and the design of the front-end electronics.

In the framework of an R&D project on CMOS monolithic sensors, a versatile readout electronics has been developed. The purpose is to have a flexible system to test different sensor geometries and substrates, allowing a detailed analog characterization and the study of effects that arise in complex mixed signal chips such as digital induced noise.

The ASIC prototype, MATISSE, has been fabricated in 0.11 μm CMOS technology with a die area of 2×2 mm^2 and a low voltage operation of 1.2 V. Hereafter, the front-end electronics are described and the first results from the characterization are reported.

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1. Introduction

Silicon pixel sensors have been successfully used in many High Energy Physics experiments (HEP). Thanks to very deep sub-micron technologies it is now possible to integrate in a small area sophisticated front-end electronics to meet the challenging requirements of future particle detectors. In applications where fast readout and very high radiation tolerant are primary concerns, hybrid pixels are still the only viable solution. The much lower cost offered by monolithic CMOS sensor, is however motivating several R&D activities to overcome the main limitation of conventional MAPS with the goal of achieving performance comparable with those of an hybrid implementations [1], [2].

The key to improve speed and radiation hardness of monolithic detectors is to have a charge collection dominated by drift. In this context, we are exploring different sensor designs and substrates materials with the aim of achieving a depletion depth of at least 30 μm. To allow a detailed characterization of the investigated options, a flexible front-end readout system has been developed. The chip architecture is described in section 2 and the test results are presented in section 3.

2. Chip architecture

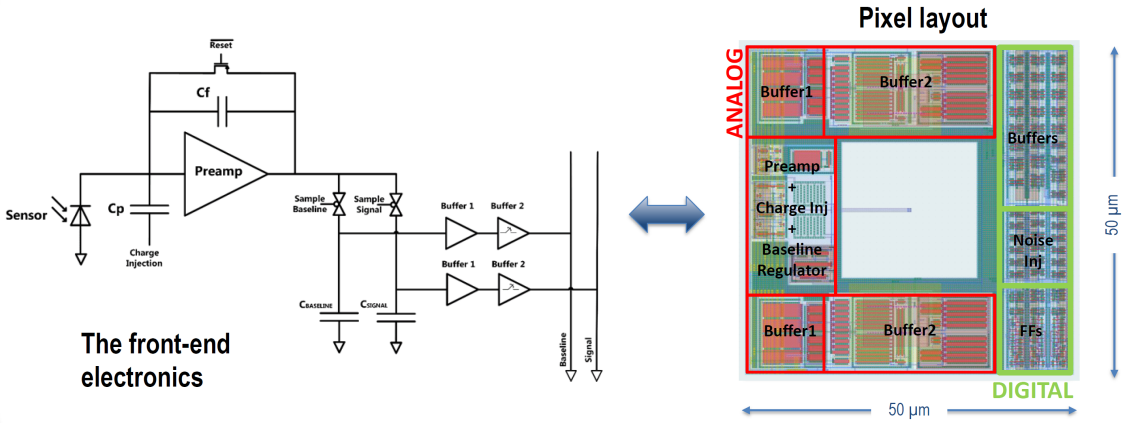

Figure 1: The analog in-pixel electronics and the layout of the pixel unit

MATISSE (Monolithic AcTIve pixel SenSor Electronics) is an ASIC prototype developed in 0.11 μm CMOS technology in an area of 2×2 mm^2. The test chip consists of 24×24 pixel matrix divided in 4 identical groups and an End of Column logic (EoC). Each group is arranged into 6 columns of 24 pixels. The monolithic pixel unit fits a total area of 50×50 μm^2 shared between a sensor of 20×20 μm^2 and the in-pixel electronics as depicted in Fig.1. The sensors differ from each other for what concern the geometry of the collection electrode, the substrate type and doping. The readout electronics is common to the different sensor flavors and integrates both analog and digital circuits in proximity of the sensitive node.

The in-pixel analog readout (Fig.1) is based on a Charge Sensitive Amplifier (CSA), two local memories and four buffers used for data transmission. The CSA is based on a telescopic cascode amplifier with a feedback capacitor which fixes the conversion gain to 130 mV/fC. The two

memories are implemented with MIM capacitors to optimize the pixel size. Moreover, in the proposed design, each memory is readout by a chain formed by a low power buffer and two rail-to-rail switched op-amps which are used to send the analogue data off-chip. The whole chain has been optimized to maximize the output dynamic range up to 500 mV maintaining a low power consumption.

The digital in-pixel logic contains three programmable flip-flops used for the readout operation and to implement features like test pulse generation and pixel masking. Moreover, the logic allows the baseline regulation which, together with the buffers wide dynamic range, makes the readout suitable for sensors of both polarities with signals in excess of 24 ke^-. The digital logic for the readout operation is implemented in the EoC. A chain of inverters driven by a dedicated signal allows to inject digital noise to study the sensitivity of the sensor and the very front-end in a mixed signal environment.

MATISSE supports snapshot shutter operation [4] and thus the integration time starts and ends at the same time for all the pixels of the matrix. The two signals, one at the beginning and one at the end of the integration time, are stored in the two pixel memory elements. In such a way, when some charge is collected in the sensor, it will be identified by the difference between the two stored values. For this reason both signals are sent off-chip. The readout of each sector is independently managed by the EoC logic which sequentially addresses every pixel of the sector. In this way, the matrix can be read out in less than 40 μs, ensuring a maximum measured voltage drop of 0.7 mV, when a clock of 5 MHz is used. The design supports Correlated Double Sampling (CDS) to subtract offsets in common between baseline and signal and to suppress the switching noise.

3. Test results

MATISSE chips were received from the foundry in April 2017 and the first results are reported here. For the characterization two dedicated PCBs has been developed: a small carrier board used to connect the ASIC to the system through wire bonding and a main board where almost all the discrete electronics is placed. Since the carrier board and main board can be easily connected, the hardware is very flexible allowing to test several chips with the same main board. The data acquisition system used for the tests is based on a software written in C++ and ROOT, a commercial FPGA and a full custom analog board with 5 channels, each with a 100 MS/s, 14 bit ADC [3].

The first electrical tests were dedicated to verify the expected power consumption of 6 μW/ch, 3.6 mW for the full chip during the integration period and 6.4 mW during the data transmission. The measurements confirm these values and suggest that all the blocks are working properly.

To study the performance of the pixel some measurements have been carry out by tuning the baseline. This operation can be done by using a voltage reference set on the main board through a dedicated trimmer and sending the proper digital signals to the ASIC. Fig. 2 shows how the baseline behaves for different voltages references. With the minimum voltage reference ($\approx$ 20 mV) the baseline reaches its maximum (700 mV) and then for higher voltage references it decreases with a linear response down to $\approx$ 320 mV. The measurement shows that the expected operation range for the analog in-pixel electronics is covered with a good linearity.

As a first check of the combined sensor and electronics performance, a measurement with a ^{55}Fe radioactive source has been done. In this measurement the integration time and the baseline

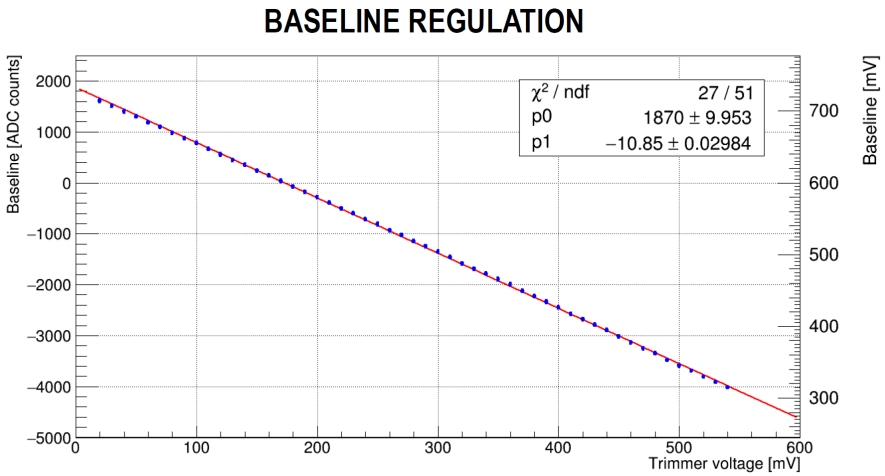

Figure 2: Regulation of the baseline for voltage references in the range of 20 mV and 550 mV

have been set to 5 μs and 450 mV respectively. Fig. 3 shows the reconstruction spectrum where the main peak at 5.9 keV is clearly seen. From this measurement it follows that the analog gain of the full readout chain is ≈117 mV/fC. This value is in fair agreement with the one expected from computer simulations (≈130 mV/fC).

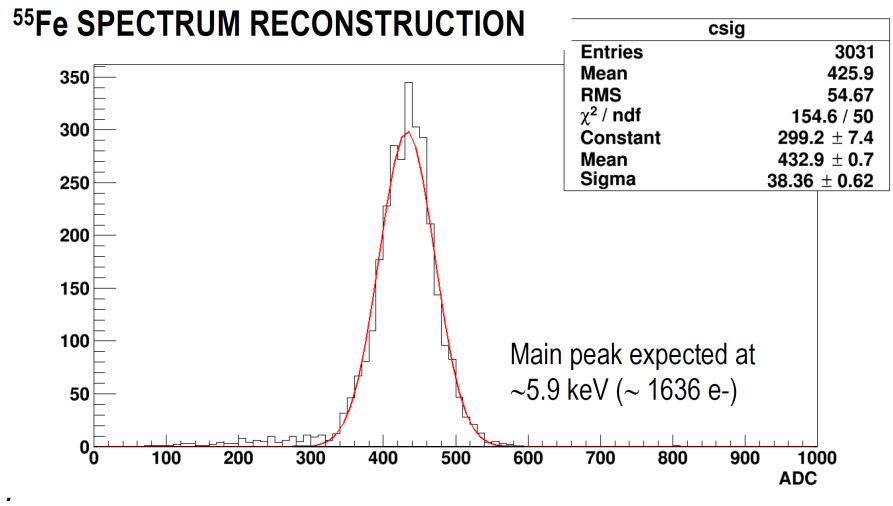

Figure 3: ^{55}Fe spectrum reconstruction

MATISSE has been designed to keep the noise at the preamplifier output below 1 mV rms. The full chain has been analyzed to estimate the noise of each block. In Table 1 the contributions from the DAQ box, main board, carrier board and finally from the ASIC itself are summarized. The noise up to the carrier board is very low (110 μV) therefore, this confirms that the DAQ system is adequate for noise measurements.

Fig. 4 shows the noise of all pixels in a matrix. The mean noise value is 1.1 mV which corresponds to 58 e^- rms.

DEVICE	NOISE [ADC]	NOISE [mV]
DAQ box	0.2	0.02
DAQ + Main Board	0.2	0.02
DAQ + Main Board + Carrier board	1.6	0.11
DAQ + Main Board + Carrier board + ASIC	15	1.0

Table 1: Noise measurement in the full readout chain.

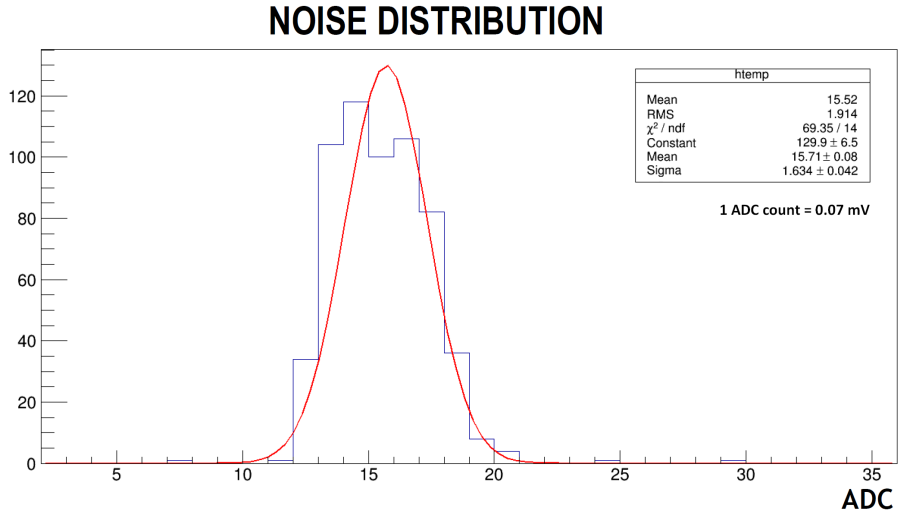

Figure 4: Noise distribution of the full matrix

4. Conclusions

A front-end electronics for the characterization of different CMOS sensors implemented in 0.11 μm CMOS technology has been developed. The circuit is intended to allow a detail characterization of the sensor performance through analog readout and to explore issues arising from the simultaneous integration in the pixel of fast digital gates. First results show that the readout electronics is fully functional. The baseline can be adjusted in a wide range making the front-end adequate for sensors of either polarity. Preliminary measurements with a ^{55}Fe source show a gain of 117 mV/fC and a noise of 58 e$^-$ rms. The study of the digital noise injected by the dedicated test structures and the characterization of matrices containing different sensor optimization is in progress.

References

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