# PixFEL project: hybrid High Dynamic Range X-ray image sensor for application at future FEL facilities

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## ABSTRACT

The goal of the pixFEL project is the realization of the sensors and readout circuits for large-area imagers to be used in future X-ray Free Electron Lasers facilities. In this paper the main application requirements are highlighted and the technological solutions adopted both in the sensor and in the readout electronics are discussed. Since the final detector will be composed by 4-side buttable tiles, active-edge sensors have been adopted to minimize the dead area at the borders of each tile. The in-pixel electronics includes a low-noise high-dynamic range preamplifier, a shaper performing Correlated Double Sampling operation and a 10-bit ADC. A 110-µm pitch pixel was designed in a 65nm process to provide single-photon detection at low photon counts, a dynamic range exceeding 90dB and 5Mfps burst frame rate.

### INTRODUCTION

X-ray Free Electron Lasers (FELs) are one of the most advanced scientific tools for the structural analysis of organic and inorganic materials [1]. FELs deliver photon beams several orders of magnitude brighter than synchrotron sources, enabling the analysis of materials and complex molecules with very high resolution. New FEL facilities with enhanced luminosity and repetition rates are currently being developed (Table 1).

The correct interpretation of the collected X-ray diffraction patterns requires the acquisition of large-area images with high dynamic range and single-photon resolution at small signals. Frame rates as high as 4.5 Mfps and tolerance to high radiation doses, reaching 1GGy are required. To comply with these tight specifications, summarized in Table 2, dedicated X-ray image sensors need to be developed [2-5]. The final goal of the PixFEL collaboration, funded by the Italian National Institute of Nuclear Physics (INFN), is the realization of a High Dynamic Range (HDR) X-ray camera to be applied in experiments at future FEL facilities. The final image sensor will be formed by several tiles to cover the large area required in diffraction experiments, as illustrated in Figure 1. In the first phase of the project, the basic building blocks, i.e. sensors, front-end electronics and ADCs, are being developed [6].

### SENSOR DESIGN

To minimize the area loss derived from tiling, which can lead to incorrect interpretation of diffraction data, activeedge detectors will be developed [7]. Deep Reactive Ion Etching will be used to create border trenches, whose sidewalls will be n+ doped to work as ohmic electrodes. Large sensor thickness ( $450\mu m$ ) is necessary to obtain high detection efficiency for the higher-energy photons. High incident photon densities can create up to  $3x10^7$  electrons per pixel in a single frame (with  $10^4$  10-keV photons) and the associated space-charge effects can slow down charge collection and spoil the sensor Modulation Transfer Function (MTF). Figure 2 shows the simulated time and distance for 95% charge collection in a 450-µm thick detector as a function of voltage. The sensors must be biased at several hundred volts to obtain fast charge collection and good MTF at high signal intensities. To these ends, pixel arrays with proper termination structures, able to stand high voltages in the presence of radiation-induced high oxide charge (up to  $3x10^{12}$  cm<sup>-2</sup> at 1GGy dose), have been designed. The cross section of a pixel array with a 4-guard ring termination structure and an edge gap of 160µm is shown in Figure 3. According to TCAD simulations, this structure could maintain a breakdown voltage larger than 400V up to the maximum radiation dose, as shown in Figure 4. The fabrication of the first detector lot at FBK (Trento, Italy) is about to start.

### PIXEL ELECTRONICS

A high-speed and high dynamic range pixel front-end was designed to cope with the very tight application specifications. The analog readout channel, shown in Figure 5, includes a charge preamplifier, a transconductor and a switched-capacitor shaper. Since local digital signal storage, to be implemented in a second tier in the final module, requires in-pixel fast digitization, a 10-bit ADC was also included. The pixel contains also the ancillary electronics needed for testing and calibration.

The HDR preamplifier needs to provide single-photon resolution at low photon counts, and a full-well signal of  $10^4$  photons. The MOS capacitor in the feedback path provides intrinsic compression thanks to its non-linear C-V characteristics. At small signals the MOS capacitor is working in the depletion region, its capacitance is small and the amplifier operates at the maximum gain. When the signal is increased, an inversion channel starts forming and the equivalent capacitance increases with the signal, until it reaches full inversion. The simulated charge sensitivity and corresponding equivalent capacitance are shown Figure 6 for a MOSFET with W/L=40µm/4µm. The simulated equivalent noise charge ENC = 60 electrons will ensure single photon discrimination capability at low photon number for 1keV photons. The shaping stage performs Correlated Double Sampling operation and provides the sampled signal to the input of the ADC.

A Successive Approximation Register (SAR) architecture was chosen for the ADC because it represents a good tradeoff between power dissipation, area occupation and conversion speed. The 10-bit resolution, while ensuring the required dynamic range, offers the margin required to accommodate for parameter dispersion and noise. The ADC uses a time-interleaved architecture to speed up the conversion time at the expense of a larger area occupation (Figure 7). In post-layout simulations, both DNL and INL are lower than 0.5 LSB, the power consumption is 85 µW and the Figure of Merit of the ADC is 21 fJ/conversion step.

An 8x8 pixel array has been submitted in a commercial 65nm process. A layout of the pixel is shown in Figure 8. The read-out channel simulated characteristics are summarized in Table 3. The first lot of test chips has been delivered and experimental results from their electrical characterization will be available by the time of the conference.

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Project	FLASH	LCLS	Eu-XFEL	LCLS II
	@DESY	@SLAC	@DESY	@SLAC
Start of	2005	2000	2015	> 2020
operation	2005	2009	2015	>2020
Photon				
energy	0.03-0.3	0.3–10	0.25-25	0.2–25
[keV]				
Frame/Burst	F	120	100	120 106
rate [Hz]	Э	120	100	120-10
Pulses per	800	1	2700	1
burst	@ 1µs		@ 220ns	

Table 1. Main features of existing and future XFEL facilities at DESY and SLAC



Figure 1. Conceptual view of a 3x3 array of 4-side buttable tiles. Each tile is composed of a sensor layer, a front-end and a digital memory and a data transmission layer assembled using 3D integration technologies.



Figure 3. Cross section of an active-edge sensor.

Frame rate (burst)	4.5 Mfps	
Frame rate (cont.)	15 kfps	
Pixel pitch	100 µm	
Total image sensor size	20 x 20 cm <sup>2</sup>	
Maximum photon number	10 <sup>4</sup>	
per pixel per frame		
Photon energy	1keV – 10keV	
On-chip memory	1 kframe	
Dead area (tiling)	< 5%	
Maximum radiation dose	1 GGy (sensor)	
	10MGy (electronics)	

Table 2. Sensor specifications.



Figure 2. Simulated time and distance for 95% charge collection as a function of bias. Simulations were performed with  $10^4$  10-keV photons and 450 $\mu$ m silicon sensor thickness.



Figure 4. Simulated breakdown voltage as a function of oxide charge density for different junction depths.



Figure 5. Block diagram of the sensor front-end circuit.



Figure 6. Simulated charge sensitivity and corresponding equivalent feedback capacitance as a function of detected 1-keV photon number



Figure 8. Pixel layout



Figure 7. ADC block diagram

Test chip				
Process	CMOS 65nm			
Array size	8 x 8			
Pixel size	110μm x 110μm			
Front – end				
ENC	60 electrons			
Gain (high gain)	1.6mV/photon (1keV)			
Gain (low gain)	40µV/photon (1keV)			
SNR (1 photon)	4.6 (1keV)			
DR	93 dB			
	Front-end: 90µW			
Power consumption	Transconductor: 120µW			
	Shaper: 40µW			
ADC				
Resolution	10 bit			
Power consumption	85µW			
SNR	60 dB			
FOM	21fJ/conversion			

Table 3. Summary of pixel simulations results