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A Physics-Informed Scaling Method for Power Electronic Converters in Power Hardware-in-the-Loop Test Beds

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ABSTRACT Power hardware in the loop (PHIL) is a modern experimental technique that allows the emulation of a full-scale converter (FSC) with the combination of a scaled-down converter (SDC), a power amplifier, and a real-time simulator, thus enabling the study of real-time interactions of power electronics with large power systems. However, assembling an accurate scaled-down replica of an FSC with off-the-shelf laboratory SDCs is practically impossible due to a mismatch in per unit losses, as well as in the impedance of the $L/LC/LCL$ filter. Consequently, the scaled-up power flow capability of SDCs differs from that of FSCs, restricting emulation to smaller regions of the four quadrants than those corresponding to the FSCs' nominal active and reactive capacity. These PHIL test beds cannot be used to emulate FSCs demanding bidirectional active and reactive power flow. Any scaling method on SDCs, emulating the entire operation of FSCs, demands underutilization of SDCs, reducing the advantages of PHIL tests. This article, therefore, proposes a physics-informed scaling method that exploits power capability curves to emulate FSCs in all four quadrants of operation. This method is independent of SDC topology, filter type, and interfacing methods. A visual identification of semiconductor device constraints bounding the emulation is also presented, utilizing the physics of converter control. A theoretical analysis of the proposed method is presented, followed by validation with MATLAB simulations and experimental tests using a 50-kVA SDC.

INDEX TERMS Capability curves, four-quadrant operation, hardware in the loop (HIL), large-scale systems, power conversion, power converter emulation, voltage-source converters (VSCs).

I. INTRODUCTION

A. BACKGROUND AND MOTIVATION

Traditional electrical grids are going through a rapid energy transition, with the penetration of power electronic systems in all aspects, starting from distributed generation, flexible alternating current transmission systems in transmission, and more power electronic interfaced industrial and residential loads [1]. There is significant ongoing research into optimizing the systems' design, control, utilization, and reliability aspects. In most cases, offline digital simulation is the preferred approach for validating solutions at the early stages of research because directly testing the actual large-power electronic converters integrated into medium- or high-voltage (HV) power systems is practically impossible and economically not viable in many laboratories. However, these offline digital simulations do not fully capture the nonlinear control interactions that power electronics cause to the power systems. Also, the analysis period should be around tens of seconds or even minutes, especially while analyzing the modern power system problems that are associated with integrating renewable sources with battery energy storage systems (BESSs) [2], subsynchronous harmonic nuisances [3], fast

frequency response support, black start capabilities, voltage support [4], etc. Running offline digital simulations of complex systems for such a long period is very cumbersome, and real-time simulations using powerful computers (real-time simulators) have, therefore, become popular [5]. However, to fully gain confidence in research findings generated through real-time simulations, some critical components under real-time simulation testing should be replaced by their real physical devices, which is referred to as hardware-in-the-loop (HIL) testing approach. However, it is less feasible or unnecessary to have a fully built device under test during the early stages of research, i.e., while developing subsystems. Therefore, scaled-down devices replicating real physical equipment are integrated into the virtual software-simulated systems. With the addition of power into the loop, the HIL concept becomes a new variant known as the power hardware in the loop (PHIL). This testing approach is enabled through a combination of the power amplifier and a real-time simulator and is gaining in popularity [6].

A general PHIL simulation test bed designed to study the implications of power electronic converters on power systems consists of a real-time simulator, a four-quadrant power amplifier for emulating ac–dc source or both sources, and often a scaled-down converter (SDC) [7], [8]. An SDC is typically a bidirectional voltage-source converter (VSC). An ac terminal from the software-simulated power system is selected and emulated as a controlled ac voltage source with the help of a power amplifier, and here, the ac terminal of the SDC is connected. The emulated ac terminal rating is limited to the nominal rating of the power amplifier, which, in turn, must be equal to or higher than the nominal rating of the SDC. In some cases, the dc input of the SDC is also emulated through a power amplifier, either in the same way or through a separate stand-alone power supply. The software-simulated power system is fed with sensed voltage and current measurements from the real converter, but scaled up in software to the magnitudes expected by the virtual simulated system. In summary, the real-time software-simulated power system assumes that a real full-scale converter (FSC) is connected to its terminals. This means that all the necessary control interactions can be studied in close relation to real practical systems. Therefore, the SDC and the four-quadrant power amplifier together emulate the FSC in PHIL tests, eliminating the drawback of not having real FSCs for research purposes in the laboratory.

B. LITERATURE REVIEW AND IDENTIFIED RESEARCH GAP

When reading the literature related to the emulation of FSCs with SDCs in PHIL tests, the following criticalities are found: an FSC or SDC is not a converter alone but a combination of the power converter and a passive (L/LC) filter or LC filter with a line frequency transformer (LFT) forming an LCL filter. There can be a difference in the passive filter topology of the SDC and the FSC [9]. An available SDC in the laboratory is rarely an accurate linear scaled-down prototype of an FSC; thus, per unit values of the SDC will have a mismatch compared with the per unit values of the FSC. In other words, the X/R ratio of the impedances of a low-power SDC differs from the X/R ratio of the FSC [10], [11], [12], [13]. These differences affect the power flow capability of SDCs when scaled up while integrating into the software-simulated systems. Consequently, the entire operating region of the FSC may not be appropriately emulated with good fidelity using the available SDC in the laboratory, i.e., in all four quadrants of power flow. One of many applications expecting an FSC's operation in all four quadrants is static synchronous compensator (STATCOM) integrated with a battery energy storage system (referred as BESS-STATCOM) and hopes to deliver grid-supporting services with bidirectional flow of active and reactive powers [14], [15], [16]. Unless the physics of the SDC are systematically understood, the PHIL tests can demand different scaling gains for rectifier and inverter power conversion modes. Proceeding with PHIL tests with same scaling gains for the rectifier and inverter can make the SDC unstable even when operated at its nominal rating. To avoid these issues, the FSC's operating region is usually narrowed down or the SDCs are underutilized to preserve a large margin (operated at less than the nominal power). Also, in some cases, test results can misguide the inaccuracy caused by wrong scaling gains toward closed-loop stability issues and increase the debugging time. This highlights an important research gap, as literature rarely discusses or presents the entire four-quadrant operation of an FSC with PHIL tests with one set of predetermined scaling gains in voltage and current feedback.

Moreover, in the PHIL research field, literature has mainly focused on the stability and accuracy of the entire simulated system with so-called hardware and software interfacing methods [17]. These interfacing methods aim to make the PHIL tests compatible with a wide range of SDCs by sufficiently adding either physical [18] or virtual impedance [19] between the SDC and power amplifiers. Damping is, therefore, provided to enhance the stability, but with a small compromise on the dynamic response of the SDC. One of the most popular software interfacing methods is the ideal transformer method, mentioned in [20] and [21], which demands complete knowledge of the SDC and adds low-pass filters in the feedback signals to improve stability. Although this article does not focus on interfacing methods, the critical point that needs to be highlighted here is that, despite having complete knowledge of the SDC, these methods ignore the impedance mismatch between the SDC and the emulated FSC. They alter the impedance further to improve the accuracy of the test, resulting in reduced power flow capability of the SDC, as mentioned in [9] and [13]. With such changes, the emulation of the FSC in all four quadrants can be challenging, pointing toward the aforementioned research gap. Experimental tests, therefore, underutilize scaled-down power converters with a limited operating range, thereby losing practical relevance significantly. This means that control interactions predicted using PHIL tests with a reduced rating of SDCs may not be accurate when compared to FSCs. A thorough scientific analysis concerning estimating the actual power flow capability

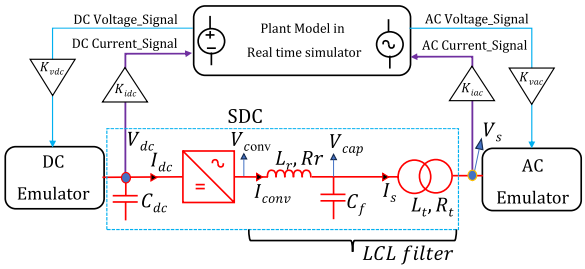

FIGURE 1. PHIL test setup.

of the SDC is, therefore, required to avoid underutilization before deciding the base power and, in turn, the scaling gains.

C. CONTRIBUTIONS

This article proposes the utilization of the entire physics of the SDC, i.e., voltage/current constraints, impedances of passive filters (between the power amplifier and the SDC), and impedance from interface methods to accurately emulate the FSC in all the four quadrants of its operation. This also meets the objective of maximizing the utilization of the SDC. From the literature, it is observed that power capability curves [22], [23], [24] are the most effective diagrams that incorporate the physics of design and control of SDCs, but have rarely been used to decide the scaling gains of SDCs in PHIL experiments. This article proposes a novel scaling method for power electronic converters, utilizing power capability curves with the following properties:

1) a physics-informed scaling method utilizing the power capability curve of the SDC for emulating the FSC in all four quadrants of operation;
2) the proposed method is independent of the SDC's circuit topology, passive filter type, and interface method;
3) visual identification of the constraints bounding the emulation with a general analytical procedure.

The rest of this article is organized as follows. The emulation of FSCs using laboratory SDCs is discussed in Section II. The theoretical estimation, sensitivity, and validation of active and reactive power capability curves are presented in Section III. A novel scaling method utilizing power capability curves is proposed in Section IV. With the help of a flowchart, all the necessary steps for emulating any FSC using SDC are also presented in the same section. In Section V, the proposed scaling method is applied to a practical 5-MVA grid-connected FSC to emulate its performance using a 50-kVA SDC, especially during a grid disturbance. The discussion is then followed by a validation of theoretical analysis with regard to offline simulation and PHIL experimental results at the National Smart Grid Laboratory in Norway. Finally, Section VI concludes this article.

II. EMULATION OF FULL-SCALE POWER CONVERTERS USING A LABORATORY SDC

Fig. 1 shows a single-line diagram of the general PHIL test setup. High-power converters are emulated in the laboratory using small-scale converters in stand-alone or dynamic PHIL modes. In stand-alone mode, dc grid and ac grid emulators can be replaced with variable voltage sources, the set points of which are decided based on the operating condition of the FSC and the nominal ratings of the SDC. Power references are sometimes set in open loop through real-time simulators. The results are then scaled up with appropriate gains to reach the FSC magnitudes, and the FSC's performance is analyzed. In dynamic PHIL mode, there is a software-simulated model running in a real-time simulator (referred to as a plant), and the dc and ac nodes between which the FSC is connected are made physically available through dc and ac power amplifiers. The SDC is connected between these physical sources. With these connections, feedback of voltage and currents of the SDC and, with appropriate scaling gains, the plant simulated in real time will have time-domain results as if a real FSC was connected. In other words, the FSC is successfully emulated using an SDC. This is possible due to the high computational power of CPUs in real-time simulators. Adding to this, the power amplifiers' high bandwidth is wide enough to reflect all the time-domain variations working as high-fidelity controllable dc and ac sources [25]. Stand-alone PHIL-mode-based emulation can be used to study the steady-state performance of the FSC with real controller validation, whereas dynamic PHIL mode can be used to explore both the transient and steady-state behavior of the FSC along with the real controller validation. These two techniques are necessary and widely utilized for emulating high-power converters for rapid prototyping. For the considered PHIL test bed, dynamic PHIL mode is used. To define the structure of the system under study, a grid-connected FSC is emulated in the laboratory with the help of SDC. This SDC under study is a 400-V 50-kVA two-level VSC integrated with an *LCL* filter (*LC* filter and 1:1 LFT). The dc-link voltage terminals of SDC and the primary side of LFT are connected to dc terminals and ac terminals of the power amplifier, respectively, aiming to integrate this hardware in the loop. A real-time simulator (OPAL-RT) with software called RT-Lab is primarily used to simulate a virtual power system and set references for the power amplifier. In addition, OPAL-RT is also used to monitor and control the SDC. Thus, the dynamic control interactions of grid-connected FSC for grid-side and dc-side disturbances can be accurately emulated and analyzed with the help of this PHIL test bed. Further details regarding the system components can be found in Section V.

III. POWER CAPABILITY CURVES OF THE SDC COMPARED TO THE FSC

Table 1 provides the design parameters of the FSC and the SDC. The objective is to emulate the FSC using the ready-to-use SDC in the laboratory with as little modification as possible. This is motivated by the fact that most SDCs in laboratories are designed to serve various research topics and are not usually tailor-made for emulating a particular FSC. The key challenge is the mismatch in the per unit impedance of passive filters for the SDC and the FSC, as the SDC is not

TABLE 1. Design Parameters of FSC and SDC

Quantity		Full-Scale Converter		Scaled-Down Converter (Nameplate values)	
Apparent power	S_{base}	5 MVA		50 kVA	
System frequency	f_{base}	50 Hz		50 Hz	
Voltage ac (rms)	V_s	690 V		400 V	
Current ac (rms)	I_s	4184 A		72 A	
Voltage dc	V_{dc}	1100 V		700 V	
Current dc	I_{dc}	4546 A		71 A	
Transformer ratio		13.8 kV / 690 V		400 V / 400 V	
Short-circuit inductance	L_t	24.2 µH	0.08 pu	316 µH	0.031 pu
Short-circuit resistance	R_t	0.476 mΩ	0.005 pu	49.4 mΩ	0.015 pu
Converter reactor inductance	L_r	77.5 µH	0.256 pu	500 µH	0.049 pu
Converter reactor resistance	R_r	0.95 mΩ	0.010 pu	32 mΩ	0.010 pu
Shunt capacitance	C_f	1.8 mF	0.054 pu	50 µF	0.050 pu
inductive-capacitive-inductive resonance	F_{res}	873.5 Hz		1.61 kHz	
Switching frequency	F_{sw}	3 kHz		7 kHz	
DC capacitance	C_{dc}	20 mF	$H = 2.42$ ms	14 mF	$H = 68.6$ ms

a linear scaled-down replica of the FSC. The passive filter (*LCL*) requirements of the considered SDC are different to the FSC, because the switching frequency of the SDC is much higher (7 kHz) than the one of the FSC (3 kHz). The choice of this specific frequency for the FSC was inspired by the design parameters of an industrial converter [26]. Thus, the resonant frequency of the *LCL* filter is designed as 873.5 Hz for the FSC and 1.61 kHz for the SDC. To the extent of the authors' knowledge, the best way to analyze the impact of impedance mismatch on scaling gains and the emulation is by comparing the power capability curves of the SDC and the FSC. The following subsection provides the theoretical framework for obtaining capability curves of a grid-connected VSC.

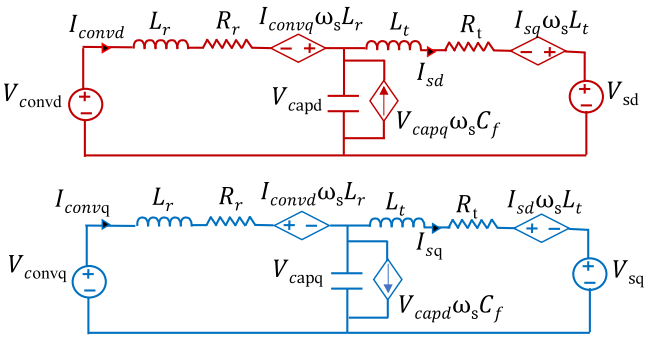

FIGURE 2. *d*- and *q*-axis equivalent circuits of the SDC.

A. THEORETICAL DERIVATION OF POWER CAPABILITY CURVES

The impedance mismatch is best viewed when per unit power capability limits of both the FSC and the SDC are plotted together. This approach forms the basis for analyzing scaling methods for PHIL test beds. The proposed analysis is generic as it includes the impedances of the passive *LC* filter and the LFT. It is also shown that the analysis can be applied to the VSC with only *LC* or *L* filters with a few modifications. Equations (1)–(4) form the basis of the mathematical derivation to evaluate the power capability of the VSC with an *LCL* filter shown in Fig. 1. The direct- and quadrature-axis equivalent circuits for Fig. 1 are shown in Fig. 2 for better understanding of symbol nomenclature.

$$Z_t = R_t + j\omega_s L_t;\ Z_r = R_r + j\omega_s L_r;\ X_{Cf} = \frac{1}{\omega_s C_f} \tag{1}$$

$$v_{capdq} = R_t i_{sdq} + L_t \frac{d}{dt} i_{sdq} + j\omega_s L_t i_{sdq} + v_{sdq} \tag{2}$$

$$v_{convdq} = R_r i_{convdq} + L_r \frac{d}{dt} i_{convdq} + j\omega_s L_r i_{convdq} + v_{capdq} \tag{3}$$

$$i_{convdq} = i_{sdq} + C_f \frac{d}{dt} v_{capdq} + j\omega_s C_f v_{capdq}. \tag{4}$$

The voltages and currents in (1)–(4) are represented in a rotating reference frame [27]. The direct and quadrature quantities appear as vectors in a complex plane with the q component aligned with the complex number axis. The variables v_{capdq}, v_{sdq}, v_{convdq}, i_{sdq}, and i_{convdq} denote, respectively, the instantaneous fundamental dq vectors of the filter capacitor voltage, source voltage (referred to low-voltage side), converter voltage, source current, and converter current. The angle for the Park transformation is obtained from a phase-locked loop applied typically over the measured filter capacitor voltage. The angular fundamental frequency is denoted by ω_s. The quantities Z_t and Z_r are complex leakage impedances of the LFT and the converter reactor, L_t and R_t are the inductance and resistance of the LFT referred to low-voltage side, respectively, L_r and R_r are the inductance and

resistance of the converter reactor, respectively, and C_f and X_{Cf} are the capacitance and reactance of the filter capacitor, respectively.

Ignoring the derivative terms for a steady-state analysis, (2)–(4) can be manipulated to obtain (11), which expresses, in a generic form, the source current for the VSC with an *LCL* filter (denoted by i_{sdq}^{LCL})

$$v_{convdq} = i_{convdq}Z_r + i_{sdq}Z_t + v_{sdq} \tag{5}$$

$$(v_{convdq} - v_{sdq}) = i_{sdq}Z_t + Z_r\left(i_{sdq} + j\frac{v_{capdq}}{X_{Cf}}\right) \tag{6}$$

$$(v_{convdq} - v_{sdq}) = i_{sdq}Z_t + Z_r\left(i_{sdq} + j\left(\frac{Z_t i_{sdq} + v_{sdq}}{X_{Cf}}\right)\right) \tag{7}$$

$$(v_{convdq} - v_{sdq}) = i_{sdq}Z_t + i_{sdq}Z_r + j\frac{Z_r Z_t i_{sdq}}{X_{Cf}} + j\frac{Z_r v_{sdq}}{X_{Cf}} \tag{8}$$

$$(v_{convdq} - v_{sdq}) = i_{sdq}\left(Z_t + Z_r + j\frac{Z_r Z_t}{X_{Cf}}\right) + j\frac{Z_r v_{sdq}}{X_{Cf}} \tag{9}$$

$$\left(v_{convdq} - v_{sdq}\left(1 + j\frac{Z_r}{X_{Cf}}\right)\right) = i_{sdq}\left(Z_t + Z_r + j\frac{Z_r Z_t}{X_{Cf}}\right) \tag{10}$$

$$i_{sdq} = i_{sdq}^{LCL} = \frac{v_{convdq} - v_{sdq}\left(1 + j\frac{Z_r}{X_{Cf}}\right)}{Z_t + Z_r + j\frac{Z_t Z_r}{X_{Cf}}}. \tag{11}$$

Once the source current i_{sdq}^{LCL} is estimated, the three-phase instantaneous active and reactive powers of the source can be calculated as

$$P_s = 1.5\ \text{Real}\left(v_{sdq}i_{sdq}^{*}\right) \tag{12}$$

$$Q_s = 1.5\ \text{Imag}\left(v_{sdq}i_{sdq}^{*}\right) \tag{13}$$

where P_s and Q_s are three-phase instantaneous active and reactive powers at the HV side of the transformer, respectively.

Equation (11) can be simplified for transformerless topologies of VSCs that are directly coupled to the ac source without an LFT. In case of an *LC* filter, Z_t is set to zero resulting in (14). In case of a simple *L* filter, Z_t and C_f are set to zero resulting in (15). Notice that i_{sdq}^{LC} and i_{sdq}^{L} represent the source current with an *LC* and an *L* filter, respectively:

$$i_{sdq} = i_{sdq}^{LC} = \frac{v_{convdq} - v_{sdq}\left(1 + j\frac{Z_r}{X_{Cf}}\right)}{Z_r} \tag{14}$$

$$i_{sdq} = i_{sdq}^{L} = \frac{v_{convdq} - v_{sdq}}{Z_r}. \tag{15}$$

Equations (12) and (13) with i_{sdq}^{LC} and i_{sdq}^{L} can again be used to compute three-phase instantaneous active and reactive powers at the source.

Using the mathematical equations derived in (1)–(15) and the algorithms provided in [23], power capability curves are drawn for both the FSC and the SDC in Fig. 3 for the parameters given in Table 1. These curves are typically constrained by two limits: 1) the current limit decided by the peak of nominal ac current rating of the converter and 2) the voltage limit of the converter limited by the maximum dc-link voltage and the pulsewidth modulation (PWM) technique used. These limits are indirectly related to the safe operating voltage/current (peak) rating of semiconductor devices with standard safety factors. In Fig. 3(a), solid and dashed curves represent the power capability curve of the FSC when V_s is 1.0 p.u. and 0.9 p.u. The maximum operating voltage on the dc link for the FSC is 1000 V. However, it is worth noting that the design parameter listed in Table 1 indicates 1100 V, factoring in a 10% tolerance. For the FSC, the maximum operating voltage on the dc link is 1000 V. The red and black portions of the capability curves (both solid and dashed) represent converter voltage and current limits, respectively. These curves show that, although the converter is rated for 5 MVA, its operating conditions are constrained within these capability curves. Similarly, for the SDC, the solid and dashed curves in Fig. 3(b) represent the power capability curve when V_s is 1.0 p.u. and 0.9 p.u. For the SDC, despite the maximum voltage on the dc link being 700 V, the operating dc link is decided by the ac–dc ratio of the FSC that it will represent in PHIL tests as given in (16). The superscript "fsc" denotes quantities related to the FSC and the superscript "sdc" denotes quantities of the SDC. If this ratio is not maintained, the SDC harmonic spectrum resulting from PWM switching will differ from the FSC, leading to higher converter voltage and current distortion when scaled to represent the FSC [11]. Based on these assumptions, the dc-link voltage of the SDC is calculated as in (17), and the same is used for generating the power capability curve in Fig. 3(b). Starting from the next section, the capability curves will be drawn in a single color, without highlighting the voltage and current limits

$$V_{\text{dc}}^{\text{sdc}}[\text{V}] = V_s^{\text{sdc}}\frac{V_{\text{dc}}^{\text{fsc}}}{V_s^{\text{fsc}}} \tag{16}$$

$$V_{\text{dc}}^{\text{sdc}}[\text{V}] = 400 \times \frac{1000}{690} = 579.7[\text{V}]. \tag{17}$$

The highlighted numbers (yellow) in the FSC capability curve can be read as: (0.261) the FSC is capable of generating a reactive power of $Q_{\text{FSC}} = 0.261$ Mvar when the active power is $P_{\text{FSC}} = 0$ MW and the voltage is $V_s = 1.0$ p.u.; (1.5613) the FSC can deliver $Q_{\text{FSC}} = 1.5613$ Mvar when $P_{\text{FSC}} = 0$ MW and $V_s = 0.9$ p.u. Similarly, the highlighted number (yellow) in the SDC capability curve shows that the SDC is capable of generating a reactive power of $Q_{\text{SDC}} = 3.71$ kvar at $P_{\text{SDC}} = 0$ kW and $V_s = 1.0$ p.u. When $V_s = 0.9$ p.u., the SDC can deliver $Q_{\text{SDC}} = 45$ kvar at $P_{\text{SDC}} = 0$ kW. The validation

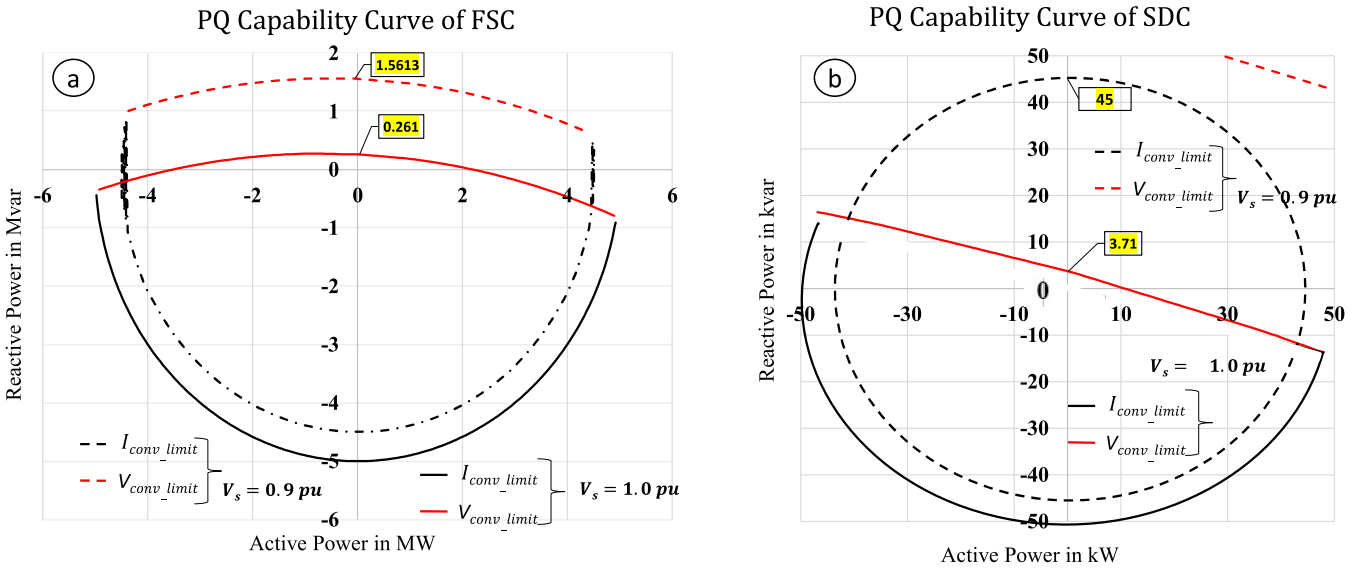

FIGURE 3. (a) PQ capability curves of FSC and (b) the PQ capability curves of SDC (black and red curves represent converter current and voltage limits, solid and dashed nature of curves represent $V_s = 1.0$ p.u. and $V_s = 0.9$ p.u.).

of the theoretical capability curve is presented in Section III-C with supporting simulation results. It is also worth noting that the impact of mismatched impedances between the FSC and the SDC can be visually confirmed through the power capability curves. This is particularly true when the emulation aims to reproduce enough operating points of the FSC across all four quadrants. As a consequence of mismatched impedances, the X/R ratio of the *LCL* filter in the SDC is also different compared to the *LCL* filter in the FSC, becoming the only reason for the asymmetrical capability curve in Fig. 3(b) (solid lines). In contrast, the capability curve of the FSC is centered symmetrically around the y-axis in Fig. 3(a) (both solid and dashed). The sensitivity of the capability curves to the X/R ratio is presented in Section III-B.

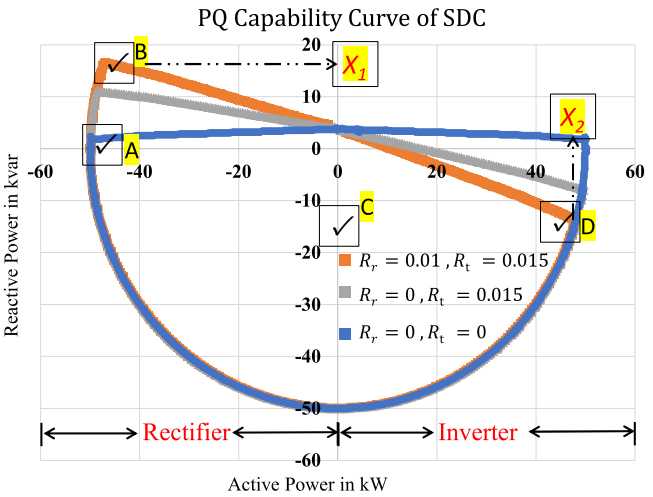

FIGURE 4. Sensitivity analysis of PQ capability for the SDC.

B. SENSITIVITY OF X/R RATIO OF LCL FILTER ON POWER CAPABILITY CURVES

This section sheds light on the influence of the *LCL* filter's X/R ratio on the power capability curves. Between the FSC and the SDC, the analysis can be carried out on the SDC, as it presents a case with asymmetrical power capability curves. Fig. 4 shows power capability curves for an SDC with: 1) $R_r = 0.01$ p.u. and $R_t = 0.015$ p.u. (orange); 2) $R_r = 0$ p.u. and $R_t = 0.015$ p.u. (gray); and 3) $R_r = 0$ p.u. and $R_t = 0$ p.u. (blue). From these curves, it can be understood that the *LCL* filter's resistance (and, in turn, the X/R ratio) can tilt capability curves. When the resistance of the converter-side main inductor and the transformer leakage resistance are assumed to be zero, the presented capability curve becomes symmetrical similar to the capability curve of the FSC seen in Fig. 3(a). This is because most of the SDCs employed in laboratories are in the capacity range of 5–100 kVA, and the transformers used have significant resistance in the overall leakage impedance compared to the leakage impedance in the FSCs. This is unavoidable as the SDCs are usually built for multitopic research purposes and are not tailor-made to suit any single application. This work assumes that there will be no provision to change any of the passive elements of the SDC. In summary, the scaling problem can now be defined as the scaling of an SDC with an asymmetrical capability curve to emulate an FSC with a symmetrical capability curve for PHIL test setups.

C. VALIDATION OF THEORETICAL POWER CAPABILITY CURVES

The overall baseline for the problem formulation lies in the assumption that the computed power capability curves put a constraint on the active and reactive power references used for converter control. To validate this, the SDC is controlled

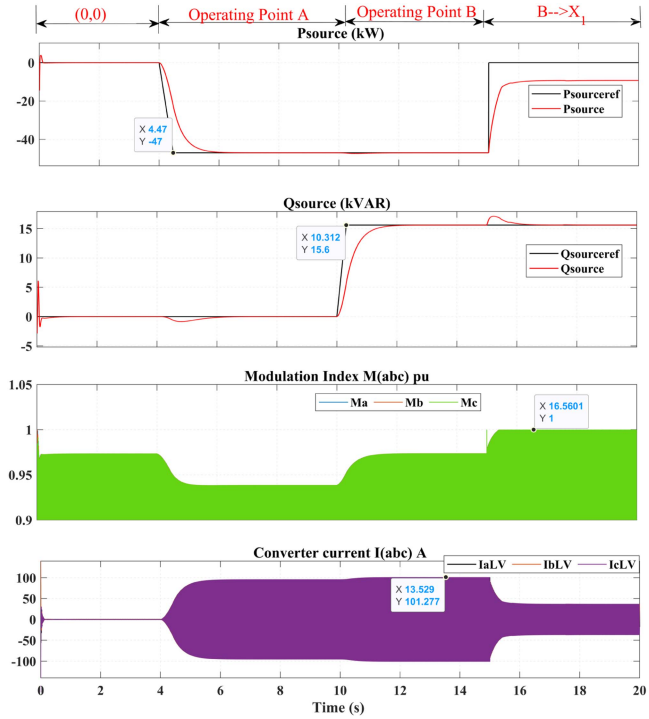

FIGURE 5. Validation of power capability curve limits when the SDC is in the rectifier mode.

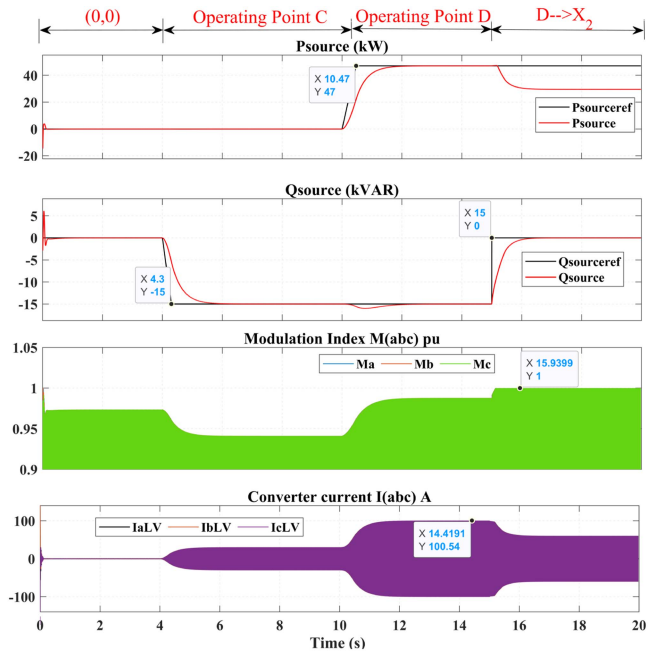

FIGURE 6. Validation of power capability curve limits when the SDC is in the inverter mode.

at critical limits in all four quadrants of the asymmetrical capability curve. A simulation model in MATLAB Simulink is developed in a similar way to the power schematic shown in Fig. 1, in which the SDC is connected to the grid and controlled with cascaded control loops in the grid-following mode [28], [29], [30]. For switching between rectifier and inverter operating modes, the outer loop active power reference polarity is changed. In the theoretical capability curves, the maximum converter output voltage is based on the sine PWM technique with a third harmonic injection for better dc bus voltage utilization [31]. The same has been used in simulations. In Fig. 4, the capability curve with $R_r = 0.01$ p.u. and $R_t = 0.015$ p.u. is marked with six operating points A, B, C, D, X_1, and X_2. Operating points A and B are chosen to validate the converter capability limits for the power flow direction being ac to dc, i.e., as rectifier operation (left-hand side to the y-axis of the capability curve). Similarly, operating points C and D appear on the right-hand side to the y-axis of the capability curve, indicating the power flow direction from dc to ac, i.e., inverter operation. Reference powers for all four operating points are summarized in Table 2.

TABLE 2. Operating Points and Reference Powers

Operating Point	Reference Powers
A	$P_{\text{ref}} = -47$ kW and $Q_{\text{ref}} = 0$ kvar
B	$P_{\text{ref}} = -47$ kW and $Q_{\text{ref}} = 15.6$ kvar
C	$P_{\text{ref}} = 0$ kW and $Q_{\text{ref}} = -15$ kvar
D	$P_{\text{ref}} = 47$ kW and $Q_{\text{ref}} = -15$ kvar

Fig. 5 shows simulation results for the rectifier operation of the SDC. At time $t = 4$ s, the active power reference is set to track operating point A ($P_{\text{ref}} = -47$ kW and $Q_{\text{ref}} = 0$ kvar). Referring only to the nonideal capability curve in orange from Fig. 4, point A is inside the capability curve; hence, the converter reaches point A. It is important here to note that point A is close to the converter current limit line (101.8 A) but away from the converter voltage limit line. The same can be observed in the modulation index M_{abc} and converter current I_{abc} plots shown in Fig. 5. To trace the edge of the capability curve, power references are changed to operating point B ($P_{\text{ref}} = -47$ kW and $Q_{\text{ref}} = 15.6$ kvar) at time $t = 10$ s. The SDC properly reaches B, thus hitting both current and voltage limits. The actual validation of the capability curve is noticed when operating point B is shifted to X_1 ($P_{\text{ref}} = 0$ kW and $Q_{\text{ref}} = 15.6$ kvar) outside the orange capability curve; SDC loses active power regulation by hitting the voltage limit despite the presence of a significant margin for the current limit.

For an SDC operating in the inverter mode, i.e., to the right-hand side to the y-axis of the capability curve, simulation results are shown in Fig. 6. At time $t = 4$ s, power references are set to operating point C ($P_{\text{ref}} = 0$ kW and $Q_{\text{ref}} = -15$ kvar), and at time $t = 10$ s, references are set to operating point D ($P_{\text{ref}} = 47$ kW and $Q_{\text{ref}} = -15$ kvar) properly tracking the edge of the capability curve (i.e., both current and voltage limits). At time $t = 15$ s, references are changed to a point X_2 ($P_{\text{ref}} = 47$ kW and $Q_{\text{ref}} = 0$ kvar) outside the capability curve, and the active power regulator does not track the reference after reaching the voltage limit. These cases are selected to validate the theoretical capability curves of the SDC and to especially highlight the impact of asymmetry in

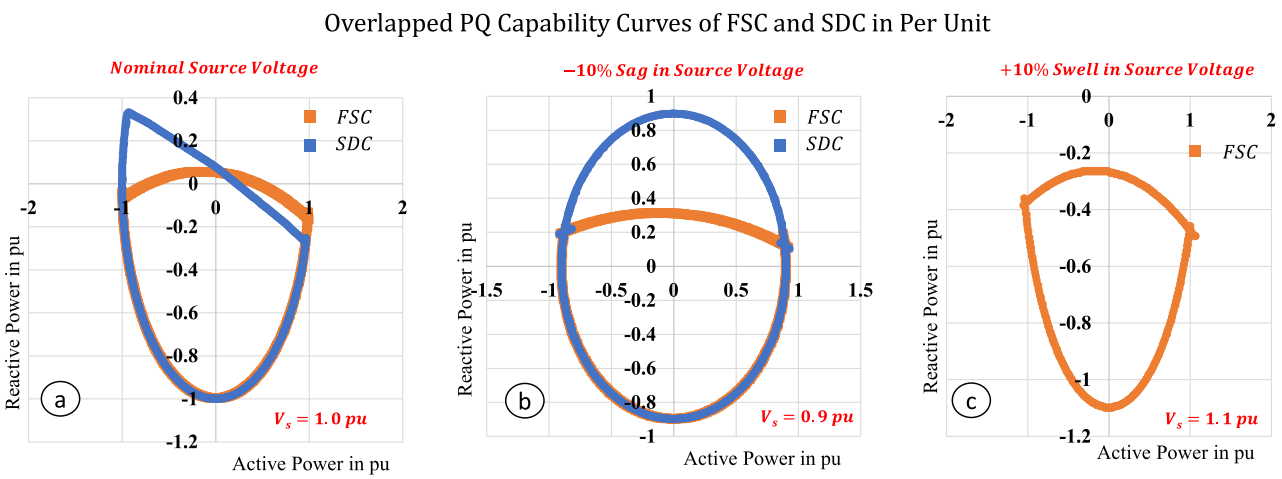

FIGURE 7. Per unit power capability curves of the FSC and the SDC when (a) $V_s = 1.0$ p.u., (b) $V_s = 0.9$ p.u., and (c) $V_s = 1.1$ p.u.

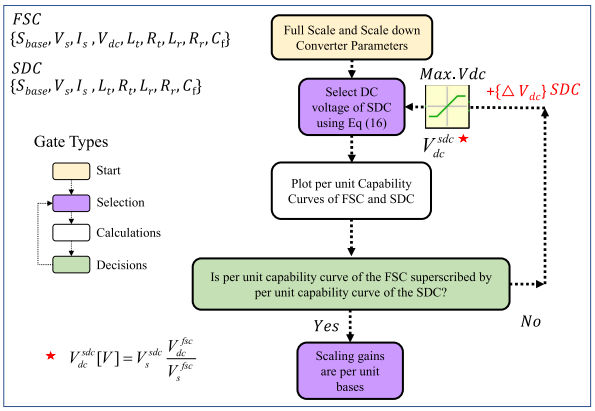

FIGURE 8. Physics-informed scaling method for emulating FSC using SDC.

rectifier and inverter operations. It is a unique perspective to see power regulators struggle to track zero-valued references but quickly track nonzero values, signifying the necessity of saturating the references through capability curves.

D. CHALLENGE WITH SCALING AN SDC TO EMULATE AN FSC

With the validation presented in Section III-C, it is clear that SDCs and FSCs have different power capability curves, as an SDC is not designed to be used as an accurate scaled-down prototype for an FSC. The challenge is that, for PHIL tests, an SDC with an asymmetrical power capability curve is used to emulate an FSC, which has a symmetrical power capability curve. The problem is better viewed if the per unit capability curve of the SDC and the FSC are plotted together, as shown in Fig. 7. It is important to remember here that per unit capability curves are obtained without violating (17), which is the fundamental step in achieving the harmonic invariance with scaling of an SDC to an FSC, as mentioned in [11]. In Fig. 7(a), per unit capability curves of an FSC and an SDC are plotted at $V_s = 1.0$ p.u. This approach shows that the SDC perfectly emulates the FSC in the rectifier mode but fails to scale up correctly in inverter operation. Without examining capability curves, researchers working on PHIL test beds might have to operate with higher or different dc and ac voltages of the SDC to emulate the FSC for bidirectional power flow, thus violating the scaling gains for harmonic invariance. Moreover, it would be cumbersome to accurately compute the required ac- and dc-link voltages of the SDC with trial and error approaches for all the operating points. Also, simply using nameplate details of the SDC can result in increased distortion of voltages and currents and misleading conclusions around stability and interface issues.

Meanwhile, the FSC may not necessarily operate continuously at $V_s = 1.0$ p.u. It is, therefore, essential to study undervoltage and overvoltage capability curves with an approach similar to the one presented previously. A $\pm 10\%$ variation in the source voltage is considered for the curves shown in Fig. 7(b) and (c), respectively. As per the physics of grid-following converter controls, it is well known that the reactive power capability increases when the grid voltage decreases. This can be seen when both orange and blue curves are compared in Fig. 7(a) and (b) for both the FSC and the SDC. It can also be observed that the SDC is quite sensitive to voltage variations, compared to the FSC. This is why the entire PQ capability curve for the SDC is available in Fig. 7(b) for $V_s = 0.9$ p.u. This means that the SDC scales accurately to emulate the FSC at all its operating points. But with some precise observations, it can be seen that FSC capability limits shrunk to less than 1 p.u., as source voltage is no longer 1 p.u. Full emulation of the FSC is not possible just with these operating electrical quantities. For $V_s = 1.1$ p.u., the SDC is not controllable; hence, the capability curve is shown only for the FSC in Fig. 7(c). This means that, at these dc and ac voltages, the SDC cannot emulate the FSC with any scaling gains.

IV. PROPOSED PHYSICS-INFORMED SCALING METHOD

The proposed physics-informed scaling method for emulating an FSC with an SDC by utilizing power capability curves

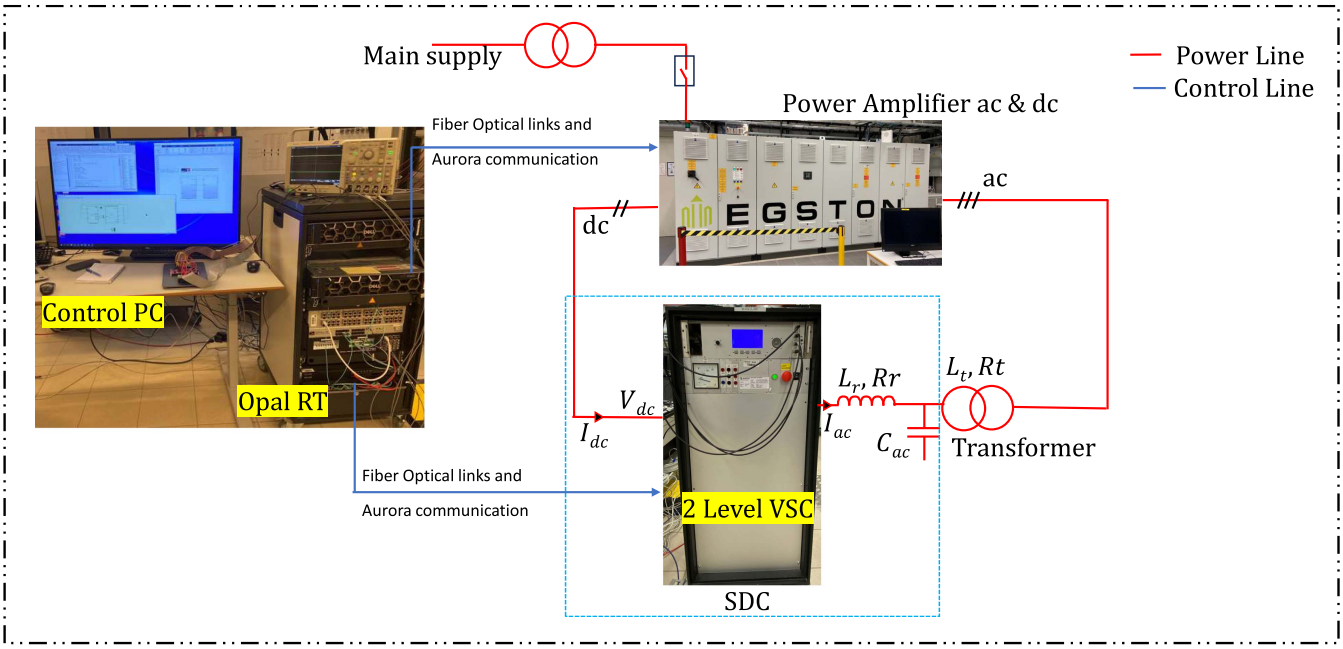

FIGURE 9. National Smart Grid Laboratory at the Norwegian University of Science and Technology, Trondheim.

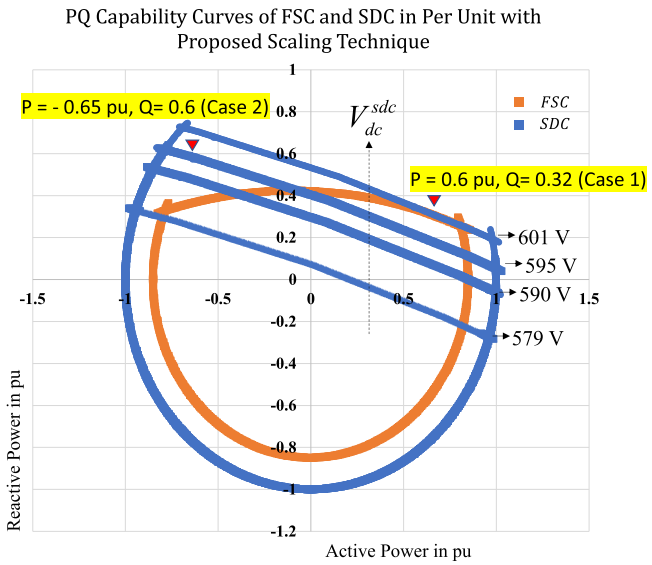

FIGURE 10. Superscribing FSC capability curve with the SDC using the proposed method.

is visualized in Fig. 8. This scaling method is implemented as a MATLAB script with a combination of two functions: one for the FSC and the other for the SDC. The project files are made publicly available at [32]. As a starting step, the MATLAB script acquires all the required design parameters of the converter, transformer, and *LCL* filter (for both the FSC and the SDC). As learned from the previous work [11], the dc link of the SDC in the second step should be selected as (16) for harmonic invariant scaling. Following this, the method plots the per unit power capability curves of both the FSC and the SDC (plotted on the same x- and y-axes). It is an important requirement and worth to mention here that the capability curves must be plotted in per unit only as we are comparing the region of operation for both the FSC and the SDC on the same x- and y-axes. In the next step, these capability curves confirm whether the FSC can emulate the SDC with the decided electrical quantities. One of the critical properties of the physics-informed scaling method is its visual aspect. The FSC can be emulated by the SDC in both rectifier and inverter modes if the per unit capability of the FSC is contained within the per unit capability curve of the SDC. On the one hand, if this condition is true, scaling gains applied to the SDC to emulate the FSC are nothing but the per unit base values of the FSC multiplied by the per unit (voltage and current) quantities of the SDC. In other words, the measured and sensed quantities of the SDC multiplied with FSC per unit bases can be directly used in virtual simulations where the FSC is assumed to be connected to. On the other hand, if this condition is false, the dc-link voltage of the SDC is increased by the minimum value (limited by peak dc-link voltage rating shown as saturator in the figure) to have the capability curve of the FSC contained in the capability curve of the SDC. Once this is completed, the scaling gains are again the per unit bases of the FSC, multiplied by the per unit quantities of the SDC. To simply put, the emulation is fully achieved if the SDC capability curve encapsulates capability curve of the FSC. Notably, by adding only the minimum required dc-link voltage to contain the capability curve of the FSC within the SDC curve, the scaling technique will stay close to an ideal harmonic invariance operation. Loss of harmonic invariance is, of course, inevitable if an improperly SDC has to be fully

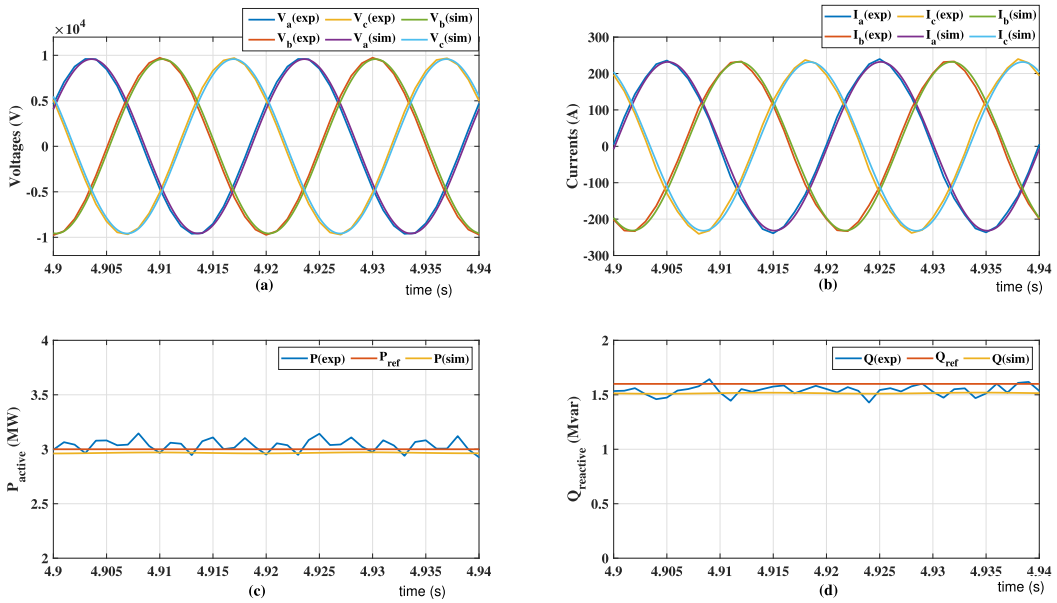

FIGURE 11. Simulation and experimental results for Case 1 showing the effectiveness of the proposed method. (a) Converter voltages (V_{cap}) measured at the filter capacitor referred to the HV side. (b) Converter currents (I_{conv}) referred to the HV side. (c) Active power at the HV side. (d) Reactive power at the HV side.

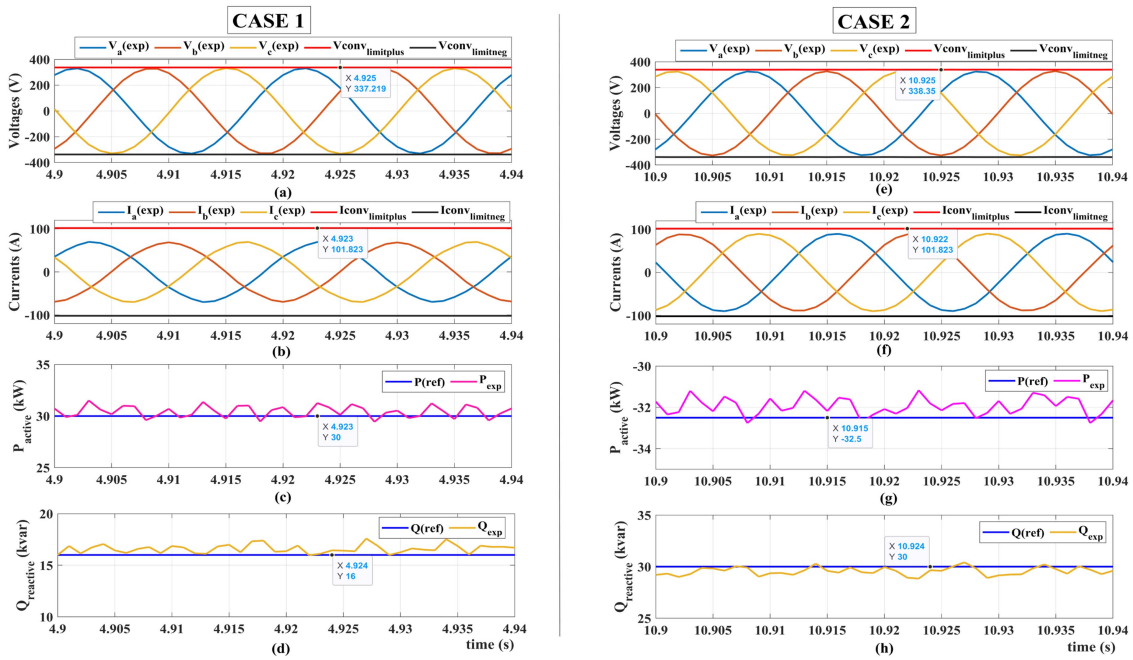

FIGURE 12. Unscaled experimental results of the SDC. (a) and (e) Converter voltages (V_{cap}) measured at the filter capacitor referred to the HV side for cases 1 and 2, respectively. (b) and (f) Converter currents (I_{conv}) referred to the HV side for cases 1 and 2, respectively. (c) and (g) Active power at the HV side for cases 1 and 2, respectively. (d) and (h) Reactive power at the HV side for cases 1 and 2, respectively.

utilized at its designed nominal rating to emulate the FSC in all quadrants.

V. EXPERIMENTAL VALIDATION AND RESULTS

The proposed method is validated using the PHIL test bed at the National Smart Grid Laboratory, Trondheim, Norway. The test setup is arranged as shown in Fig. 9. The power amplifier Egston CSU 200: Compiso System unit rated for 200 kVA with six outputs at a 5-kHz bandwidth can emulate a controllable three-phase ac voltage source and a dc source. Emulated ac terminals are connected to the SDC through a 1:1 delta–wye LFT for galvanic isolation, and dc source is connected to the dc-link bus of the SDC. The connected SDC is a 50-kVA two-level VSC with an *LC* filter (together

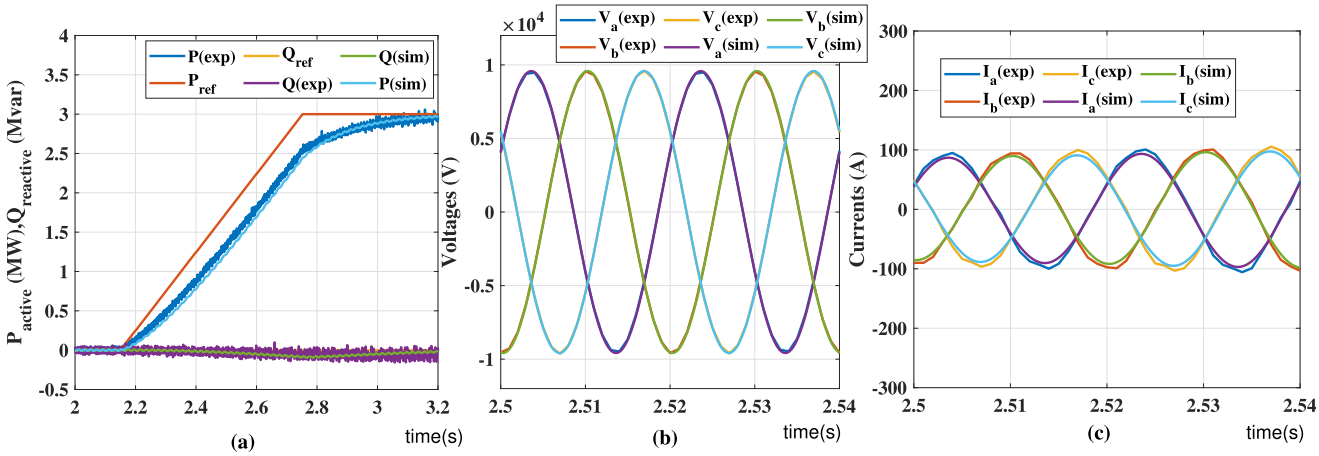

FIGURE 13. Simulation and experimental results for Case 1 showing the effectiveness of the proposed method for transient condition in the active power regulator. (a) Active power and reactive power at the HV side. (b) Converter voltages (V_{cap}) measured at the filter capacitor referred to the HV side. (c) Converter currents (I_{conv}) referred to the HV side.

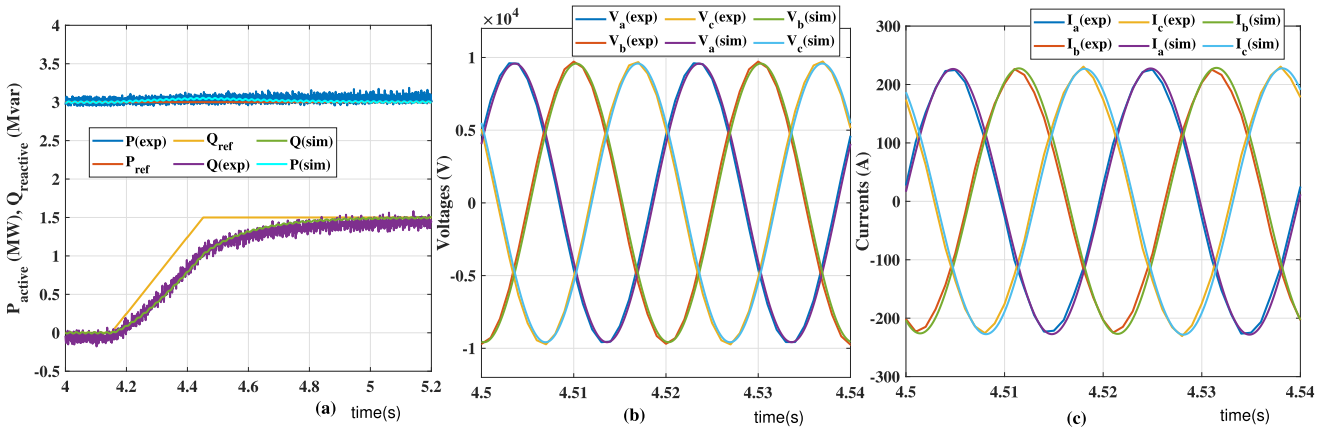

FIGURE 14. Simulation and experimental results for Case 1 showing the effectiveness of the proposed method for transient condition in the reactive power regulator. (a) Active power and reactive power at the HV side. (b) Converter voltages (V_{cap}) measured at the filter capacitor referred to the HV side. (c) Converter currents (I_{conv}) referred to the HV side.

with the LFT, becomes *LCL* filter). A real-time simulator (OPAL-RT OP4520) with a software called RT-Lab is used to monitor and set references for power amplifier and to control the SDC. This platform can run electromagnetic transient simulations in real time. Control of SDC is done through a Simulink model running at a step time of 50 µs, translated into embedded C code with the help of RT-lab software and is loaded into the OP4520 cores. The bidirectional power flow is recirculated between the ac and dc sources, thereby making the test setup efficient. The flown power during tests from input mains is only the losses resulting from power conversion.

A. PRACTICAL SCENARIO: SCALING OF AN SDC TO EMULATE AN FSC DURING GRID DISTURBANCE

The critical case seen in Fig. 7 shows that when the SDC is operated within its nominal rating, it can only emulate the FSC in rectifier operation, but fails to emulate it in the inverter mode. Although this identifies a theoretical scaling problem with $V_s = 1.0$ p.u., typical challenges in scaling arise for practical situations when the FSC is expected to stay connected to the grid during disturbances, and such tests are analyzed through PHIL test setups using an SDC. One such practical case is selected to validate the effectiveness of the proposed algorithm. The source voltage of the FSC is considered at the maximum voltage sag scenario as 0.85 p.u., and the resultant capability curve of the FSC at this source voltage is plotted as a solid orange curve in Fig. 10. The FSC is expected to exchange active power and support the grid by generating reactive power to counteract the voltage sag.

B. CASE 1

Applying the proposed method for the considered practical scenario, the per unit capability curves of both the FSC and the SDC are obtained and plotted on top of each other. As expected, most of the capability curve of the SDC does not superscribe the capability curve of the FSC, as seen in Fig. 10, corresponding to 579 V in solid blue. This indicates that

most of the operating regions of the FSC cannot be emulated using the considered SDC. The dc-link voltage of the SDC is, therefore, increased in steps until an optimal dc-link voltage of the SDC is reached (601 V), i.e., when the resultant capability curve of the SDC superscribes the capability curves of the FSC. To validate the scaling method effectively, Case 1 represents the operation of the SDC in the inverter mode at $P_{\text{ref}} = 0.6$ p.u. or 30 kW and $Q_{\text{ref}} = 0.32$ p.u. or 16 kvar, where the SDC is just superscribing the FSC. The test results are captured in real time at 1-ms resolution. Using MATLAB-Simulink-based average model of the FSC, an offline simulation of the FSC operated in the grid-following mode is performed at the chosen operating point where the absolute values are $P_{\text{ref}} = 0.6$ p.u. or 3 MW and $Q_{\text{ref}} = 0.32$ p.u. or 1.6 Mvar. When the measured instantaneous values of voltages and currents are subsequently scaled up using per unit bases, an excellent match with FSC simulation results captured at the HV side can be seen in Fig. 11(a)–(d), which highlight the effectiveness of the proposed method. Due to this, the measured and simulated average powers are also scaled up with a minimal error, and the FSC is therefore well emulated with the SDC.

To further validate the proposed method, unscaled measurements of voltages, currents, and powers of the SDC are shown in Fig. 12(a)–(d). The power regulators (active and reactive) are tracking well at the respective references ($P_{\text{ref}} = 30$ kW and $Q_{\text{ref}} = 16$ kvar), as seen in Fig. 12(c) and (d). On the one hand, the converter voltages measured at the filter capacitor are plotted along with the maximum voltage limits of the sine PWM scheme with third harmonic injection in Fig. 12(a). On the other hand, converter currents measured before the filter capacitor are plotted along with the peak nominal current in Fig. 12(b). It is worth noting that the chosen operating point of Case 1 (solid blue curve corresponding to 601 V in Fig. 10) is hitting the voltage limit (337.2 V) on the capability curve but is away from the current limit (101.8 A). The same can be seen in Fig. 12(a) and (b).

C. CASE 2

To experimentally validate the asymmetric capability curve of an SDC, an operating point (Case 2) in the rectifier mode outside the FSC's operating region is chosen, as seen in Fig. 10. Power regulators track the desired references ($P_{\text{ref}} = -0.65$ p.u. or -32.5 kW and $Q_{\text{ref}} = 0.6$ p.u. or 30 kvar) in Fig. 12(g) and (h). This reactive power is much higher than in Case 1, which can only be reached with an asymmetrical capability curve of the SDC (higher reactive power capability in the rectifier mode). As the operating point is close to both voltage and current limits on the solid blue curve corresponding to 601 V in Fig. 10, the converter voltage and currents are very close to their limits (338.35 V and 101.8 A, respectively) in Fig. 12(e) and (f).

D. TRANSIENT ANALYSIS

As long as the operating point of the FSC lies within the obtained emulated region of the SDC using the proposed algorithm, any transient change in the FSC operating points will not cause any stability issues during PHIL experiments. However, the exact matching of the transient response of the FSC with the SDC requires a thorough analysis on the tuning of proportional–integral regulators. It is not a straightforward approach to match the dynamics of outer power and inner current regulators for the SDC with the FSC because of the mismatched time constants and controller bandwidths. Adding to this, the decoupling of d- and q-axis current regulators heavily depends on impedance parameters, and, if they are mismatched, transient response can also differ. However, in many cases, SDCs operate at higher switching frequencies, and their controllers can be designed to work at higher sampling rates and bandwidth. Alternatively, FSCs are typically high-power converters, and their outer loop references are set in a ramp fashion. Ramp rates are usually limited to a few MW/s or Mvar/s; thus, slowing down SDC's transient response can help to match the transient response of FSC's. The procedure around controller tuning for getting an exact match of transient response in PHIL test beds is another open research area, and it is considered out of scope of this article. However, an attempt has been made to present transient responses in reaching Case 1, whose steady-state scaled and unscaled results are shown in Figs. 11 and 12, respectively. Case 1 presents a critical operating point where the capability curves of the FSC and the SDC meet with the proposed algorithm. Thus, the transient response results are discussed only for Case 1. A two-step approach by sequentially adding transients to both active and reactive power regulators is considered to prove the effectiveness of the proposed algorithm. In Fig. 13(a), the desired active power reference of Case 1 is set to 3 MW at 2.15 s; the reference power is ramped up at 5 MW/s, reaching 3 MW at 2.75 s. In the meantime, the reactive power reference is set to zero. The simulated measured active power from the FSC and the measured active power from the SDC when scaled up reach the desired reference power with a good match in transient response. The instantaneous voltages and currents of the simulated FSC and the scaled-up SDC are also seen to have a good match when zoomed in between the response, i.e., 2.5–2.54 s (two cycles), as seen in Fig. 13(b) and (c). Once the active regulator loop is settled, the desired reactive power reference is set to 1.5 Mvar at 4.15 s at the same ramp rate (5 Mvar/s). A good match in regulator response and instantaneous voltages/currents is again observed in Fig. 14(a)–(c). As the converter reaches the Case 1 operating point, the magnitudes of voltage and current match with the steady-state results presented in Figs. 11 and 12. Thus, with the proposed scaling method, every operating point on the FSC can be emulated with a good match in both the transient and steady states.

VI. CONCLUSION

Small-scale converters in PHIL tests in laboratories are rarely a linear scaled-down version of the FSC being emulated. Comparing an FSC and an SDC, a mismatch in the per unit values of the impedances (in turn, the X/R ratio) is inevitable.

This affects the power flow of the SDC connected to a power amplifier, and the scaling gains are often decided on the basis of a cumbersome trial and error method that does not guarantee the emulation of the FSC in all four quadrants. This article, therefore, proposes a physics-informed scaling method based on power capability curves that are drawn using fundamental quantities (voltage and current), aiming to emulate the FSC in all four quadrants of operation. Also, for the first time, a visual identification of the semiconductor device constraints bounding the emulation process is presented and used to decide scaling gains. The performance of the proposed physics-informed scaling method was tested by comparing the instantaneous voltages, currents, and powers of a simulated FSC with the measured equivalents of an SDC in a PHIL setup for Case 1 (see Section V-B). In addition, the validation of asymmetrical power capability curves in Case 2 (see Section V-C) proves that SDCs are very sensitive to the X/R ratio of the impedances between the power amplifier and the converter. As the method relies only on the fundamental quantities, the proposed method offers a general scaling method that is independent of SDC's topology, i.e., two-level or multilevel VSCs, etc. As the method is applied to a converter with an *LCL* filter, it is also shown to be easily adaptable to an *LC* or *L* filter. This scaling method can, therefore, be widely applicable to PHIL test setups aimed at utilizing an improperly SDC in the laboratory to emulate bidirectional FSCs operating in all four quadrants.

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