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Simulation and first characterization of MAPS test structures with gain for timing applications

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Abstract: Thanks to their advantages in terms of easiness of manufacturing and reduced production costs, Monolithic Active Pixel Sensors (MAPS) represent an appealing solution for radiation imaging applications, which require to cover large areas with pixelated detectors. In the next upgrade of the ALICE detector, that will have to deal with the higher event rate resulting from the planned increase in the LHC luminosity, it is foreseen to include two additional sensor layers to perform Time of Flight (ToF) measurements. Trying to reach the challenging timing resolution required by the ALICE ToF layers, an internal gain layer has been included in the test structures of the third engineering run of the ARCADIA project to improve the timing performance of this MAPS technology. In the paper we will present an overview of the main results obtained from the electrical and the dynamic characterization of the fabricated devices, which have been compared with the behavior expected from the preliminary TCAD simulations carried out in the design phase. The experimental results confirmed the feasibility of embedding a gain layer in the ARCADIA 110 nm CMOS technology to develop monolithic LGADs.

Keywords: Detector design and construction technologies and materials; Solid state detectors; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc)

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Contents

1 Introduction

For more than 20 years different collaborations have tackled the development of Monolithic Active Pixel Sensors (MAPS) to be employed in High Energy Physics experiments or in space and medical applications [1–5]. Two possible approaches have been followed in the detector design, leading to sensors with the embedded electronics implemented within large pixel collection electrodes [4, 6, 7] or to sensors having small collection electrodes surrounded by wells, where the front-end electronics can be hosted [3, 8].

In the ARCADIA collaboration this second approach was followed to develop a possible technology for the fabrication of fully depleted MAPS starting from the LFoundry 110 nm CMOS production process [9, 10]. Exploiting drift as main charge transport mechanism, the sensors implemented in this technology are able to provide good performance in terms of charge collection dynamics. Namely, fast charge collection times in the order of few ns have been measured on the produced passive pixel arrays with layouts designed to improve the charge collection speed and on large pad diodes implemented with the same technology [11, 12]. The ARCADIA sensors have been fabricated starting from high resistivity n-type substrates thinned down to nominal thicknesses of 100 and 200 µm or, alternatively, using a n-type epitaxial layer, having a nominal thickness in the order of 48 µm, grown on top of a highly doped p^+ substrate. The sensor n-type collection electrode and the surrounding pwell and deep pwell, where the front-end electronics can be hosted, were realized by ion implantation on the chip frontside surface. A continuous p-type implant was included on the backside surface of the 100 µm thick sensors to create the backside p-n junction. Instead, a dedicated backside lithography step was used to form the backside p-n junction and the guard rings designed to prevent the junction breakdown in the devices with 200 µm active thickness [13]. A surface n-type epitaxial layer, having a higher doping concentration than the n-type active volume, is present in all wafers. This layer delays the onset of the punch through current between the frontside and backside p-type regions and thus enables to reach the full depletion of the substrate, while allowing the sensors to be biased at low voltage.

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A significant increase in the event rate will be experienced by the sensors employed in the High Luminosity LHC, that is expected to provide an integrated luminosity about 10 times larger than the current one in the LHC [14]. As a consequence, in the related upgrade of the ALICE detector it is planned to include two new sensor layers able to perform Time of Flight measurements [15]. To enable particle identification and pileup rejection, a challenging requirement in terms of detector timing resolution, that should be lower than 20 ps, has been set for the sensors of the ToF layers of the ALICE 3 detector. Those sensors will also have to guarantee a moderate radiation hardness in terms of Non-Ionizing Energy Loss (NIEL) and Total Ionizing Dose (TID) in the order of 10^{13} 1 MeV n_{eq} cm^{-2} and 1 Mrad, respectively [15].

Hybrid sensors such as the traditional LGADs already proved to be able to reach the required detector performance showing timing resolution lower than 20 ps [16, 17] as well as good performance in terms of radiation hardness [18]. As an alternative, embedding a gain layer inside a MAPS represents a promising strategy to reach the required timing resolution, combining the advantages of monolithic detectors in terms of cost savings and lower noise levels w.r.t. hybrid detectors and the excellent timing performance of LGADs.

The PicoAD project proposed a possible solution to realize a monolithic LGAD developed on the basis of the Monolith project [19]. In the Picosecond-Avalanche Detector a continuous gain layer is realized between two p-type epitaxial layers, which represent the sensor absorption and drift regions, respectively. This leads to a continuous deep gain layer, which is completely independent from the pixel geometry and does not interfere with the surface implants [19]. However, the use of SiGe transistors in the embedded electronics and the dedicated production process steps needed to create the deep gain layer result in a customized CMOS technology, that complicates the technology transfer to a high-volume production line, and in an increase in the production costs.

This paper is structured as follows: the layout of the produced test structures with integrated gain layer is described in section 2; a summary of the electrical and dynamic characteristics of the passive pixel arrays with integrated gain layer is reported in sections 3.1 and 3.2, respectively; a comparison of the performance of the pixel matrices with different termination layouts is presented in section 3.3; finally, in the Conclusions we recall the main results of the performed characterization and we present the plan for the next production.

2 Device description

Monolithic LGADs were designed by including a gain layer in the modified CMOS technology developed within the ARCADIA project for the production of MAPS [20]. A p-type layer was implanted below the sensor n-type collection electrode to create a gain layer able to multiply the generated charges. The presence of the gain layer generates a localized electric field peak that exceeds the threshold value in the order of 2–5×10^5 V/cm required to trigger impact ionization in silicon. A positive voltage above 20 V has to be applied to the frontside n-type electrode to fully deplete the gain layer and to overcome this threshold value enabling the avalanche multiplication. As a consequence, the sensor nodes have to be AC coupled to the low-voltage preamplifier to enable the application of the bias voltage, in the order of tens of V, required for sensor operation [20]. The possibility to control the gain value and the signal dynamics tuning the bias voltages applied to the frontside collection electrode (V_n) and to the backside p-type contact (V_{bias}) independently represents another main difference with respect to traditional LGADs.

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To maximize the timing performance of the detectors, the size chosen for the pixels with gain was larger than the one typically used in conventional MAPS, in order to guarantee a fast and uniform charge collection thanks to the regular electric field shape. The tested matrices included rectangular or squared pixels having active areas equal to 250×100 μm^2 and 250×250 μm^2, respectively. To evaluate the effect of the pixel termination layout on the charge collection dynamics, we measured the signals of two passive pixel arrays having rectangular pixels with same pixel sizes but different layouts of the implants at the pixel borders, labeled as A1 and A2. Figure 1 shows the schematic cross-sections of two pixels having different termination layouts. In the rectangular pixels with layout A1 and also in the squared pixels with layout G1, shown on the left side, the deep pwells at the pixel borders extend until the sides of the gain layer implant. Instead, the pixels with layout A2 are characterized by the presence of a gap region between the two p-type implants.

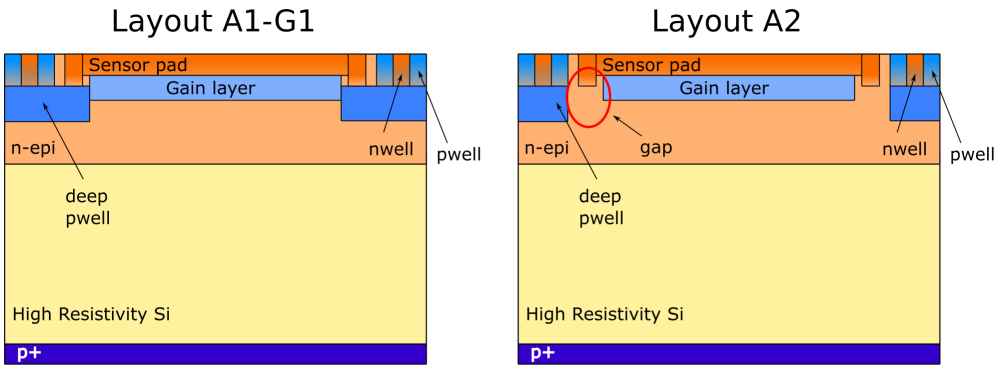

Figure 1. Schematic cross-sections of the pixels with gain having different termination layouts.

3 Characterization and simulation

3.1 Electrical characteristics

A micrograph of the measured pixel arrays is shown in figure 2, where the rectangular or squared pixel shapes can be clearly identified. The three structures present four electrodes on the chip frontside that, starting from the left-hand side, correspond to the frontside external pwell, to the n-type collection electrode, to the internal pwell and, finally, to the n-type guard ring.

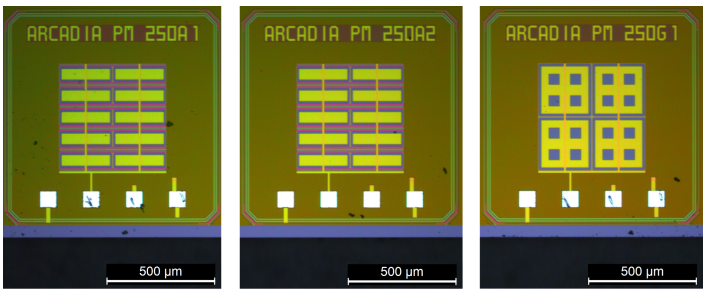

Figure 2. Micrograph of the tested passive pixel arrays with integrated gain layer having rectangular or squared pixel shape and different termination layouts.

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In these matrices the n-type collection nodes of the pixels are connected in parallel to a common readout electrode, where the frontside bias voltage (V_n) needed to trigger the avalanche multiplication was applied. The internal pwell electrode represents the ground reference in the performed measurements and, as a consequence, the pwell voltage was set to 0 V. Finally, the guard ring was biased at 8 V to collect the current diffusing from the semiconductor volume surrounding the tested structure.

We used a Keithley 4210A-SCS Parameter Analyzer connected to a probe station equipped with needle connectors to measure the IV and CV characteristics of the pixel arrays with integrated gain layer included on a group of dies extracted from the produced wafers. Figure 3A and figure 3B report the IV characteristics measured on two matrices with rectangular pixels having layout A1 applying a voltage sweep to V_n and V_{bias}, respectively.

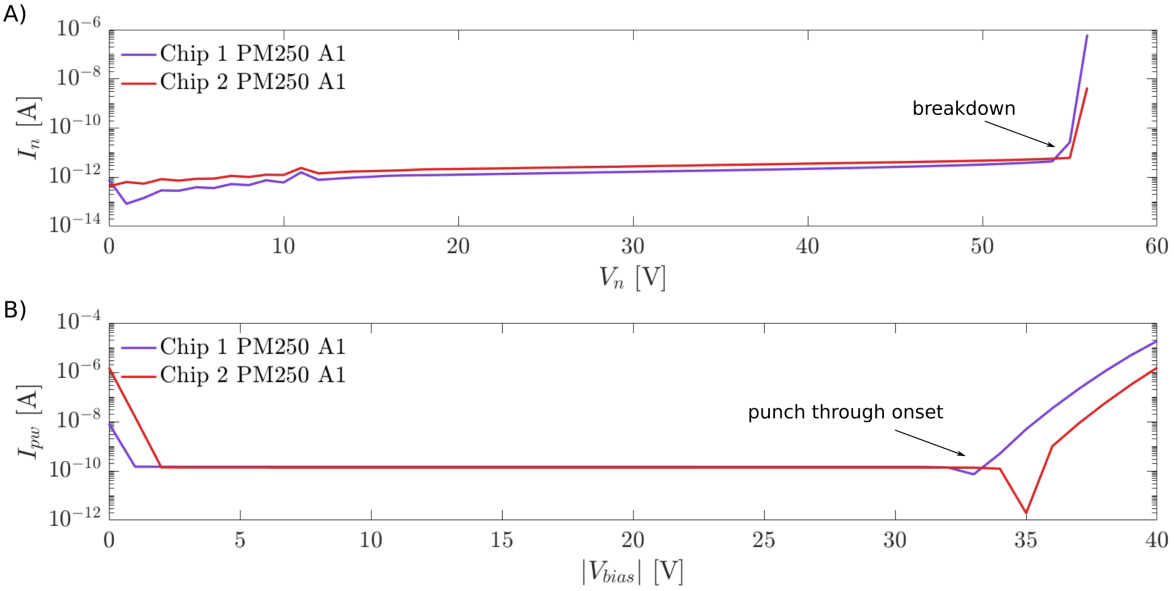

Figure 3. Pixel (A) and internal pwell (B) currents as a function of the applied V_n and V_{bias} measured on two passive pixel arrays with rectangular pixels with layout A1.

We extracted the frontside voltage related to the breakdown occurring at the borders of the frontside junction from the plot in figure 3A showing the variation in the pixel current for increasing V_n values. In an analogous way, we took as a reference the dips in the curves of the internal pwell current as a function of the applied V_{bias}, shown in figure 3B, to extract the backside voltage associated to the onset of the punch through (V_{PT}). The extracted breakdown voltages represent the upper limit to the voltage that can be safely applied to the frontside collection electrode for a correct device operation. On the other hand, negative voltages slightly larger than V_{PT} can be applied to the backside electrode, if the generated power can be dissipated efficiently, keeping under control the resulting increase in the device temperature.

3.2 Dynamic characteristics

The effect of the applied bias voltages on the signal dynamics and on the obtained gain value has been evaluated using an optical setup, where a group of wire bonded samples has been illuminated on the backside surface with a fast pulsed IR laser with 1060 nm wavelength, that can be focused in a

spot with a diameter in the order of 10 µm FWHM. The resulting pixel signals were amplified by a commercial external amplifier with 1.5 GHz bandwidth and 36 dB gain (Hamamatsu C5594) and, then, were acquired with a digital oscilloscope having 1 GHz bandwidth (Tektronix MDO3102).

The effects of the variation in the applied V_n can be observed in the two plots of figure 4, showing the signals measured on a matrix with squared pixels having layout G1 (figure 4A) and the corresponding amount of collected charges (figure 4B), computed as the integral of the acquired signals for a maximum integration time of 20 ns.

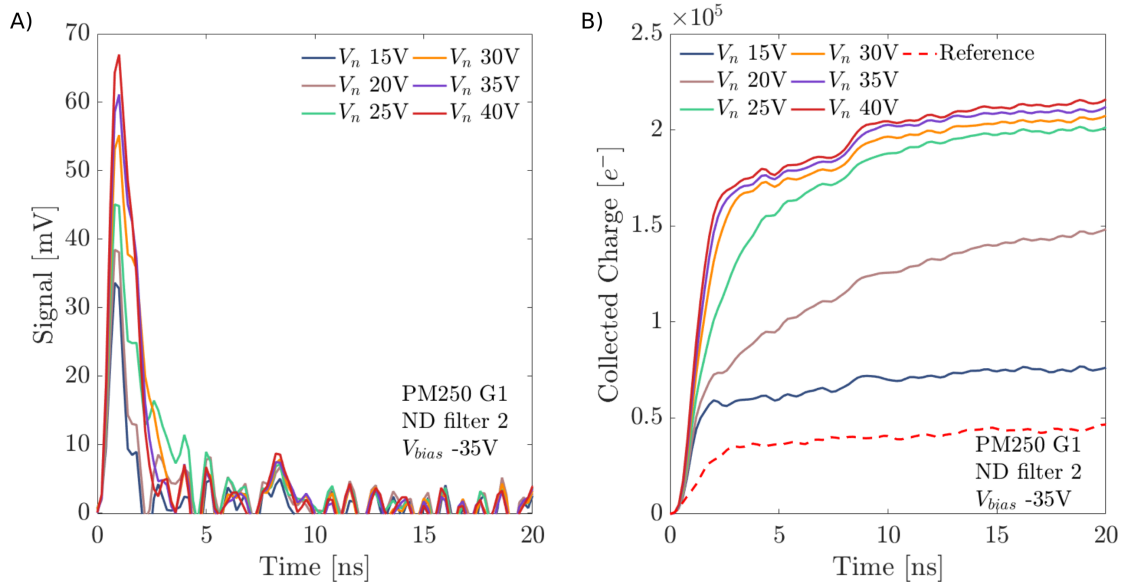

Figure 4. (A) Signals measured on a pixel matrix with layout G1 as a function of the applied V_n. (B) Collected charge as a function of the applied V_n.

According to figure 4A, increasing the applied V_n leads to higher and wider signal peaks. Namely, according to TCAD simulations, a higher frontside voltage creates a stronger electric field peak in correspondence of the gain layer and, therefore, improves the charge multiplication. The curves reported in figure 4B show that a frontside voltage above 20 V has to be applied before measuring a significant increase in the collected charge w.r.t. the one collected by a reference structure without gain. We used the ratio between the charge collected by the structure with integrated gain layer and the one collected by the reference structure to estimate the gain value. The gain values obtained measuring different structures belonged to a range of values between 2 and 4, which represented the best considered case for the matrix with squared pixels with applied V_n and V_{bias} equal to 40 and -35 V, respectively. However, due to the different IR-light reflectivity of the top-side surface, that depends on the layout of the metals at the frontside present in all the structures, the obtained gain values represented only a rough estimation of the actual gain value, that can be evaluated with a higher accuracy only in a test beam.

Figure 5 shows that a variation in the applied backside bias voltage had similar but less pronounced effects, which led to an increase in the signal peak amplitude and peak width for increasing V_{bias} values and, as a consequence, to an higher amount of collected charges. These results confirmed the expectations of TCAD simulations, proving that the signal dynamics and the gain value can be controlled by independently varying the applied V_n and V_{bias}.

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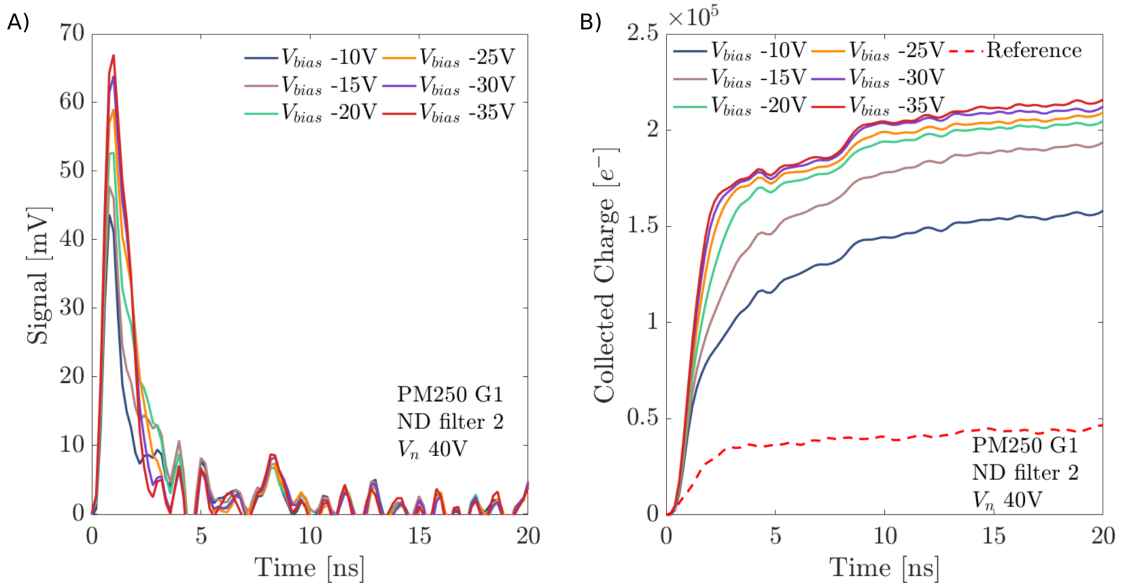

Figure 5. (A) Signals measured on a pixel matrix with layout G1 as a function of the applied V_{bias}. (B) Collected charge as a function of the applied V_{bias}.

3.3 Termination layout effects

Two different layouts have been designed for the terminations at the borders of the pixels with rectangular shape to evaluate which one could be the best option in terms of uniformity in the time response and in the charge multiplication within the pixel area. In the pixels having layout A1, due to the presence of a continuous p-type implant at the pixel borders, the charges generated in the pixel periphery are forced to flow through the gain layer and, as a consequence, are multiplied by impact ionization. This effect leads to a more uniform charge multiplication within the matrix area for the pixel arrays with layout A1. On the contrary, the presence of the gaps in the frontside p-type implants at the borders of the pixels with layout A2 guarantees a direct path to the n-type collection electrodes for the charges generated in the inter-pad regions. As a result, this speeds up the charge collection at the pixel borders, resulting in a more uniform time response within the matrix area. At the same time, the results of the TCAD simulations performed on 2D domains having pixels with border layout A1 or A2 predicted a lower charge multiplication at the pixel borders when the gap region was present. We reported in figure 6 the results of the simulations that were used to evaluate the charge collection in the border regions of the designed pixel layouts. In these simulations we employed 2D domains representing a cross-section of two neighboring pixels separated by an n-type guard ring, where the position of incidence of a monochromatic optical source having 10 µm width was varied along the domain surface to model the optical generation of charges in different pixel positions. Looking at the plot, it is possible to observe the effect of the different termination layouts on the simulated pixel charge collection. In the region surrounding the guard ring center, corresponding in the plot to the laser spot position equal to 0, the solid orange curve representing the sum of the charges collected by the two pixels with layout A1 is significantly higher than the dashed orange curve, which stands for the sum of the charges collected by the two pixels with layout A2.

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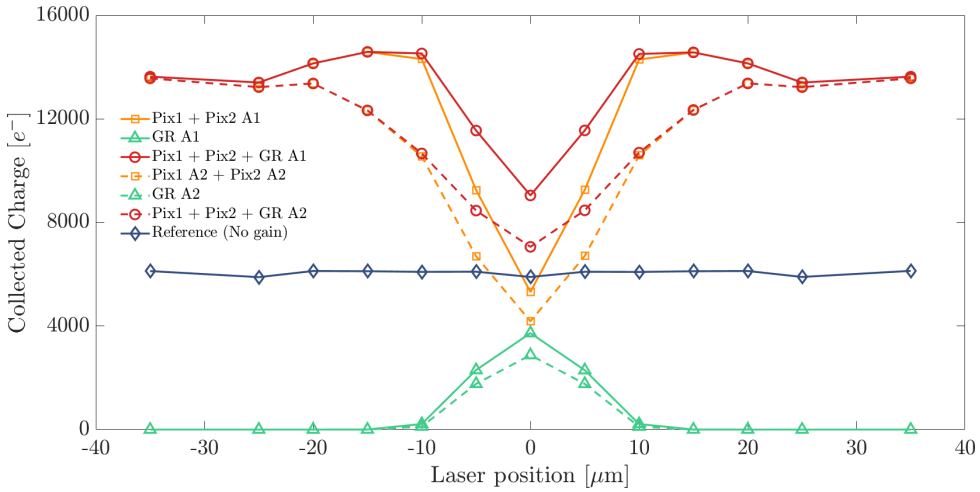

Figure 6. Charge collected by pixels and guard ring as a function of the position of incidence of the laser spot on the TCAD simulation domain.

To validate the results of TCAD simulations, we scanned the laser position on two matrices with pixel layouts A1 and A2, where we acquired the pixel array signals for different position of incidence of the focused IR laser spot controlled through the combined action along x and y directions of two step motors mounted in the optical setup. The obtained signal maps represented the response of the pixel array on a scan area of 350×350 μm^2 with a spatial resolution equal to the employed motor step size of 5 µm. Computing the integral of the acquired signal maps, we obtained the maps showing the amount of charges collected as a function of the laser spot position, that are reported in figure 7A and in figure 7B for the pixel arrays with layout A1 and A2, respectively.

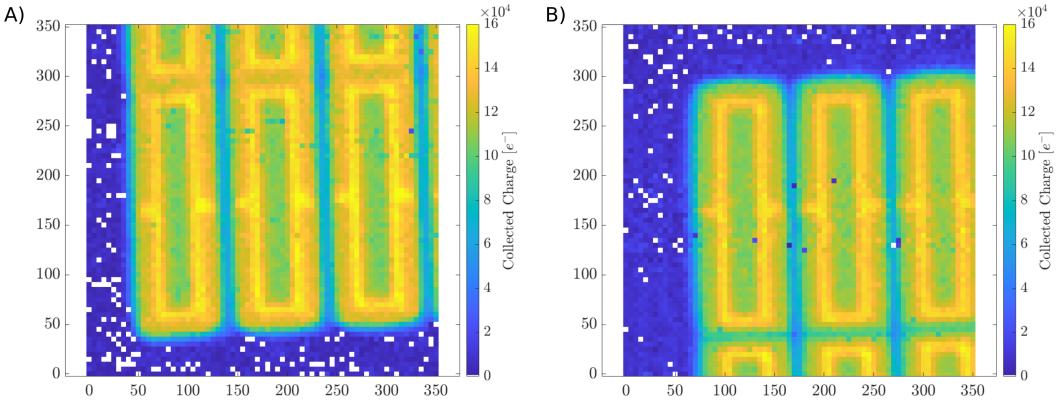

Figure 7. Signal integral maps for the passive arrays with rectangular pixels having layout A1 (A) and layout A2 (B).

Looking at the maps, it is possible to identify the position of the pixel collection electrodes corresponding to the yellow and green regions. In an analogous way, the light blue regions represent areas where the inter-pixel regions are covered by guard rings, which collect part of the generated charges. The non-uniform charge collection within the sensor pad regions is related to the back-reflection of the IR light due to the presence of the frontside metals and frontside contacts having different reflectivity and, thus, resulting in a non-uniform charge generation.

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Considering a horizontal cut plane parallel to the x-axis, we extracted the cross sections of the signal integral maps, that are reported in figure 8, showing the variation in the charge collected by the pixels changing the position of incidence of the laser spot along the x-direction. As expected from TCAD simulations, the profile extracted from the signal integral map of the matrix with layout A1 showed a higher charge collection at the pad borders due to the improved multiplication of the charges generated in those regions.

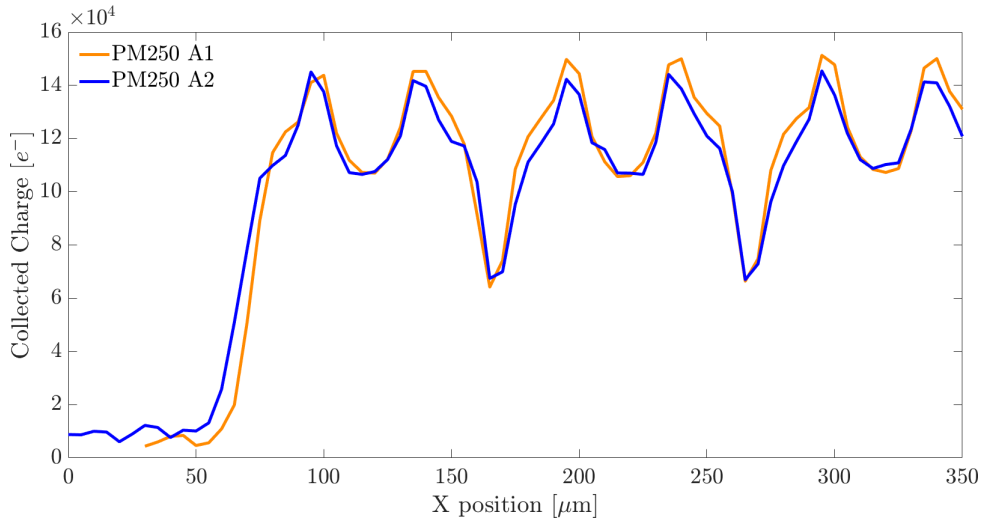

Figure 8. Signal integral profiles extracted from a horizontal cut-plane parallel to the x-axis in the signal integral maps.

In an analogous way, we created the maps reported in figure 9 showing the time needed to reach 50% of the signal rising edge ($t_{rise_{50}}$) for the two considered pixel arrays. Again, the experimental results confirmed the behavior expected from TCAD simulations, showing a more uniform time response within the area of the matrix with layout A2 and a significantly slower signal dynamics in the inter-pad regions of the pixel array with layout A1.

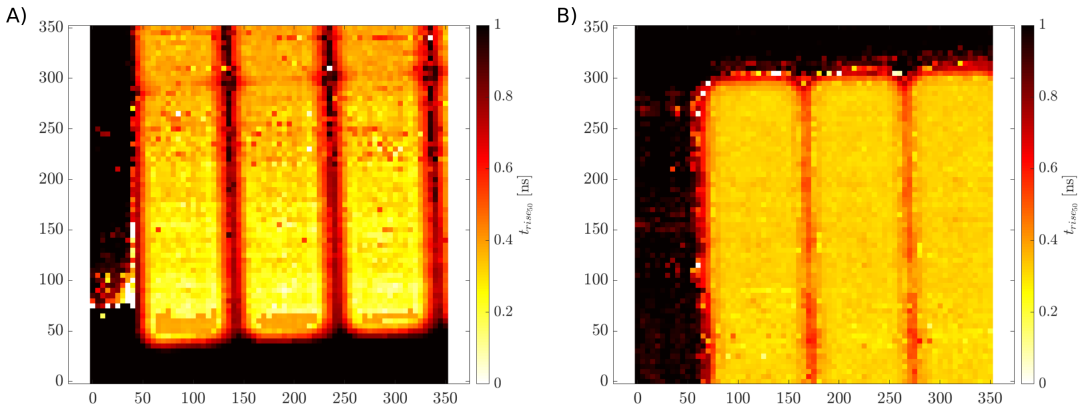

Figure 9. Rising edge maps for the passive arrays with rectangular pixels having layout A1 (A) and layout A2 (B).

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Considering the same horizontal cut plane employed previously, we compared in figure 10 the extracted profiles showing the variation in the $t_{rise_{50}}$ along the x-direction for the two pixel layouts. Looking at the curves, we can clearly notice the lower variability in the extracted $t_{rise_{50}}$ for the pixel array with layout A2 presenting a gap in the p-type implants at the pixel borders and, instead, $t_{rise_{50}}$ results more than doubled at the pixel borders in the matrix with termination layout A1.

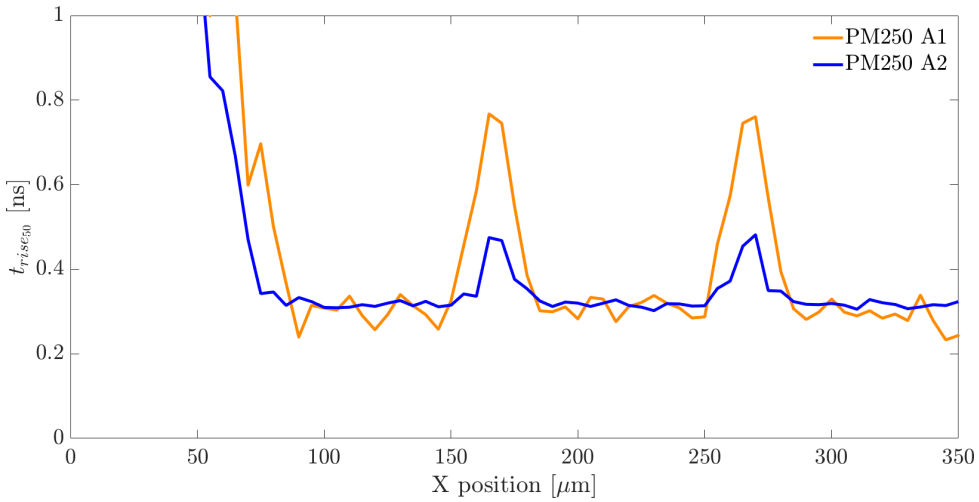

Figure 10. Rising edge profiles extracted from a horizontal cut-plane parallel to the x-axis in the rising edge maps.

4 Conclusions

In this paper, we presented the results of the electrical and the optical characterization of a group of MAPS test structures with integrated gain layer. The measurements proved the feasibility of integrating a gain layer within the sensor technology developed in the ARCADIA project. The charge collection dynamics and the gain value were measured on a group of structures with different pixel layouts as a function of the voltages applied to the frontside and backside contacts, reaching a maximum gain value around 4 in the best case. Different layouts of the terminations at the pixel borders were designed by means of TCAD simulations. We evaluated experimentally their influence on the uniformity in the charge multiplication and on the signal dynamics performing scans of the matrix areas with a focused IR laser spot, which confirmed the behaviors expected from the preliminary TCAD simulations. We will exploit the acquired experience to select the pixel layouts and to tune the gain layer implant in order to further improve the performance of the MAPS test structures that will be included in the next production foreseen for 2024.

Acknowledgments

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