Design and Characterization of 10 Gb/s and 1 Grad TID-Tolerant Optical Modulator Driver

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***Abstract*— This paper presents the design and the experimental characterization of a 10 Gb/s electronic driver for silicon Mach-Zehnder modulators (MZMs). This driver is able to operate in harsh environments characterized by radiation levels up to 1 Grad(SiO_2) total ionizing dose (TID). To compensate for the detrimental effects that radiation produces on the target 65 nm bulk silicon technology both device- and circuit-level radiation hardened by design (RHBD) techniques are developed and implemented. Extreme TID levels are faced using long-channel transistors with enclosed layout, avoiding the use of p-MOSFETs, and implementing a differential self-biased cascode architecture with common-mode feedback. Band-widening techniques, e.g., inductive peaking, cross-coupled capacitors, and buffer chaining, have been used to improve the driver's frequency response and reach the targeted data rate. Electrical measurements show 10 Gb/s waveforms with an eye diagram amplitude suitable for MZM driving. Electro-optical measurements performed connecting the electronic driver to a silicon photonic MZM confirm the achievement of a 10 Gb/s system-level operability. The radiation hardness of the driver is verified by exposing the integrated circuit to X-rays. The measurements confirm the ability of the driver to work up to 1 Grad with an eye amplitude reduction of only 10% and a 7% increment in the rise and fall times, validating the effectiveness of the implemented RHBD techniques.**

***Index Terms*— High-speed optical communication, radiation hardened by design, CMOS integrated circuits, silicon photonics.**

I. Introduction

THE upgrade of the current Large Hadron Collider (LHC) at CERN, also known as High Luminosity LHC (HL-LHC), requires electronics to reliably detect particle properties, manage the collected experimental data and transmit it to the processing sites. Given the harsh conditions determined by particle collision outcomes, all the electronic subsystems must guarantee a robust operation against radiation damage. Radiation levels can indeed reach up to 1 Grad(SiO_2) of total ionizing dose (TID) in the innermost detector shells [1]–[3].

LHC experiments currently exploit optical links to read out the data produced by the various sensors deployed in the detector. Fiber optic-based links enable low-power and high-speed data transmission, allowing, at the same time, a substantial mass and footprint reduction compared to aluminum- or copper-based alternative solutions. Material budget is indeed a critical metric for high energy physics (HEP) systems since every spurious interaction with the surrounding environment may affect the ability to precisely reconstruct particle trajectories [4].

Tens of thousands optical links based on vertical-cavity surface-emitting lasers (VCSELs) are already installed in the experimental caverns together with the driving electronics needed to convert the electrical signals coming out of the particle sensors into modulated optical waves. However, VCSEL components have been shown to be strongly sensitive to radiation effects. Radiation-induced atomic displacement damage is indeed responsible for a progressive degradation of the laser performance metrics, e.g., threshold current [5]. This phenomenon leads to device failures even at doses far lower than those required by the HL-LHC upgrade [2], [3]. Therefore, state-of-the-art electro-optic transceivers, e.g., VTRx+ [6]–[12], are limited in their usage only to regions of the detector which are relatively far from the particle beams interaction point, i.e., where the radiation exposure is not prohibitive for VSCEL devices [5]. Sensors located close to the beamline, e.g., silicon pixel detectors, are thus still being accessed with bulky copper cables, affecting material budget, speed, and density scalability.

In the last years, devices based on silicon photonics (SiPh) technology, such as Mach-Zehnder modulators (MZMs) and ring modulators (RMs), have been reported to have stronger radiation hardness than VCSELs, promising radiation tolerance levels in line with the next HEP experiment upgrades [13]–[19]. SiPh-based optical links able to withstand up to 1 Grad(SiO_2) are indeed one of the most promising solutions for data transfer in HL-LHC experiments, in order to deploy them down to the innermost detector layers [2]. The design of 1 Grad(SiO_2) tolerant high-speed electronic drivers for optical modulators is thus of paramount importance to support the transition to silicon-based integrated photonic devices inside the electro-optical conversion units.

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The work presented in this paper is the direct upgrade of the previous design presented in [20], where two 5 Gb/s electronic drivers, respectively designed for RMs and MZMs, were able to work up to 800 Mrad TID while losing at most 30% in their output voltage swing. Extending the previous work, this driver can operate to a doubled bit rate, i.e., 10 Gb/s, thanks to an improved modeling of the load and an extensive usage of circuit solutions to extend the operational bandwidth, e.g., inductive peaking and cross-coupled capacitors. In addition, the implementation of circuit-level radiation hardened by design (RHBD) techniques allowed us to achieve higher radiation levels, i.e., 1 Grad(SiO_2), with better performances.

After a general introduction about the radiation effects on the target 65 nm technology, a discussion regarding device-level RHBD techniques is reported in Section II. The design procedure that leads to the radiation-hard driver realization is described in Section III, while a further technique for radiation hardness improvement is proposed in Section IV. The following sections, i.e., Sections V and VI, respectively, deal with the driver layout and the report of the experimental electrical, electro-optical, and radiation characterizations. Conclusions are then drawn in Section VII.

II. Radiation Impact and Device Level RHBD Techniques

Radiation effects on silicon technologies are mainly related to the thickness of oxide layers. TID-induced effects, i.e., positive charge generation and transport in insulating layers, indeed go as the square of the oxide thickness [21]–[24]. Metal-oxide-semiconductor field-effect transistors (MOSFETs) available in the selected technology are characterized by a 2 nm-thick gate oxide, which would suggest a strong resistance to radiation damage. However, at extreme levels of absorbed ionizing dose, charges generated in the insulating regions that surround the MOSFET channel start to play a major role. The presence of shallow trench isolations (STIs) and gate spacers indeed drastically reduce the performance of the transistors. For example, minimum-sized n- and p-MOSFETs connected in diode configuration suffer a reduction in their on-state current respectively of 52% and 98% after 1 Grad(SiO_2) TID exposure [25]–[28]. Therefore, RHBD techniques must be adopted to face these detrimental effects and extend the operability of MOSFET devices in environments pervaded by radiation [29]. In particular, the usage of p-MOSFETs should be avoided since radiation-induced positive charges accumulated in the oxide layers generate an electric field that repulses the p-MOSFET conductive charges, making these devices more sensitive to radiation. Moreover, the usage of longer-channel transistors helps in reducing the impact of charges accumulated in gate spacers. Nevertheless, a trade-off between speed and radiation resistance inevitably arises since channel length is inversely proportional to MOSFET's cut-off frequency. Then, to reduce the impact of charges trapped in STI trenches, enclosed layout transistors (ELTs) should be used to avoid by design any interface between MOSFET channels and isolation oxides [30]. All these device-level RHBD techniques are adopted in the driver's design for radiation hardness improvement.

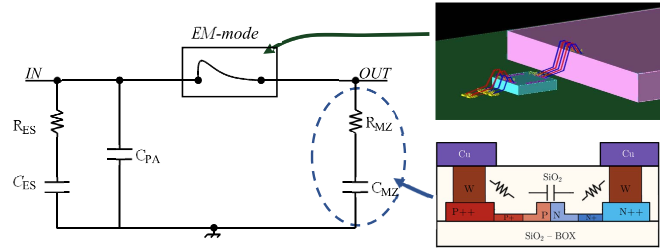

Fig. 1. Schematic of the equivalent single-ended loading model. The top-right detail shows the chip-to-chip coupling configuration used for electromagnetic simulations of the bonding wires. The bottom-right detail shows a simplified section of one of the two SiPh-MZM arms.

III. Driver Design

A. Output Load Modeling

One of the fundamental design steps is the modeling of all the elements that will be connected to the driver, such as electrostatic discharge (ESD) protection circuits, chip pads, bond wires, and electro-optical modulators. A schematic of the loading model is shown in Fig. 1. The ESD protections used in this work are based on diode-triggered silicon-controller rectifiers [31], [32] and are designed to be compliant with the 2 kV human-body model and 500 V machine model. They were reused from previous projects since they have already been qualified for sustaining high radiation doses. Their impact on the driver design was modeled with an equivalent series impedance, composed by a resistance and a capacitance whose values were obtained from post-layout parasitic extraction, respectively $R_{ESD} = 1.8\ \Omega$ and $C_{ESD} = 350$ fF. A 50 fF capacitance (C_{PAD}) is placed in parallel to the ESD equivalent model to represent the impact of $50 \times 70\ \mu m^2$ pads. Pad capacitance value, also extracted with post-layout simulations, results to be mainly determined by the capacitive effects between overlapping metals, i.e., between the top metal layers exploited for the pad itself and the lower metal layers used for the low-resistance ESD paths. These paths are used by the ESD protection circuits to distribute the charge caused by electrostatic discharge toward the power clamps protections [33], [34]. The bond wires were modeled using an electromagnetic simulator to convert connection wires into an electrical model. Direct coupling between the electrical chip hosting the driver and the SiPh chip hosting the MZM is assumed as a study case (see top-right detail in Fig. 1). The wire bonding simulations are performed considering a higher thickness of the SiPh chip than the electronic one, in agreement with the experimental setup which will be described in Section VI. The pads of the two chips are arranged with a 100 μm-pitch in GSGSG configuration, where G stands for ground and S for signal.

The MZM is an optical modulator that relies on an interferometric working principle [13]. A beam of light travelling in an integrated silicon waveguide is split in two parts and routed through two different electro-optic phase modulators. By recombining the two beams, the output optical power will

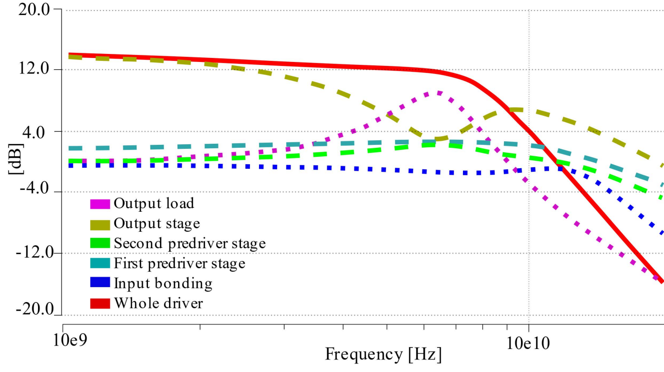

Fig. 2. Frequency response of every single stage, the load network, and the whole driver obtained using Harmonic Balance simulations.

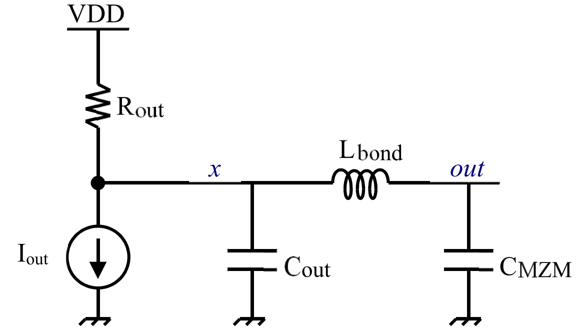

Fig. 3. Simplified model of the output load and of the output stage without the inductive peaking (introduced in the next section).

depend on the phase difference between them. By driving the phase shifters accordingly, e.g., differentially, is thus possible to achieve an optical amplitude modulation out of the MZM, and thus encode a bitstream on the optical carrier wave. High-speed electro-optical phase shifters are realized in SiPh by embedding a pn-junction inside an integrated optical waveguide and driving it in reverse polarization. The MZM targeted in this work presents 1 mm long phase shifters characterized by a modulation efficiency of $V_\pi \cdot L_\pi = 1$ V·cm. This latter quantity corresponds to the voltage V_π that should be applied to an arm having length L_π to produce a phase shift of π radiant. Considering that the targeted MZM has 1 mm long phase shifters, the voltage required to achieve a fully destructive interference would be $V_\pi \sim 10$ V.

Considering the modulation speed required by the application and the footprint of the devices to be driven, it is sufficient to consider the MZM as a lumped device Concerning the driver design, the pn-junction of the optical modulator can thus be modelled as a series impedance made of a capacitance to represents the depletion region and a resistive contribution associated with the pn-junction access paths (see Fig. 1 bottom-right detail) [35]–[38]. Considering the targeted MZM device, we used $C_{MZM} = 500$ fF and $R_{MZM} = 1.8\ \Omega$ for the model. Since the driver differentially drives the two MZM arms, Fig. 1 only reports the single-ended loading condition applied to each of the driver's output nodes.

The contribution of pads, ESD structures, bonding wires, and photonic modulator have been included in the model, determining a transfer function characterized by a significative +9.3 dB peak located at 6.3 GHz, followed by a rapid roll-off at higher frequencies. Then, the ±3 dB bandwidth of the load network is located around 4.5 GHz, which imposes the adoption of compensation mechanisms on the driver side to target the 10 Gb/s bit rate.

Fig. 2 reports the frequency response of the output load (pink dotted line) together with all the other stages' frequency responses, which will be commented in the next sections.

To give an intuitive explanation for the frequency responses of the output load and the driving circuit, a simplified circuit (shown in Fig. 3) can be used to carry out handily equations for design purposes. A successive simulating phase is required for the proper stage sizing.

The output load frequency response is indeed characterized by the interaction between the MZM and the bonding equivalent model. Considering the simplified model in Fig. 3, we obtain the following transfer function, whose variable names are the same as those in Fig. 3:

$$\frac{v_{out}}{v_x}(s) \approx \frac{1}{L_{bond}C_{MZM}s^2 + 1} \tag{1}$$

that has two conjugate poles placed at a pulsation equal to:

$$\omega_{p,1-2} = \frac{1}{\sqrt{L_{bond}C_{MZM}}} \tag{2}$$

which are well observable in the output load behavior reported in Fig. 2 (pink dotted line). Note that this behavior is independent of the driver design.

On the other hand, the frequency response of the output stage, reported by the dashed yellow line in Fig. 2, can be explained considering that the output response of the model in Fig. 3 is given by the product between the equivalent driving stage transconductance ($G_m = I_{out}/V_{in}$) and the load made by the parallel connection between the driver's output resistance (R_{out}) and the actual load impedance (Z_x, seen on the right side of the node x in Fig. 3):

$$H(s) = G_m\left(\frac{R_{out} \cdot Z_x}{R_{out} + Z_x}\right) \tag{3}$$

The frequency behavior of Z_x is reported below:

$$Z_x(s) \approx \frac{1}{C_{out}} \cdot \frac{s^2 + \frac{1}{L_{bond}C_{MZM}}}{s\left(s^2 + \frac{C_{out} + C_{MZM}}{L_{bond} \cdot C_{out}C_{MZM}}\right)} \tag{4}$$

Describing the frequency behavior of eq. (4) from low frequency to high frequency, we can observe:

- a pole in the origin that generates a −20 dB/decade roll-off for low frequencies. Being Z_x in parallel to R_{out}, the R_{out} dominates the response for low frequencies so this pole cannot be observed in Fig. 2.
- a pair of conjugates zeros placed at:

$$\omega_{z,1-2} = \frac{1}{\sqrt{L_{bond}C_{MZM}}}.$$

They generate the yellow line drop at 6.3 GHz in Fig. 2. To be noticed that these zeros are placed in the same position as the output load poles.

- a pair of conjugate poles placed at:

$$\omega_{p,1-2} = \frac{1}{\sqrt{L_{bond}\left(\frac{C_{out}+C_{MZM}}{L \cdot C_{out} C_{MZM}}\right)}},$$

which generate a peak around 8.5 GHz. This peak has a lower value than that shown in Fig. 2, because in the complete design, the inductive peaking technique is introduced in the pull-up impedance to increase this peak and thus mitigate the overall frequency response (see Section III-B).

B. Output Stage

The MZM requires quite large voltage driving to modulate the optical carrier wave. Considering that the targeted MZM device has a $V_\pi \sim 10$ V, a voltage swing on the order of 2 V per arm is chosen to obtain an Extinction Ratio (ER) of nearly 2.5 dB, which is compatible with the modulation performances required by the final application [9]. For this reason, a supply voltage higher than the maximum supported by the standard devices (also called "core" devices), i.e., those provided with the technology process design kit (PDK), should be provided to the last driving stage. According to the RHBD guidelines introduced in Section II, this increased voltage stress on the electronic devices could not be addressed with the usage of thick-oxide MOSFETs to avoid trading off with radiation tolerance. Hence, a cascode architecture, composed of a common-source (CS) and a common-gate (CG) stage, has been chosen for the last driver stage, as shown in Fig. 4. Considering the 10 Gb/s target data rate and the required voltage swing to drive the MZM, two 50 Ω pull-up resistors and 50 mA tail current are adopted in the output stage. To sustain this current level wide MOSFETs are employed, i.e., 828 μm wide devices for the CS couple and 1248 μm wide for the CG ones. Then, as described in Section II, device lengths longer than the minimum allowed by the technology node were chosen to address the effect of charge accumulated in MOSFETs' spacers. Channel lengths equal to 120 nm have thus been adopted for the high-speed devices as a trade-off between speed and radiation hardness. The choice comes from the evaluation of the overall circuit performances by harnessing the MOSFET model reported in [20], which was guaranteed till 1 Grad. It is based on the Berkeley Short-channel IGFET Model whose parameters are changed according to the characterization data of 65 nm MOSFETs exposed up to 1 Grad [29].

In a common cascode configuration, as sketched in Fig. 4(a), the sustained voltage is not equally distributed on both the transistors [39]. Indeed, the time-domain simulation of the cascode architecture reported in Fig. 5 shows that 73% of the voltage swing falls on the drain-source voltage (V_{DS}) of the CG transistors and 27% on the CS one. The voltage unbalance can be observed also on the drain-gate junctions, making the CG drain-gate voltage drop (V_{DG}) the limiting factor for the output signal swing. The maximum CS V_{DG} is about half of the maximum CG V_{DG} (i.e., 58% of CG V_{DG}).

In addition, considering that the splitting efficiency of radiation-induced electron-hole pairs depends on the electrical field intensity [22], the higher the V_{DG} voltage and the heavier will be the radiation effects on the transistor. Therefore,

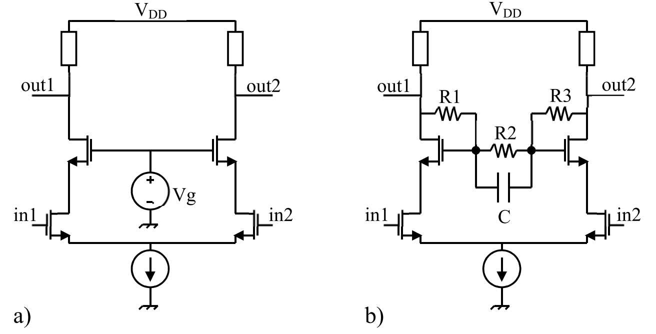

Fig. 4. Schematics of cascode output stage architectures: (a) Standard cascode biasing, (b) Differential self-biased cascode.

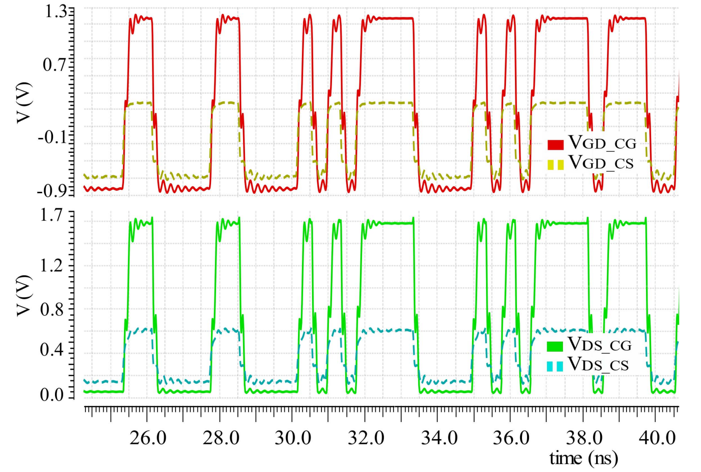

Fig. 5. Time-domain simulation results of the GD and DS junction voltages on the standard cascode stage shown in Fig. 4(a).

a reduction of the V_{DG} will generate benefits not only in terms of output swing and junction breakdown but also in the overall circuit radiation hardness. To balance the voltage sharing between the cascode devices a self-biased differential cascode architecture is then proposed for the output stage of the driver. As shown in Fig. 4(b), three resistors and a capacitor are added to the conventional architecture. For low frequencies, the self-bias structure allows us to modulate the voltage on the CG gate with a partition of the output voltage given by $(R_2/2)/(R_1 + R_2/2)$. Higher frequency components are attenuated by the low-pass nature of the R-C network, which generates a pole at a pulsation equal to:

$$\omega_{sb} = \frac{R_1 + \frac{R_2}{2}}{R_1 \cdot \frac{R_2}{2} \cdot \frac{C}{2}} \tag{5}$$

The resistors and capacitor values can thus be chosen to balance the V_{GD} between the CG and CS. In the proposed driver, the CG gate is fed with one-third of the output voltage and the frequency pole is fixed to one-fifth of the driver bandwidth. With these values, a fairer voltage sharing is achieved, as shown in the time-domain simulations of Fig. 6, without affecting the overall driver frequency response.

The differential self-bias architecture indeed enables 55% of the output voltage swing to fall on the CG V_{DS} with the

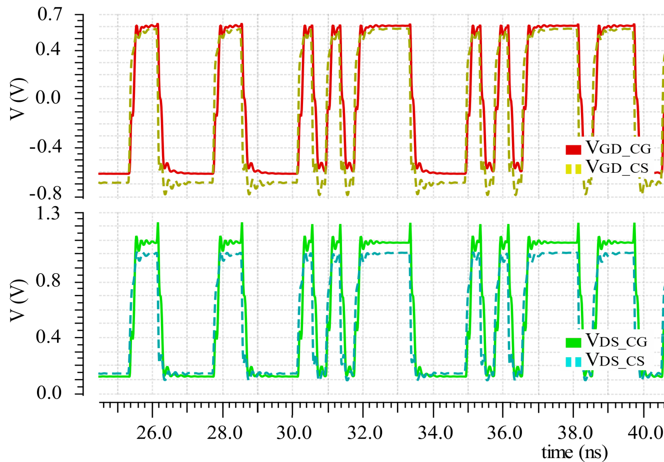

Fig. 6. Time-domain simulation results of the GD and DS junction voltages on the differential self-biased cascode stage shown in Fig. 4(b).

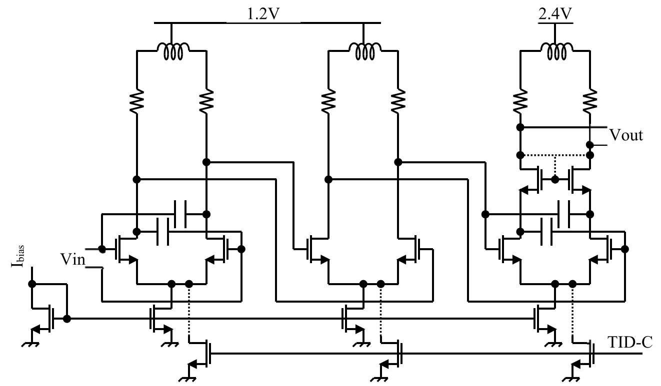

Fig. 7. Schematic of the whole proposed driver composed of an output stage and two predriver stages. The additional biasing tails connected to the net labeled "TID-C" is part of the TID countermeasure described in Section IV.

remaining 45% on the CS one. At the same time, the V_{DG} voltages of the cascode internal stages have become approximatively equal (i.e., CS's V_{DG} is about 93% of the CG's V_{DG}). Therefore, this circuit solution is expected to mitigate both junction breakdown issues and radiation hardness.

Concerning the frequency response, the output stage is equipped with an inductive peaked 50 Ω pull-up network [40]–[43]. Being aware of the output load transfer function, the inductor has been chosen to achieve a maximally flat response for the overall driver. As shown in Fig. 2, the peak in the frequency response belonging to the output stage indeed generates a +9.5 dB peak around 9.5 GHz which partially compensates for the load roll-off at higher frequencies.

C. Predriver Stages

The wide-sized MOSFETs used in the output stage present a huge input capacitance that imposes the introduction of a few pre-driving stages to handle it. A tapered current-mode logic (CML) chain composed of two elements has thus been chosen to pre-drive the output stage. The two cells have been designed with a scale factor equal to 3, unlike the commonly used factors of 2 or 2.7. In particular, MOSFET widths of 85 μm and 262 μm have been adopted for the first and second predriver stages, respectively. A higher scale factor indeed helps in reducing the number of stages but has the drawback of also decreasing the overall bandwidth [40], [41], [44]–[45]. To cope with this bandwidth reduction, other broad-banding techniques have been adopted. Inductive peaking is introduced in the output stage as well as in both pre-driver stages. It helps in shaping the driver's frequency response to partially compensate for the rapid drop of the output load frequency response after the 6.3 GHz peak (see Fig. 2). The placement of the frequency response peaks and their amplitudes depend on the inductor values, the pull-up resistances, and the output node capacitances of each cell. Since in a traditional buffer chain, the value of the pull-up resistors and the node capacitances are imposed by the scale factor, the inductor choice remains the unique degree of freedom to shape the device's frequency response. To precisely tune the position and the amplitude of the peaks, we thus decided to introduce an additional circuital solution to modify the output node capacitances. Cross-coupled capacitances have thus been inserted between input and output nodes of critical stages, as sketched in Fig. 7. This connection determines an equivalent negative capacitance that goes in parallel with the intrinsic gate impedance, effectively reducing the stage's input capacitance. This is intuitively related to Miller's effect applied to a capacitance placed across a positive gain stage [40], [41].

Generally, extensive usage of this technique is quite discouraged because the input capacitance reduction happens at the expense of an output capacitance increase of the stage where it is applied. Indeed, in the proposed design only a minimal cross-coupled capacitive adjustment has been implemented on the first pre-driver stage and the output stage, i.e., 40 fF capacitances have been selected for the former while the latter is equipped with 100 fF. These choices allowed to reduce the input capacitances of 40% and 11%, respectively.

Then, the inductive peaks have been set at the desired frequency position and amplitude by using 1.3 nH and 600 pH on-chip inductors for the first and second pre-driver cells, respectively. The tail currents of the predriver stages are 8.7 mA and 20.2 mA for the first and the second one, respectively.

IV. RADIATION DETECTION AND CORRECTION

The exposure of the target 65 nm technology to high ionizing doses has several effects on the active devices used to design the driver, e.g., threshold voltage shifts and leakage current increase [21]. Few RHBD techniques related to single-device engineering have already been reported in Section II. In this Section, a circuit-level approach is introduced as a counteracting mechanism to further increase the driver's radiation hardness when exposed to extreme TID levels. Assuming that the amount of dose accumulated on the whole electronic chip is uniform, we propose a design strategy that detects radiation-related effects on a dedicated region of the chip and then automatically compensates for the generated impairments on all the other devices distributed on the chip. In other words,

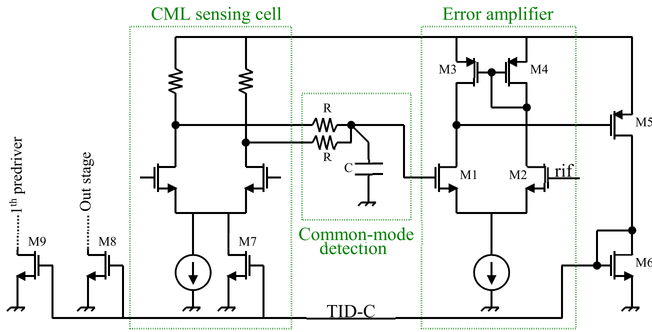

Fig. 8. TID compensation system composed of a CML sensing cell, a common-mode detection system, and an error amplifier. The transistors on the left are the additional current tails connected to the "TID-C" net of the driver's stages depicted in Fig. 7.

it consists of the design of an indirect radiation-damage sensor to locally counteract device performance degradation.

According to the large-signal analysis of a CML cell, the output swing depends on the product of the tail current and the pull-up resistors. Considering the higher impact that TID has on active devices than passives ones, the signal amplitude reduction at high doses could then be mainly attributed to a bias current reduction rather than a variation in the resistance values. The idea then relies on a compensation mechanism that acts on the bias current of the driver's stages whenever the output amplitude starts to reduce because of radiation exposure. In order to sense the radiation-induced swing reduction, we recall that the output common-mode of a CML cell can be expressed as:

$$\mathrm{V_{o_{cm}}}=\mathrm{V_{DD}}-\frac{\mathrm{I_{tail}}}{2}\cdot\mathrm{R_L} \tag{6}$$

where V_{DD} is the supply voltage, R_L is the pull-up resistor and I_{tail} is the tail current of the cell. Being a function of the cell's bias current, the detection and control of the output common-mode can be used to partially compensate for the TID effects.

The circuit depicted in Fig. 8 is thus implemented for this purpose. It is composed of a CML cell that is used as a sensing element and an error amplifier which generates an additional current bias for the driver stages, with the appropriate current mirroring ratios (cross-check Fig. 7 and 8). In particular, the second stage of the pre-driver is used itself as the sensing element to save on area and power consumption. Its output common-mode voltage is easily detected by an RC network with a large time constant. TID is indeed a timely slow disturb, e.g., the declared 1 Grad(SiO_2) accumulated dose for LHC experiments is forecast to be collected after at least ten years of operating time.

Then, the error amplifier is employed to compare the detected value with a reference voltage externally provided. This amplifier is an n-couple differential amplifier with active load. The error amplifier output is then used to drive a current mirror feedback, which increases the tail current of the sensing CML cell and that of the other CML stages of the driver. Although p-MOSFET devices are heavily affected by TID, as described in Section II, their use is allowed for low-frequency applications where long and wide devices can be adopted.

The usage of a single CML structure to sense the TID effects of the overall circuit with different MOSFET sizes is justified by the relationship between TID and the MOSFETs sizes. Each MOSFET parameter (e.g., transconductance, threshold voltage, etc.) has typically a different dependence with respect to TID and the device's width/length sizing according to the measured data reported in the literature [21]–[30]. However, since MOSFET devices used for the driver circuit have short channel lengths and wide widths, the following considerations can be made:

- For n-MOSFETs with a width wider than 30 μm, the dependence of the related losses due to TID from the device width is negligible. Therefore, for example, since there is a linear relationship between the MOSFET width and the on-current, the absolute current variation due to TID has a linear dependence with the MOSFET width.
- Concerning the MOSFET length, it has a strong impact on the performance of devices exposed to TID. In particular, the dependence of the device length on the TID effects is well observed for some MOSFET parameters, such as threshold voltage, drain-induced barrier lowering, mobility, offset voltage, sidewall current, and subthreshold swing factor. There is no linear relationship between the TID effects on these parameters and the length of the devices, but each parameter has its own relationship that can be extracted by interpolating data from the literature [21]–[30], as performed in [29].

Therefore, the usage of the second stage of the pre-driver as a sensing element is justified because it is designed with the same channel lengths of all the other MOSFETs in the circuit, while the different device width is compensated by the appropriate choice of current mirror ratios in the feedback circuit.

Concerning the feedback stability of the TID compensation system shown in Fig. 8, the dominant pole is obtained by the RC network used for the common-mode detection and the input capacitance of the error amplifier. It is located at 7.8 MHz obtaining a phase margin of 98° and a gain margin of 25.5 dB. Conservative stability margins are adopted to consider an eventual pole shift due to the high TID doses. The whole area and power consumption of the implemented TID compensation technique are about 0.012 mm^2 and 2.6 mW, respectively.

In Table I are listed the sizes of the error amplifier and of the common-mode detection block involved in the TID compensation system. Considering the lower speed requirements of this sub-circuit, the MOSFET lengths within this block have been made longer than those chosen for the main driving stages, reducing the TID effects on this block.

V. Driver Layout

The full-custom layout of the driver is focused on the techniques used to improve the driver bandwidth and mitigate the radiation effects on silicon devices. The layout of all MOSFETs has an interdigitated structure for matching purposes.

TABLE I
TID COMPENSATION SYSTEM SIZING

Device	Width [µm]	Length [nm]	Size
M1, M2	828	240	-
M3, M4, M5	1070	500	-
M6	105	500	-
M7	130	500	-
M8	413	500	-
M9	46	500	-
R	-	-	10 kΩ
C	-	-	240 fF

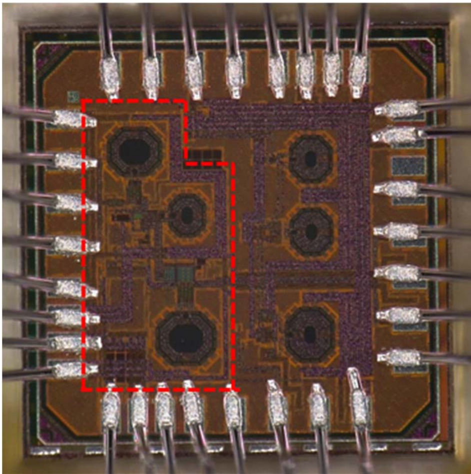

Fig. 9. Photo of the 1×1 mm^2 chip in 65 nm technology with the integrated driver enclosed by the red path.

They are designed with particular attention to the electromigration problem due to the high currents chosen for the generation of the wide output voltage. Therefore, the last metals of the stack are used everywhere is possible for their higher tolerated current density. To improve the draining of the radiation-induced parasitic charge, all the free layout space is filled with a grid of substrate contacts to reduce the resistive path toward the ground potential. The whole driver layout has an area of about 0.15 mm^2 which is predominantly occupied by the three differential inductors, as shown in the red circled area of Fig. 9. A redesign of the inductors with a more compact shape could be helpful in reducing the overall area.

VI. Driver Measurements

The experimental characterization of the driver is performed by wire bonding the chip directly to a testing printed circuit board (PCB) to avoid the spurious effects that a package may introduce. A four-layer board has been designed on a Rogers™ 4003C substrate and is depicted in Fig. 10. It is equipped with commercial off-the-shelf (COTS) components dedicated to the generation of supply voltages and bias currents. To verify the radiation hardness of the driver, the whole carrier board needs to be exposed to X-rays, hence a safe margin between COTS components and X-ray source prevents them to be damaged during measurements under irradiation. The board layout indeed includes a 2 cm distance keep-out distance between the chip under test and the COTS devices.

A. Electrical Measurements

The electrical measurements are performed by exciting the device under test (DUT) with a 2^{32}-1 combinations-long pseudo random binary sequence (PRBS-31) generated by a Kintex Ultrascale FPGA and using a 23 GHz 100 GS/s Tektronix oscilloscope to acquire the output signals. The oscilloscope disturbs the signal measurement by introducing a 50 Ω loading impedance shunt to ground. This could change the driver operation since it has not been designed for that load configuration. In addition, also the testing board traces can inevitably affect the quality of signal integrity. Therefore, some simulations have been performed to understand the effects of the testing board and the 50 Ω loading on the driver performances. They highlight a variation in 3 dB bandwidth variation of nearly 1.7% and an almost halved amplitude. Therefore, a factor of 2 should be considered to get the real signal amplitude, while speed performances could be taken without further adjustments. The frequency-domain characterization has been performed by feeding the driver with the PRBS-31 signals at different bit rates. This procedure, contrary to the use of a vector network analyzer (VNA), allows us to also take nonlinear circuit behaviors into account. Indeed, the VNA only excites the DUT with pure tones at different frequencies, thus providing only a linear approximation of the driver bandwidth. Fig. 11 shows the eye diagram amplitude of the driver output signals for different bit rate values, from 1.25 Gb/s to 12 Gb/s. The low-frequency amplitude is around 1.1 V, which should be doubled to get the actual swing provided to a single arm of a lumped MZM, i.e., a not terminated device.

Considering the 3 dB bandwidth, the driver appears to be operable with a bit rate up to 10 Gb/s. The 10 Gb/s measured eye diagram of the driver output signals is reported in Fig. 12. It has an amplitude of about 0.9 V which is within the 3 dB bandwidth and would correspond to a 1.8 V per arm with an MZM load.

B. Electro-Optical Measurements

An electro-optical characterization has been performed to verify the proposed driver's capability to control a p-n junction-based SiPh MZM.

As described in Section III-A together with the modelling assumptions, the photonic integrated circuit (PIC) hosting the MZM and the electronic chip including the driver under test have been assembled on the same PCB. The electrical connections have been made with 40 μm-diameter aluminum wedge-wedge bonding. The driver's differential input and output ports have been respectively bonded to the PCB and the PIC with wire lengths on the order of 1 mm. A detail of the described assembly is shown in Fig. 13.

Supply and control voltages for the driver are generated on a custom-made programmable board, while the input electrical bit stream is produced with an Anritsu MP1763C pulse pattern

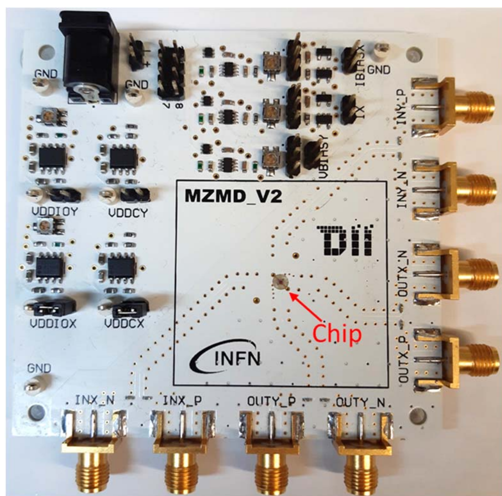

Fig. 10. Photo of the testing board with the chip directly bonded on it.

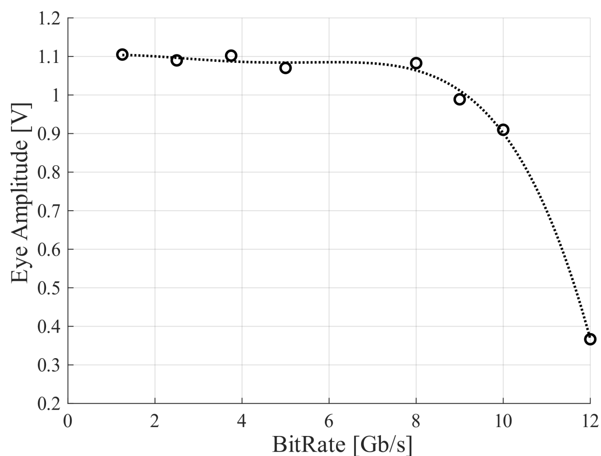

Fig. 11. Eye amplitude of the driver output signals as a function of bit rate.

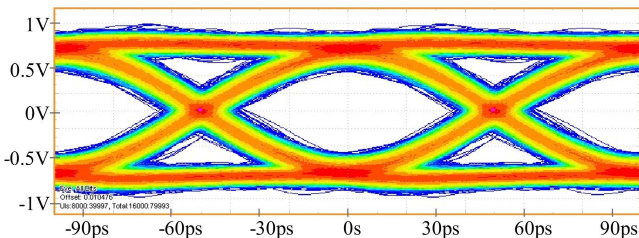

Fig. 12. Eye diagram of the driver output signals at 10 Gb/s.

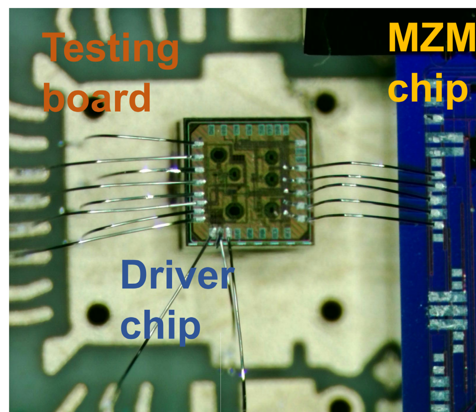

Fig. 13. Image of the driver chip connected with the testing board and SiPh chip hosting the MZM through aluminum bonding wires.

generator (PPG) following a PRBS-31 sequence. This signal is conveyed to the driver's input port passing through sub-miniature version K (SMK) cables, 2.92-mm connectors, and on-board microstrip transmission lines.

Concerning the optical setup, a tunable laser source (TLS) working in the C band has been used to provide optical power to the MZM. The operating wavelength has been fixed to 1548 nm in order to drive the MZM in quadrature, i.e., the working point which gives the maximum ER on the received waveform. Since optical input/output coupling is realized with grating couplers (GCs), a polarization controller (PC) was placed in the optical chain before the PIC. GCs are typically sensitive to a single polarization direction, hence an external alignment allows us to maximise the light intensity injected into the PIC. Although nominal optical insertion losses (IL) for the GCs used in this work are rated around 3-4 dB at each fiber-GC interface, these devices are strongly sensitive to their relative position to the pigtailed fibers. A non-optimal placement of the fiber array on the PIC can indeed dramatically affect the overall insertion loss to access the photonic devices under test [46]. In our measurement setup, we ended up with an IL of nearly 40 dB while accessing the MZM on the PIC, while expecting a maximum of 14 dB, considering optimal fiber-GC positionings together with ILs due to the MZM itself and on-chip routing. We attributed the excess loss to a mechanical misalignment between the fiber array and the GCs happened during the shipment of the testing boards.

To counteract this unexpectedly large IL and demonstrate the driver's ability to drive the on-chip MZM, two erbium-doped fiber amplifiers (EDFAs) have been inserted in the setup. Optical amplification has been split in two parts to avoid injecting too high optical power levels in the silicon waveguides, preventing the onset of optical nonlinear effects. The optical noise introduced by EDFAs was partially filtered by placing a tunable band-pass filter (TBPF) downstream the last optical amplifier. In this way, the out-of-band amplified spontaneous emission (ASE) was greatly reduced and, in turn, also the ASE-ASE beat noise in the output waveform. Nevertheless, the optical signal-to-noise ratio (OSNR) has been measured to be greater than 27 dB, ensuring that any eventual noise contribution to the received waveform could be attributed to the electronic side. The measurement setup is completed by a variable optical attenuator (VOA), followed by a 15 GHz-bandwidth photo-receiver module (HP11982a) which includes both photodetector (PD) and trans-impedance amplifier (TIA).

The electrical signal converted by the optical receiver is then fed to either a 20 GHz-bandwidth oscilloscope (Agilent DCA 86100C) or an Anritsu MP1764C error detector (ED). An overall scheme of the experimental setup is depicted in Fig. 14. Electro-optical bit error rate (BER) characterization has been

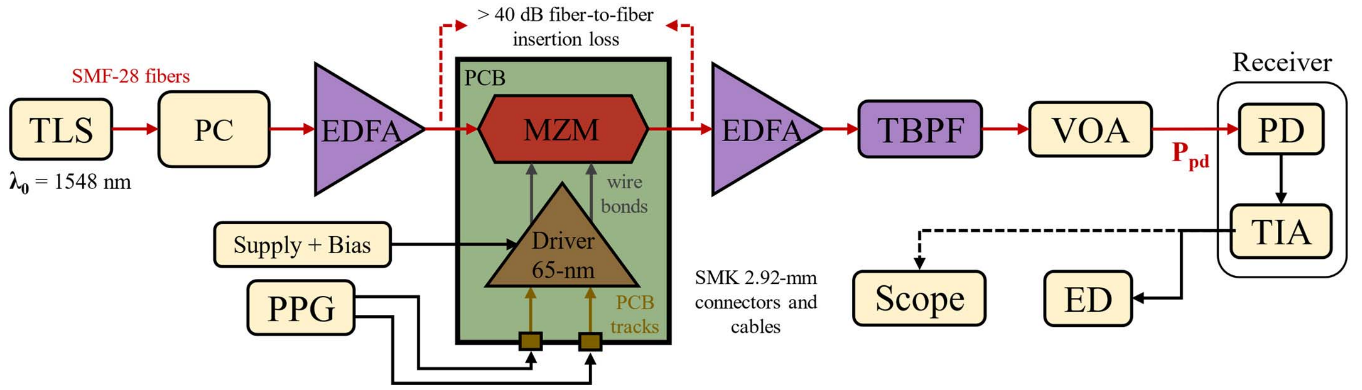

Fig. 14. Schematic of the electro-optical measurement system. Legend: TLS (tunable laser source), PC (polarization controller), EDFA (erbium-doped fiber amplifier), VOA (variable optical attenuator), TBPF (tunable band-pass filter), PD and TIA (photodetector and trans-impedance amplifier, HP 11982A), PPG (pulse pattern generator, Anritsu MP1763C), ED (error detector, Anritsu MP1764C), Scope (Agilent Infinium DCA 86100C).

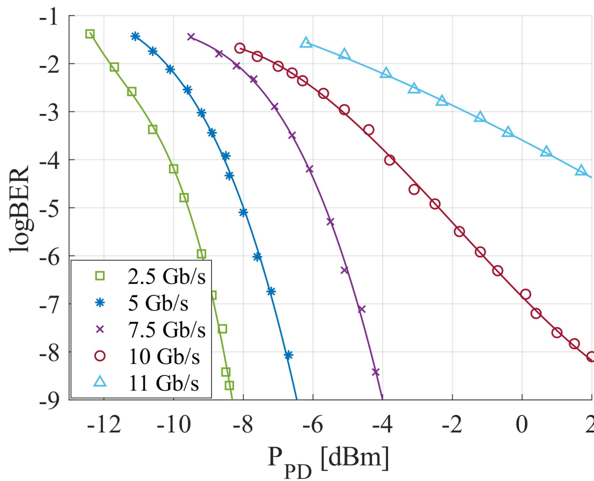

Fig. 15. Electro-optical BER results as a function of the photo-receiver input power and data rates.

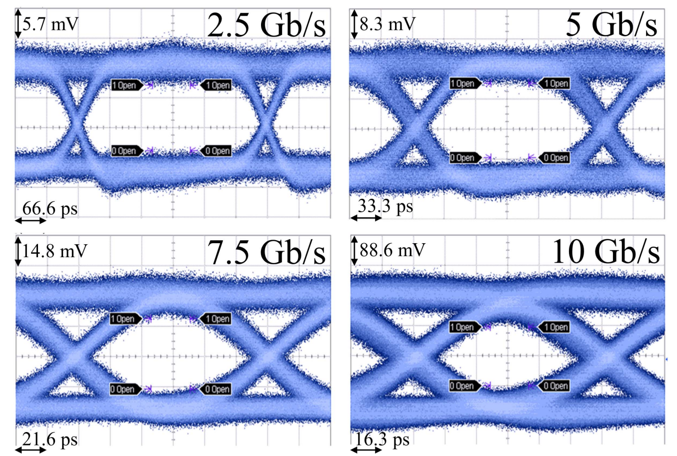

Fig. 16. Eye diagrams measured on the electro-optical setup. The photodetector output signals at different bit-rates are collected by the oscilloscope.

performed as a function of both bit-rate and optical power at the receiver (i.e., P_{pd} in Fig. 14) to verify the quality of the data transmission. Setting the bit rate on the PPG, the optical intensity level on the receiver is varied acting on the VOA and the BER level is taken from the ED. The results of these measurements are shown in Fig. 15. They confirm the driver's operability till 10 Gb/s when loaded with an MZM. Although the BER trace for 10 Gb/s shows a reduced slope compared to the curves at slower data rates, no apparent sign of BER floor is visible. The BER $1{\cdot}10^{-9}$ condition was not explicitly achieved for that trace because of the safety input optical power levels of the used photo-receiver (max. 1.76 dBm). Eye diagrams captured after the receiver's TIA are reported in the same BER condition (i.e., $8.1{\cdot}10^{-9}$) for different bit rates in Fig. 16. As expected from the BER characterization, they show that an increment in the eye height, which is proportional to the photo-receiver input power, is required to achieve the same BER for higher data rates. This is due to slight modifications in the shape of the eye diagrams while the bandwidth limit of the driver is approached. It is worth noting that the absolute values of the shown eye amplitudes depend on several setup-related factors, e.g., input optical power, optical losses and amplifications, photo-receiver gain, etc., and should not be considered as strictly relevant for the driver characterization.

C. Radiation Hardness Performances

The radiation hardness of the driver is evaluated by exposing the DUT to X-rays. The TID measurement is performed using the X-ray Seifert RP149 machine at the X-ray facility of CERN. The used dose rate is 8.2 Mrad/h, which is about 720 times higher than the mean dose rate forecasted for HL-LHC. Since the charge build-up in the oxide layers does not have time to recombine through annealing effects, the results of this stressing TID test are more conservative than the real case.

During irradiation, the driver is excited with 5 Gb/s PRBS-31 signal. This speed downgrading, compared to the results presented in Section III-A, was due to the implemented measurement setup. The usage of 3 meters-long cables indeed limited the maximum achievable bit rate. These long interconnections were required to access the DUT inside the irradiation chamber, while keeping data and power generators and measurements instruments safely outside.

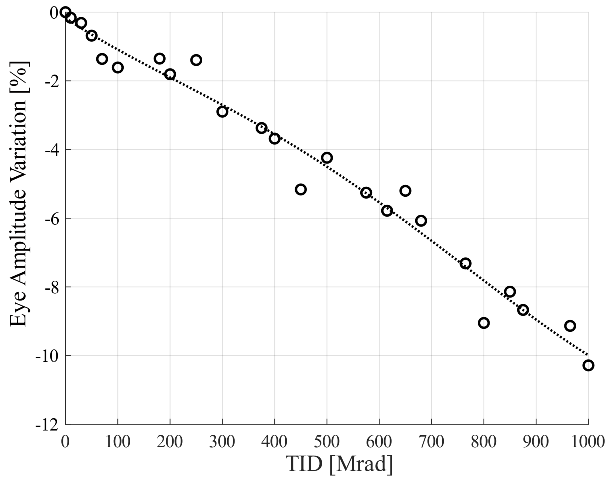

Fig. 17. Eye amplitude variation as a function of the TID.

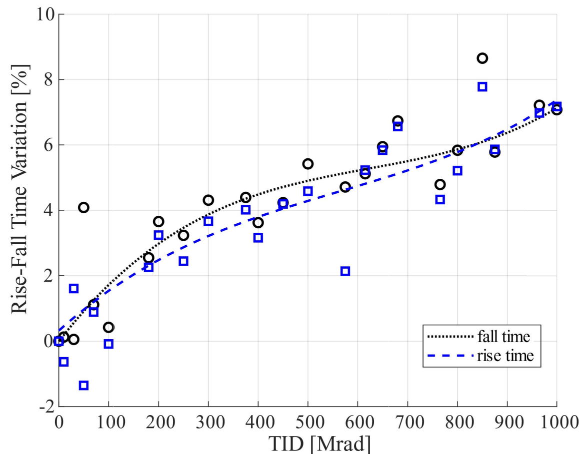

Fig. 18. Variation of the rise time and fall time of the output signals as a function of the dose.

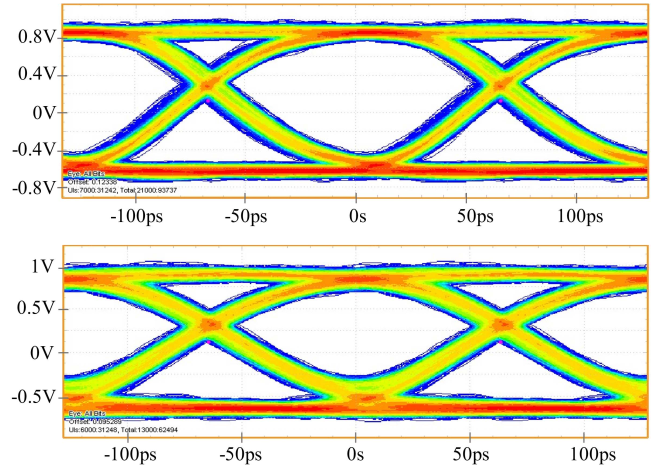

Fig. 19. Eye-diagram of the driver output signals at 7.8 Gb/s in pre-irradiated (top) and 1 Grad TID (bottom) measurements.

In Fig. 17 the variation of the eye amplitude as a function of TID is shown from 0 to 1 Grad. The eye amplitude decreases with the cumulated dose increment for the reduction of the MOSFETs performances, as expected from Section II. Although high TID levels impose severe effects on silicon devices, the driver is still able to operate with an eye amplitude reduction of about 10% at 1 Grad(SiO_2), thus validating the effectiveness of the proposed implemented RHBD techniques. In [20], the presented drivers were produced in the same technology and adopted only device-level RHBD techniques ending up with eye amplitude reductions of 25-30% at 800 Mrad (SiO_2). This confirms the substantial contribution of the circuit-level RHBD techniques proposed in this paper.

Concerning the impact of high-level TID on the driver's frequency response, we propose to analyse the behaviour of the rise and fall times on the measured output signals.

The spectral power density of a generic random NRZ (Non-Return-to-Zero) signal, is made by nulls at multiple of the bit rate and a spectrum amplitude decrement of −20 dB/decade up to the knee frequency (f_{knee}) and greater beyond [47]. The f_{knee}, which is typically considered as the maximum significant frequency of the random signal, does not depend on the bit rate but only on the rise and fall times of the signal, as shown in the following eq. (7):

$$f_{knee} \approx \frac{1}{2 \cdot t_r} \tag{7}$$

where t_r is the rise time and it is considered equal to the fall time. The behaviour of the f_{knee}as a function of the TID can thus be extracted from that of the rise and fall times.

Fig. 18 displays the variation of the output signals' rise and fall times as a function of the TID levels. As can be observed, the rise and fall times increase with the TID, reaching an increment of about 7% when the driver is exposed to 1 Grad(SiO_2).

Considering eq. (7), this increment in the rise and fall times corresponds to a reduction in f_{knee} of about 6.54% at 1 Grad, confirming the operability of the driver up to this high dose level.

In addition, the total jitter measurements were performed showing an increment of only 1.7% when the driver is exposed to 1 Grad. Therefore, no significant degradation is expected on the eye diagram shape. Fig. 19 shows the comparison between the measured eye diagrams of the driver output signals when it works in typical conditions and after being exposed to 1 Grad. Both eye plots have been acquired with the same setup used for the irradiation measurement to be comparable. Unfortunately, as also stated above, the setup did not allow us to perform 10 Gb/s measurements hence eye diagrams at 7.8 Gb/s are reported in Fig. 19.

VII. Conclusion

We have presented the design and the experimental characterization of a driver for a SiPh MZM able to operate up to 10 Gb/s in radiation environments exposed to doses up to 1 Grad(SiO_2). Considering the heavy impact that TID has on the performance of silicon technologies, the driver was designed following device- and circuit-level RHBD techniques. Design methodologies such as the usage of long-channel transistors, the adoption of ELT devices, the

TABLE II
STATE-OF-THE-ART COMPARISON

	[10]	[9]	[20][a]	This work
Technology	130 nm	65 nm	65 nm	65 nm
Bit rate	10 Gb/s	10 Gb/s	5 Gb/s	10 Gb/s
Electrical output swing	0.4 V	15 mA	2.75 V 2.08 V	1.8 V
Targeted Device	VCSEL	VCSEL	MZM-RR	MZM
Optical AOP / OMA [b]	-	3.41 dBm / 0.96 mW	-0.7 dBm / 0.55 μW	2 dBm / 0.89 mW
Consumption Power	55 mW	94 mW	98.06 mW	114.8 mW
TID tolerant	100 Mrad	600 Mrad	800 Mrad	1 Grad

[a]Two drivers with different output voltage swings are reported, one for an MZM device and the other for a RR device.
[b]AOP (Average Optical Power), OMA (Optical Modulation Amplitude)

avoidance of p-MOSFETs and thick oxide devices have all been adopted for device-level TID compensation. In addition, some circuit-level strategies have been exploited to further increase radiation hardness. Differential self-bias cascode architecture and common-mode feedback compensation for TID-induced degradation have been developed and applied to the driver. To meet both radiation-resistance and speed specifications, several broad-banding circuital solutions have been implemented, e.g., inductive peaking, cross-coupled capacitances, and CML buffer chaining. Electrical characterization in typical conditions shows the possibility to achieve data rates up to 10 Gb/s with a measured eye diagram amplitude of 0.9 V (see Fig. 11). Considering the loading effect of the 50 Ω terminated oscilloscope an eye diagram amplitude of 1.8 V is expected on each MZM arm.

Electro-optical measurements performed connecting the proposed driver to an MZM through bonding wires indeed report the achievement of a 10 Gb/s data rate. Then, the driver's radiation hardness, tested exposing the device to X-rays, highlights an operative range up to 1 Grad(SiO_2) with an amplitude loss of only 10% in the output signal swing. Considering the collected results, an eye amplitude greater than 1.78 V is expected till 10 Gb/s and 1 Grad(SiO_2). This voltage swing is still suitable for driving an MZM and thus validates the electronic driver's feasibility for radiation-hard optical link applications.

Table II compares the driver proposed in this work with state-of-the-art drivers for electro-optical modulators able to operate in radiation-pervaded environments. The work in [10], implemented in 130 nm technology, presents a driver for VCSEL diodes up to 10 Gb/s data rate using programmable pre-emphasis circuits and T-coils inductors to compensate for ESD capacitance. However, it shows a TID radiation hardness level of about 100 Mrad, the lowest of the compared drivers. In [9], another VCSEL driver reaches a 10 Gb/s data rate removing the ESD protections and using a capacitive feed-forward. Its radiation hardness is about 600 Mrad, which is still not suitable for the innermost layers of the HL-LHC experiments, where the TID expected is 1 Grad.

Comparing the last two table columns is clearly observable the performance upgrade with respect to our previous work [20]. This work indeed outperforms the driver presented in [20] not only in terms of speed performances but also in terms of radiation hardness. All the implemented broad-banding and RHBD techniques are therefore validated to be effective for the design of radiation-hard optical drivers for HEP experiments and could be further investigated in future works to address even better performance levels.

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