Terahertz Detectors and Imaging Array with In-Pixel Low-Noise Amplification and Filtering in CMOS technologies

A PhD dissertation presented by

Muhammad Ali

To

Integrated Radiation and Image Sensors (IRIS)
Fondazione Bruno Kessler, Italy

&

Information and Communication Technology (ICT)
University of Trento, Italy

Submitted in partial fulfilment for the degree of

Doctor of Philosophy

PhD Supervisor: Matteo Perenzoni (Senior Researcher)
Fondazione Bruno Kessler, Italy

Commission Members:

Prof. Gianfranco Dalla Betta, Prof. Andrea Neviani, Prof. Alessandro Tredicucci

Trento, April 2017

Declaration

I, Muhammad Ali, hereby declare that I wrote this thesis independently as part of the Doctoral work performed at Fondazione Bruno Kessler and University of Trento, Italy. I have clearly mentioned the aid, support and data taken from any external source.

Muhammad Ali

Abstract

Terahertz gap corresponding to the frequency band of 0.3-3.0 THz is historically the last unexplored region of the electromagnetic spectrum left to be fully investigated. The major difficulty that has hampered the maturation of technologies operating in this region lies in the fact that much unlike its bordering millimeter and infrared regions, generation and detection of THz radiation is not trivial. Yet, such is the intriguing nature and properties of the terahertz radiations that the interest in this region has not faded. Infact, potential applications of THz based systems have emerged in various fields including biomedical imaging, safety and security, quality control and communication.

Over the past decade, a lot of research work has been published with an aim to bridge this *gap* by both electronics and photonics based systems. While these attempts have succeeded to a certain extent, the available solutions either lack in terms of performance or are mostly bulky and difficult to integrate for portable and commercial purpose.

This PhD dissertation focuses on the design and investigation of direct terahertz detectors which could be operated at room temperature and fabricated in standard silicon technologies, thereby making use of several advantages like high level of integration, low cost and small device size that these technologies have to offer. In particular, the emphasis is on developing and characterizing terahertz systems for imaging application by using field effect transistor devices as detectors. This objective is pursued in three parts.

The first part (chapter 3) of the dissertation deals with the measurement and characterization challenges of terahertz systems. Unlike guided mode solutions, measurements of terahertz detectors and their systems require free space which presents several challenges due to atmospheric attenuation, spurious reflections and diffractions, beam shaping, and so on. Moreover, background noise is also significant considering that the detected signal is typically in the order of a few microvolts. In this regard, an overview of the most common techniques is given and a measurement methodology involving the use of a reference pyroelectric detector to measure the impinging input power and techniques for the evaluation of the detector under-test effective area is presented.

The second part (chapter 4) is related to the investigation of variants of antenna-coupled field effect transistor and schottky barrier diode in standard 180 nm CMOS process as examples of direct detectors. During laboratory characterization, detection of terahertz radiation from schottky diode could not be achieved due to matching issues. Moreover, optimization of schottky diode by modifying its standard cell proved to be challenging as compared to field effect transistor, which can be optimized easily to enhance performance parameters and was therefore finally chosen as the preferred choice.

The final part of the thesis (chapters 5 and 6) concerns with the implementation of analog readout interface to perform signal processing of detected terahertz signal. First, a single pixel consisting of on-chip antenna-coupled detector and a switched capacitor based filtering operation is designed and fabricated in 0.15µm process. The pixel is tested by performing both electrical and terahertz characterization, achieving high voltage responsivity value of 470 kV/W and a minimum NEP of 480 pW/sqrt (Hz). The interface architecture is highly repeatable and it can be used with any commercially terahertz source, even if its operation is limited by low modulation frequency. On the basis of the successful measurement results, an 8 x 6 terahertz array for real-time imaging application is fabricated in the same technology by modifying the interface architecture to make it power and area efficient.

Thesis: Objective and Contributions

The objective of this thesis is to investigate Silicon based direct THz detectors and systems for imaging applications implemented in standard CMOS technologies with a special emphasis on Field Effect Transistor (FET)-based detectors. This thesis involves design, fabrication and characterization of various chips and I had been involved in carrying out most of these tasks. A brief overview of the chapter contents is given below.

Chapter 1 Introduction

This chapter presents an overview of the state-of-the-art THz devices, sources and detectors with an emphasis on their utilization in various applications. The merits and demerits of these devices are discussed and summarized in tabular forms along with their most important performance parameters. THz region is explained with reference to the electromagnetic spectrum: its fascinating properties and the potential applications of THz based systems is outlined.

Chapter 2 Theory of CMOS based FET THz detection

The advantages of fabricating THz detectors in standard CMOS technologies are presented here. The chapter then discusses the underlying theory of the plasma waves generation in the FET channel in the historical context. Moreover, the quasi static and Non-Quasi static modeling shows the rectification of the incoming THz signal of the FET channel.

Chapter 3 Measurement techniques for direct THz detectors

This part deals with the investigation of various laboratory techniques for the real-time measurement and characterization of direct THz detectors. In particular, accurate measurements regarding the impinging input power received by the detector and its effective area illuminated by THz radiation are important as they directly affect the performance parameters. An overview of existing methods and their limitations are discussed. Moreover, a methodology involving the use of a reference pyroelectric detector to accurately measure the input power is presented. This methodology is validated on a test structure consisting of an on-chip antenna and a FET based direct THz detector implemented in a standard 0.18µm technology.

Chapter 4 Simulation and Optimization of FET THz detectors

In this chapter the performance parameters of direct THz detector are defined. The results from SPICE simulation of FET detector are compared with the theoretical/mathematical modeling describing the performance parameters. Moreover several variants of the FET detector, based on the difference in configuration and device parameters are characterized using the test methodology of Chapter 3.

Chapter 5 Single-pixel design and readout interface for FET THz detector

This chapter discusses the theoretical details and simulations of the Switched Capacitor readout interface to process the detected signal of the FET THz detector are presented. The focus has been to design a low noise, robust and repeatable interface that could achieve high voltage responsivity and preserve the detector NEP. The electrical and THz characterization results are presented, confirming the functionality of pixel.

Chapter 6 Terahertz imaging array

The chapter presents an improved readout interface architecture for a FET detector, which is different from the one presented in Chapter 5. The main objective of designing a new architecture is to reduce power consumption and pixel area as compared to the previous pixel. Based on this interface, an 8 x 6 THz imaging array has been fabricated. The theoretical design details, simulations and characterization results are presented in this chapter.

Chapter 7 Thesis conclusion and Future prospects

List of Publications

Journal Article(s)

- **M. Ali**, M. Perenzoni and D. Stoppa, "A Methodology to Measure Input Power and Effective Area for Characterization of Direct THz Detectors," in *IEEE Transactions on Instrumentation and Measurement*, vol. 65, no. 5, pp. 1225-1231, May 2016.

Conference Publications

- M. Zanoli, **M. Ali** and M. Perenzoni, "A 8-6 pixel THz Focal Plane Array with Per-Pixel High-Gain Readout Channel in 150 nm CMOS Technology," *42nd International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz), 2017* (submitted).
- **M. Ali**, M. Perenzoni and D. Stoppa, "A high-gain, low-noise switched capacitor readout for FET-based THz detectors," *42nd European Solid-State Circuits Conference*, Lausanne, Switzerland, 2016, pp. 401-404.
- **M. Ali**, M. Perenzoni and D. Stoppa, "A measurement setup for THz detectors characterization validated on FET-based CMOS test structures," *IEEE International Instrumentation and Measurement Technology Conference (I2MTC) Proceedings*, Pisa, 2015, pp. 320-324.
- **M. Ali** and M. Perenzoni, "Comparison of gate driven and source driven FET structures as THz detectors," *Proc. SPIE*, vol. 9141, pp. 914106-1–914106-9, May 2014.

Keywords

CMOS, Terahertz, imaging, Field Effect Transistors, modulation, direct detectors, Noise Equivalent Power (NEP), voltage and current Responsivity (R), readout interface, Switched Capacitor (SC) filters, antenna gain, directivity, polarization, thermal noise, flicker noise, chopper stabilized circuit, gm/id design, deice optimization, real time imaging , focal plane array, correlated multiple sampling, non-linear device, solid state, antenna-coupled

Acknowledgements

I would like to express my gratitude to my advisor Mr. Matteo Perenzoni and group head Dr. David Stoppa for providing me an opportunity to work on this dissertation in Integrated Radiation and Image Sensor (IRIS) group, Fondazione Bruno Kessler (FBK) Italy. I am indebted to Matteo's valuable guidance throughout this work and the efforts he had put in to review this thesis. I would also like to thank other members of IRIS including Dr. Leonardo Gasparini, Nicola Massari and Massimo Gottardi, as well as Dr. Lucio Pancheri of the University of Trento. My special appreciation goes to Daniele Perenzoni and Daniele Rucatti for helping me out in various laboratory and chip measurement activities and for useful technical discussion.

I would like to thank current and former PhD students I had the pleasure of working with, including Olufemi Olumodeji, Hesong Xu, Leo Huf Campos Braga and Moustafa Khatib. My special appreciation goes to Suzana Domingues for regularly helping me out and our several useful discussions regarding technical contents of the topic. I would also like to thank Marco Zanoli for carrying out measurements of 3rd chip.

My friends in Trento proved a great source of fun and happiness which made my stay in Italy very memorable. I would like to thank Usman Raza for our long chats and for the help he provided me on various matters in the initial stages of my PhD. Maqsood Ahmed, Musawar Saeed, and Atta *Bhai:* you guys had been wonderful in arranging parties in San Bartolomeo.

My dearest friend Usman Hafeez Sandhu: I know I have found a gem of a person in you. I would like to thank you and your family for hosting countless dinners and for making us laugh with your light banter.

I extend my gratitude to Mr. Harald Neubauer for giving me an opportunity to work in the Fraunhofer Institute of Integrated Circuits (IIS), Germany after I finished the technical work at FBK. My appreciation also goes to other colleagues including Dr. Stephan Junger and Thomas Schweiger. In particular I would like to thank Dr. Matthias Oberst for his patience and guidance regarding my work in IIS.

I would like to thank my wife *Ameera* for standing by my side through every thick and thin and for helping me out to get through difficult times. It was her love, insistence and motivation that kept me going even in those moments when a part of me thought of giving up. Our bond strengthened during this time and also with the arrival of our son *Azlaan* who filled our lives with joy and happiness.

And finally above all, I owe my every success and specially this one to my mother for all the sacrifices she had made in her life just so I could have my dreams fulfilled. I thank you for filling me with determination, passion and hunger to achieve my goals and for believing in me. I know how much this means to you.

To my family

List of Symbols, Abbreviations and Glossary

EM	Electromagnetic
IR	Infrared
THz	Terahertz
Si	Silicon
eV	Electron volt
K	Kelvin
W	Watt
SOA	State of the Art
FEL	Free Electron Laser
CMOS	Complementary Metal Oxide Semiconductor
QCL	Quantum Cascade Laser
IF	Intermediate Frequency
LO	Local Oscillator
PA	Power Amplifier
QS	Quasi Static
NQS	Non Quasi Static
KCL	Kirchhoff Current Law
PDE	Partial Differential Equation
KVL	Kirchhoff Voltage Law
GD	Gate Driven
SD	Source Driven
DR	Dynamic Range
MDS	Minimum Detectable Signal
NEP	Noise Equivalent Power
VCVS	Voltage Controlled Voltage Source

MMIC	Monolithic Microwave Integrated Circuits
OPAMP	Operational Amplifier
S&H	Sample and Hold
FOM	Figure of Merit
GBW	Gain Bandwidth
BW	Bandwidth
AM	Amplitude Modulation
D	Directivity
FPA	Focal Plane Array
DUT	Device under Test
BN	Background Noise
UCA	User Controlled Attenuation
ADC	Analog to Digital Converter
SC	Switched Capacitor
FET	Field Effect Transistor
SBD	Schottky Barrier Diode
SNR	Signal-to-Noise Ratio
HPF	High Pass Filter
BPF	Band Pass Filter
LPF	Low Pass Filter
QF	Quality Factor
CT	Continuous Time
DT	Discrete Time
STF	Signal Transfer Function
NTF	Noise Transfer Function
PSD	Power Spectral Density
OTA	Operational Transconductance Amplifier

CMFB	Common Mode Feedback
CM	Common Mode
PAC	Periodic AC analysis
CW	Continuous Wave
GND	Ground
CMS	Correlated Multiple Sampling
FD	Fully Differential
MC	Monte Carlo
FF	Flip Flop
SR	Shift Register
MUX	Multiplexer
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MIM	Metal Insulator Metal
RMS	Root Mean Square
AC	Alternating current
DC	Direct current
FoM	Figure of Merits
JSSC	Journal of Solid-State Circuits
ISSCC	International Solid State Circuits Conference
IEEE	Institute of Electrical and Electronics Engineers
MOS	Metal Oxide Semiconductor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
SPCIE	Simulation Program with Integrated Circuit Emphasis
MC	Monte Carlo
BSIM	Berkeley Short-channel IGFET Mode
G	Closed loop gain

V_{IN}	Input Voltage
A	Amplitude
g_m	Small signal transconductance
g_{DS}	Drain to source conductance
r_{DS}	Drain to source resistance
k	Boltzmann constant
T	Temperature
K	Kelvin
C	Capacitance
I	Current
V	Voltage
V_{REF}	Reference Voltage
V_{OUT}	Output Voltage
ω_0	Angular frequency
f_{CENTER}	Center frequency
S_{TH} (f)	Thermal noise spectral density
1/f	Flicker noise
V_{OV}	Overdrive voltage
V_N^2	Voltage noise power
T_S	Sampling period
η	Substrate factor
λ	Wavelength
Q	Quality Factor
A_0	DC open loop gain
f_{In}	Input frequency
f_{clk}	clock frequency
MATLAB	Matrix Laboratory

Table of Contents

List of Figures

List of Tables

CHAPTER 1: INTRODUCTION

1.1 ELECTROMAGNETIC SPECTRUM

THz attracted vast scientific research and experimental interests primarily due to its nature of behavior that, at times, is at odds with the rest of the electromagnetic spectrum. Figure 1-1 shows the Electromagnetic (EM) Spectrum on the frequency and wavelength axes depicting the frequency range of different regions. The Terahertz range (THz) correspond to the waves oscillating at the rate of 10^{12} oscillations or periods per second and it lies between the millimeter-wave and far-infrared (IR) regions on its lower and upper end of the spectrum, respectively. The boundaries of this region are generally defined between 300 GHz (1000µm) to 10 THz (30 µm) [1] [2]. Thanks to its several intrinsic behavioral properties, the THz region had specially been of keen interest to the physicists and scientists for long time dating as far back as the early 19th century.

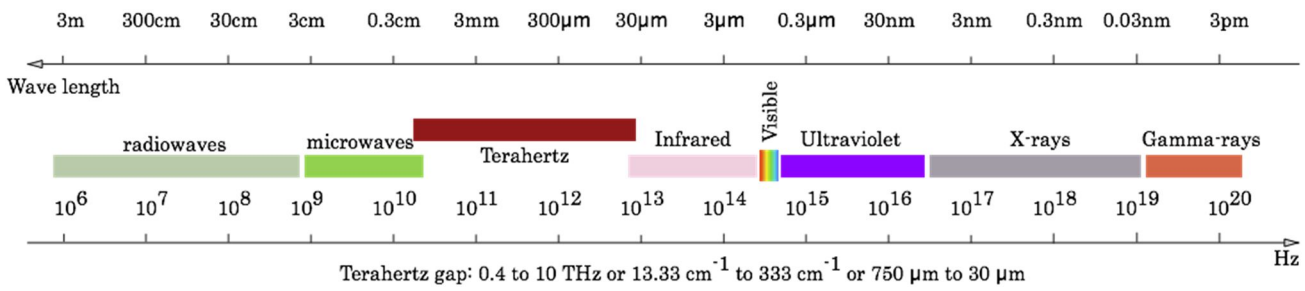

Figure 1-1: Electromagnetic Spectrum [3]

From historical perspective, the realization of the THz systems and their prototypes has proven to be quite difficult. Indeed, in and below its neighboring millimeter-wave region, many electronic and RF systems for signal generation, detection, and amplification are reported. Thanks to the scalability and low cost of these technologies, these systems make up the very basis of many commercial applications for large scale manufacturing, especially in communication systems. On the other hand, well-known optical techniques are employed to cover the far-IR region. However, unlike these two, the THz region had been marked with the lack of

solid-state devices that could be used for efficient signal generation and THz detection at room temperature, and hence the name 'THz gap' was originated. Despite of this difficulty, there has been an interest to explore and bridge this gap, mainly because of many peculiar properties which are explained in details in the following paragraphs [4] [5].

1.2 PROPERTIES OF THZ RADIATION

1.2.1 Low Photon Energy

THz waves carry very low photon energy. At 1 THz, the energy carried by the photons is only 4 milli-electron volt (meV): this level is extremely low, for example compared to the X-rays that carry up to several keV of energy. Such low levels of energy cannot cause ionization which makes the use of THz technology harmless to human body tissues. However, low energy levels also make it very difficult to detect THz radiation.

1.2.2 High Penetration

THz radiation can penetrate through many non-metallic and nonpolar materials including plastic, clothing and wood but they are reflected back from the metals. This property enables THz systems to see through packaging to find out hidden and concealed object [6]. Many materials, such as explosives, dangerous chemical substances and biological agents have characteristics THz spectra which can be used to detect the fingerprint, thus allowing the detection of these substances.

1.2.3 Atmospheric behavior

THz radiations have high water absorption coefficient and they are scattered from water molecules which means that they can be severely attenuated while propagating through the atmosphere [7].

Figure 1-2 shows the behavior of the THz radiations on their interaction with water molecules which shows that the attenuation is dependent on the concentration of water vapors and the THz region (especially from 1 - 10 THz) suffers from the highest atmospheric attenuation. It is also worth noticing that attenuation is dependent on water vapors and the effects of fog and rain cannot be easily

distinguished. Indeed, atmospheric attenuation effects both passive and active imaging applications with the possible reduction in the SNR value in the sensor image.

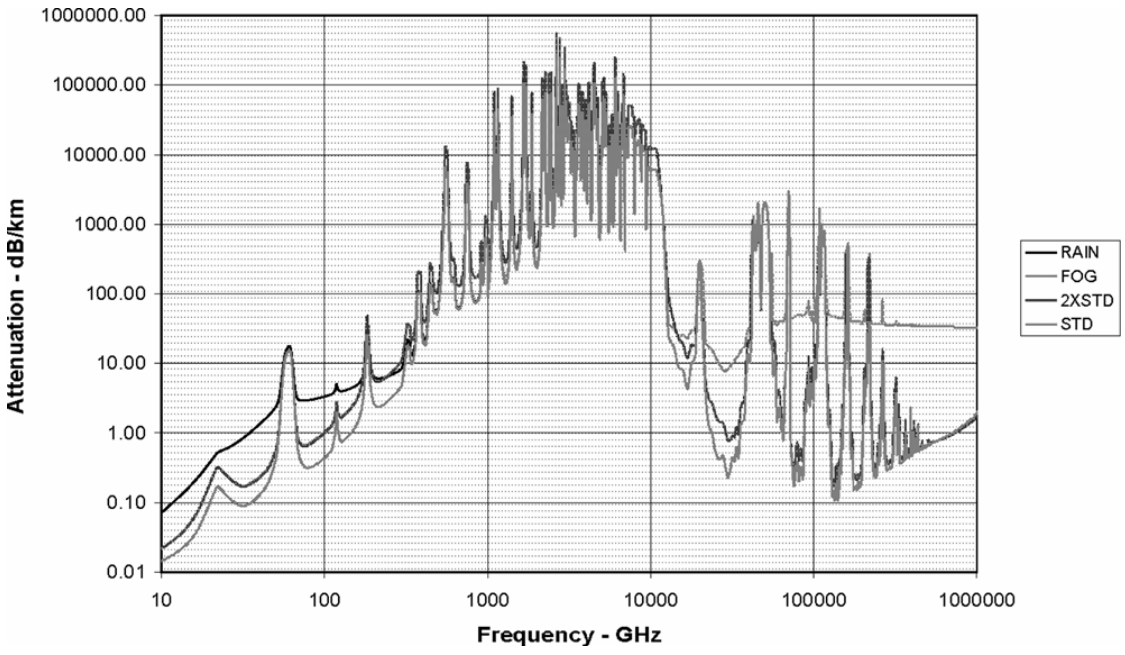

Figure 1-2: Graph showing the atmospheric attenuation as a function of frequency at sea level [7]

1.3 THz APPLICATIONS

1.3.1 Imaging

Low photon energy and ability to penetrate specific materials make the THz region useful for imaging applications, especially in the defense and security fields [8] [9]. THz imaging systems can be employed as body scanners at airports, sensitive installations and important buildings [10] [11], making them a complementary solution in addition to X-ray screening and other types of metal detectors. However, low photon energy also reduces the quantum efficiency of the THz detectors which makes it very challenging to design suitable readout architectures for imaging systems [12].

Medical and biomedical imaging is another field that can be potentially benefitted from THz imaging systems. Again, thanks to their low energy and high spectral resolution, THz radiation is safe to use for human body tissues but the water contents in these tissues hamper imaging. THz radiations can also be employed to analyze and reveal various chemical and biological phenomena [13]. For example, due to the large absorption coefficient of water, measurement of water contents in a plant is one potential application. Another application involves analyzing various kinds of cancers, including liver and breast cancer cells [14].

1.3.2 Quality control and non-destructive testing

Every material is made up of atoms and molecules that are combined together by chemical bonding. These bonds can vibrate at their characteristics frequency when exposed to electromagnetic radiation of certain wavelength. Indeed, information about their properties and composition, as well as impurities of the substance can be determined. THz radiation can be used to carry out the non-destructive testing and quality control of the materials and objects, including the analysis of tablets and pharmaceutical products during production for quality control purposes [15] [16]. This offers a marked improvement and advantage as compared to the other techniques like X-rays scanning and traces detection. Another example of non-destructing testing includes detecting and preventing smuggling of objects and illicit drugs across borders and countries.

1.3.3 Spectroscopy

Spectroscopy is referred to as the interaction phenomenon between electromagnetic radiations and matter and it is used to carry out the measurement of intensity of radiation as function of wavelength. Examples of spectroscopic systems include (but are not limited to) near infrared, Raman, gamma and X-ray spectroscopy. In a spectroscopic system, it is possible to determine the electrical characteristics of the material by knowing the absorbance or reflectance of molecules of the detected signal [8] [14] [17]. The Time Domain Spectroscopy (TDS) works on the principle of coherent detection which determines the amplitude and phase of the received sample signal. The TDS is considered to be one of the most useful application fields of THz waves [18].

1.3.4 Communications

Wireless data rates have drastically increased over the last decade for information sharing purposes because of which there has been a high demand for much higher speed wireless communication systems. THz systems can provide an option for extremely high data rate transmission for both the wired and wireless transmission since in THz range, high communication rates can be achieved with modulation techniques [19] [20] [21] . This possibility of THz-based communication can also alleviate the problems regarding spectrum scarcity and data limitations pertaining to the current wireless standards. However as discussed earlier, due to very low power levels of the THz sources and high water and atmospheric absorption, THz radiation is severely attenuated which necessitates the requirement for directive systems. Moreover this also puts a limit regarding the distance as THz based communication can be used for only short range or line-of-sight communication since the limiting factors hamper their potential for long range communication.

1.3.5 Astronomy

One of the most fascinating applications of THz region is its usage to understand atmospheric composition, as well as the formation of planets and stars of the solar system [22] [4].The interstellar medium, which is considered to be the matter existing in space between stars and in galaxy consists of gases in various forms, dust particles and cosmic rays. It is an experimentally proven fact that 98% of the photons emitted by the Big Bang fall either in the infrared or THz band. The age of galaxies can therefore be estimated by determining the energy levels of these photons. Likewise, THz radiation can also be used to observe composition of the earth's outer hemisphere where atmospheric temperature generally varies between 10K up to several 100K temperature range as it helps in determining the behavior, pressure and concentration of the gases surrounding the earth atmosphere. These gases include nitrogen, oxygen, argon and carbon dioxide among others as well as the ozone layer that absorbs the harmful rays emitted by the sun. Observing ozone gas is also critical to monitor pollution and global warming [22].

1.4 THz Sources

In the THz gap, the difficulty for signal generation stems from the fact that solid-state electronic sources are limited by the maximum operating frequency of the device which is useful for RF and microwave regions but not for THz signal generation. Of late however, with the advancement in Si technology the device speed is pushing well into the lower end of THz region, making it possible to design low power sources [23] [24]. On the other hand, photon energy of many optical sources is very low at room temperature, rendering them ineligible to use in THz region. THz radiations can be generated using thermal, electronic and optical means [25]. In the next section, these sources are explained in more detail.

1.4.1 Thermal Sources

Any radiating object operating at a temperature above absolute zero produces THz radiation. An example is a blackbody radiator which is a thermal based THz source having broadband characteristics that can radiate waves up to Infrared region. However, the emission efficiency of a blackbody radiator is low and the radiated power is only in nanowatt range.

1.4.2 Electronic Sources

The electronic THz sources include:

1.4.2.1 Backward Wave Oscillator (BWO)

A BWO is a vacuum tube that is used to generate waves in the microwave up to the THz frequency range [26]. Its principle of operation is based on the interaction of an electron beam with a slow wave structure. The BWO produces high power THz radiation, typically of the order of a few watts (W). The main disadvantage of the BWO is that it requires a strong magnetic field to operate and it is also potentially fragile.

1.4.2.2 Gunn and IMPATT diodes

Gunn and IMPATT diodes are usually exploited in the microwave regime where they can be used as oscillators or amplifiers based on their negative conductance. They

are high power devices and have recently been implemented to produce THz waves at 0.7 THz signal frequency [27] [28]. However, their application in the THz frequencies is still in the preliminary stages of the research work and they are not used for commercial applications.

1.4.2.3 Free electron laser

Free Electron Laser (FEL) is a high output power source capable of producing THz radiation. The principle of operation of a FEL is based on the acceleration of the free electrons through vacuum to a relativistic speed, and then decelerating these high speed electrons by moving them through a magnetic structure where they lose energy which is ultimately converted into light [29]. A FEL can generate power from several hundred of Watts (W) to kilowatts (kW). One advantage of the FEL is that its frequency can be fine-tuned continuously within 0.1 THz to 10 THz. However, the disadvantages include high cost, large and complex systems due to which the FEL based sources are only limited to scientific research area.

1.4.2.4 Frequency Multipliers

Frequency multiplier is an example of Si based electronic source and it works on the principle of multiplication of the fundamental frequency to reach up to the THz frequency range. They make use of the Power Amplifier (PA) in the RF and microwave region, where enough transistor gain is available to provide the necessary RF power. The fundamental frequency is then passed through frequency doublers and triplers to reach the desired frequency [30] [24] . However, implementing the PA on-chip occupies area and consumes a lot of DC power. Despite of this, a lot of research activity in the recent past has focused on designing THz sources using frequency multipliers [31] [32].

1.4.2.5 Oscillators

Si based oscillators provides another option to implement electronic THz sources. As the maximum oscillation frequency is limited and defined by the technology, harmonic oscillators can be utilized to increase the fundamental frequency in order to generate the desired signal in the THz range. A few examples of these oscillators are given in [33] [23].

1.4.3 Optical Sources

Optical THz sources can be broadly divided into two categories:

- Continuous Wave (CW) sources
- Pulsed sources

The Quantum Cascade Lasers (QCL) and photomixers are good examples of CW THz sources, although they can also be used in pulsed-mode. These are described in detail in the following paragraphs.

1.4.3.1 Quantum Cascade Lasers

QCL is an optical source that is capable of generating milliwatt power at the THz frequencies. Its principle of operation is based on injecting electrons into a periodic structure of compound semiconductors [34] [35].The electrons undergo inter-sub band transitions in a cascade configuration, resulting in the emission of photons at the THz frequencies. QCL can be used in many applications and their frequency can be fine-tuned using different quantum well structures. Their biggest disadvantage is that they might require a cooling mechanism to maintain the cryogenic temperatures. However, as the operating frequency of the QCL decreases, the photon energy also decreases resulting in a decrease in the operating temperature.

1.4.3.2 Photomixers

A photo-mixing device or photo-conductive mixer is typically a metal-semiconductor junction which mixes two laser sources operating at different frequencies and produces an output as a result of the mixing multiplication process. This output can be fine-tuned within a large range by varying the frequency values of the laser sources and hence photomixers are tunable sources. The THz radiations produced on the basis of photo-mixing principle typically achieve only a few nanowatt (nW) of output power and are therefore useful for only those applications that require a small amount of power [36] [37].

Table 1-1 presents a summary of the characteristics of various THz sources.

Table 1-1: Characteristics of various THz sources

	FEL	QCL	GUNN oscillator	IMPATT oscillator	Frequency multiplier	Photomixer
Output power (W)	10-100	10^{-3}- 1	10^{-3}- 0.1	1	0.1	10^{-5}
Frequency range (THz)	0.1-10	1-5	0.03-0.3	0.03-0.3	0.1-2	0.1-1.6

1.5 THz DETECTORS

THz detectors can be broadly classified in two main types:

- Heterodyne (coherent) detectors
- Direct (Incoherent) detectors

1.5.1 Heterodyne (Coherent) Detectors

In heterodyne detectors, THz radiations are down converted to an intermediate frequency (IF) using a Local Oscillator (LO), thereby preserving the amplitude and phase of the incoming radiations [25] [38]. The primary advantage of this type of detection is that the IF signal falls in the much lower frequency range (1-50 GHz), appropriate to electronics response time and it is much easier to process this signal, for example, to increase the SNR using low noise amplifiers which are easily available. Heterodyne detectors show good performance in terms of their sensitivity and responsivity, which makes these devices useful for spectroscopy and high-resolution imaging [39]. However, the limiting factor to achieve the heterodyne sensor arrays in THz region for these applications is the low output power produced by the solid-state LOs. Indeed for an on-chip solution, their main drawback is the increased DC power consumption of the PA and large area. As a result, they are not usually employed in large arrays. However, there exist some small arrays that are combined with phase control to allow beam steering, which makes virtually large arrays possible.

1.5.2 Direct (Incoherent) Detectors

Direct THz detectors directly convert the impinging THz radiation into a baseband (DC) signal. Direct detectors are preferred for applications requiring moderate spectral resolution but demand high sensitivity. Just like THz emitters described above, their principle of operation is based on thermal, optical and electronic mechanisms. Some of these detectors are implemented in specialized technologies which are not compatible with the CMOS technology. Bolometers, microbolometers and golay cells are some of the examples of thermal direct THz detectors, while Field Effect Transistor (FET) and Schottky Barrier Diode (SBD) are the examples of electronic detectors. These are briefly explained below:

1.5.2.1 Bolometer

Bolometers are a kind of thermal detectors that rely on the temperature dependent resistor, whose resistance can be changed when exposed to electromagnetic radiations [40]. Figure 1-3 shows the schematic of the bolometer which typically consists of a silicon bridge and an absorber of thin semiconductor layer. It is vital to have a material with high **T**emperature **C**oefficient of **R**esistance (TCR) to detect signal changes due to the change of temperature. Their principle of operation is as follows: the incident radiation falls on the absorber surface which raises the temperature of the silicon bridge above the temperature of the thermal reservoir T_0. This temperature change alters the resistance of bolometer and the power of the incident radiation can be estimated by applying the voltage at the device terminals and measuring current passing through it or vice versa.

Bolometers exhibit high sensitivity over a wide frequency range but they require a sensitive electronic readout circuitry to process the output quantity [41].

1.5.2.2 Golay Cell

A Golay cell is an opto-acoustic device that is used for the detection of infrared and THz radiations. It consists of a gas chamber, a flexible membrane and a window to receive the incident THz radiations as show in the schematic of Figure 1-4 .

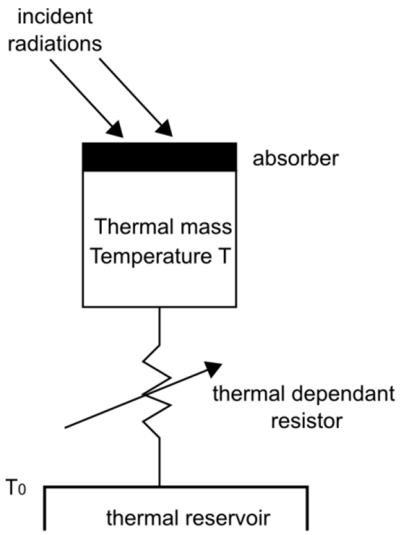

Figure 1-3: Schematic showing the operation of bolometer

The principle of operation is as follows: the incident THz radiation passes through window and absorbed by the metallic film (absorber) which heats up gas inside the chamber. As a result of this temperature increase, the gas expands, causing distortion of the membrane [42]. This distortion is a measure of the incident energy absorbed by the gas and it can be sensed by combination of an LED, a photodiode and an optical lens as the deflected light from the membrane represents the intensity of the incident radiations.

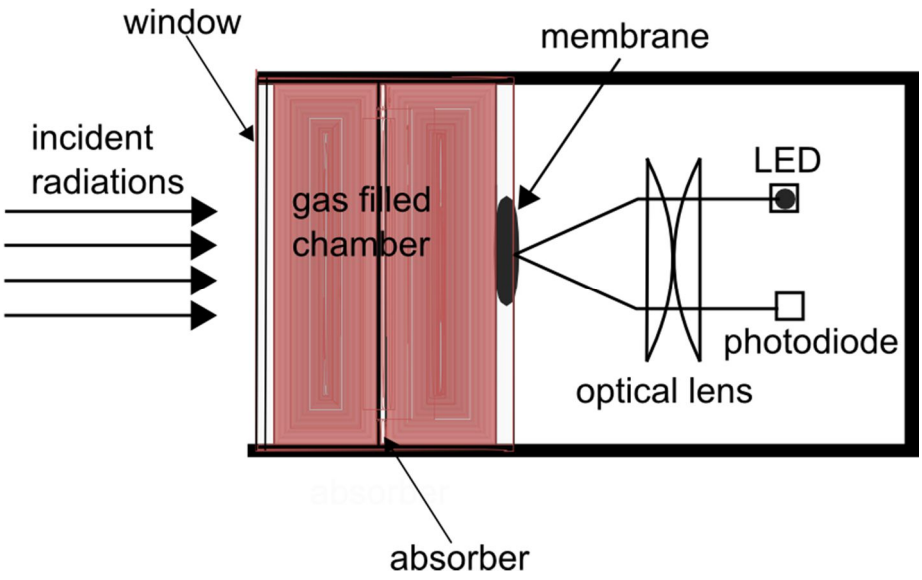

Figure 1-4: Schematic showing the operation of golay cell

Golay cells are sensitive devices with a very large spectral response over a wide range of frequencies, typically ranging from 0.1 THz to 30 THz.

1.5.2.3 Pyroelectric detector

A pyroelectric detector is a type of thermal detector that works on the basis of thermal pyro-electric effect [43]. It uses a thin pyroelectric film in the form of a capacitor, which is sensitive to THz radiation at room temperatures. When the incident radiation falls on the pyroelectric film, the temperature increases inducing a polarization change that eventually changes the capacitance value. The incident power of the THz radiation can be determined by biasing the detector at a fixed bias voltage and measuring the charging or discharging of the current due to the change of the capacitance.

Just like the golay cells, pyroelectric detector exhibits a broad spectral response, exhibiting high value of voltage responsivity in the THz region while operating at room temperature [44]. However, the incident THz radiation must be modulated either electronically or mechanically for the proper functioning of the pyroelectric detector.

1.5.2.4 Field Effect Transistor

FET is an example of solid-state electronic/plasmonic detector that can be easily fabricated in the sub-nanometer CMOS technologies [45]. From an electronic viewpoint, THz detection in the FET takes place on the basis of resistive self-mixing. However, the actual underlying principle of the FET as a THz detector is more physical in nature and dates back to early 90's when Dyakonov and Shur proposed the concept of plasma waves inside the FET channel which generates a DC output signal [46].

1.5.2.5 Schottky Barrier Diode

Schottky Barrier Diode (SBD) has traditionally been used in RF and high frequency circuits as frequency mixers [43]. Recently they were employed on-chip to work in THz imaging arrays. Their highly non-linear exponential (I-V) relationship down converts the incident THz radiations into DC signal and thus the SBD falls in the category of direct THz detectors. Figure 1-5 shows the symbol of the SBD alongside

its small signal model. If R_S is the series resistance of the diode while R_J and C_J represent the junction resistance and capacitance, respectively then the voltage responsivity of the SBD is:

$$R_V = \frac{V_D}{P_{IN}} = \frac{1}{2I_S . e^{\frac{qV_D}{nk_BT}}} = \frac{1}{2(I_S + I_D)} \quad (1\text{-}1)$$

SBD is able to achieve very high voltage responsivity, of the order of a few hundred [V/W]. However at low bias voltages, the junction resistance is very high and perfect matching network is required for efficient power transmission [48,49].

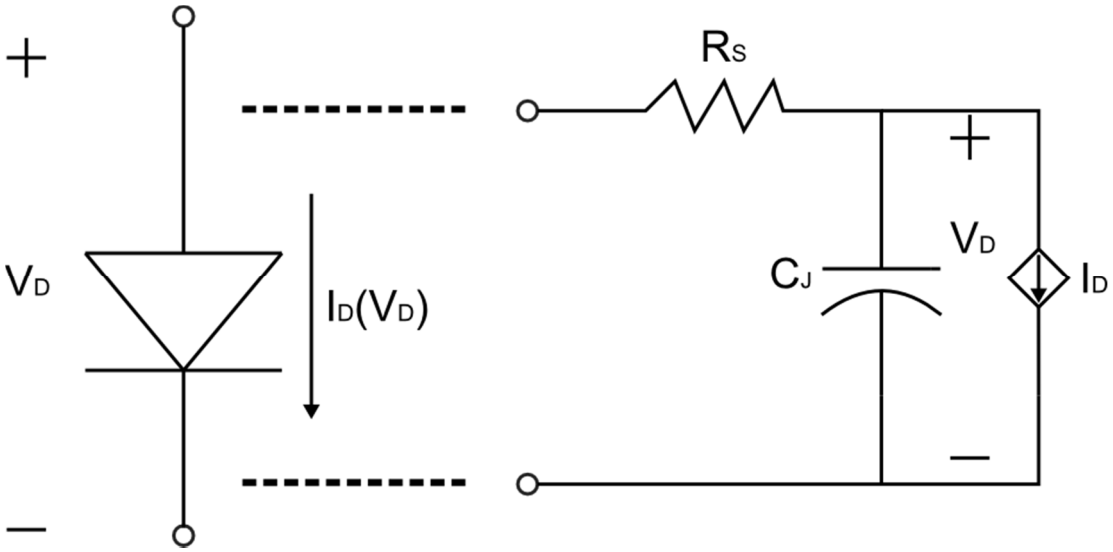

Figure 1-5: Schottky Barrier Diode and its small signal model

Table 1-2 summarizes the characteristics of various THz detectors in terms of performance parameters.

Table 1-2: Characteristics of various THz detectors

	Golay cell	Si FET	Si SBD	Pyroelectric	Bolometer
Responsivity (kV/W)	10-100	0.1	1	100	100-1000
NEP (pW/√Hz)	100	100	1	1000	0.1
Frequency range (THz)	0.2-20	0.1-8	0.1-10	0.1-30	0.1-30

1.6 CHAPTER SUMMARY

This chapter presents a state-of-the art review of the various THz sources and detectors based on their principle of operation. It also discusses the properties and applications of THz region. Some of the THz sources described above are not good enough for completely characterizing the THz detectors. Similarly, other monochromatic THz sources cannot be used to measure the spectral response of the detectors. For example, mostly QCL generates THz waves of only a single frequency, which is not electronically tunable, and thus it cannot be used to characterize THz detector for varying signal frequencies. On the other hand, the detectors are superior in performance but are usually marred with issues like huge area, complicated systems and high cost. Consequently, they have limited usage, mainly in scientific research and for defense and military related applications.

CHAPTER 2: THEORY OF CMOS BASED FET THZ DETECTION

Most of the THz devices mentioned in the last chapter are not feasible for applications demanding large volumes and high integration. Some of the mentioned technologies require cooling mechanism to maintain the cryogenic temperature which makes them bulky and power hungry, thus limiting their usage to only a few military related applications. Moreover, some of these detectors are fabricated using specialized processes and are thus incompatible to make up for a *single-die, monolithic* THz systems alongside the mainstream Si based microelectronic systems which are required to do the signal processing of the detected signal. This led the scientific community to find new solutions in order to realize THz systems that could be mass produced not just for research purposes and specialized fields, but also for commercial applications [50] [51] [52].

2.1 WHY CMOS?

Si technology provides a viable option to fabricate low cost, small size THz systems [46] [48]. There are numerous reasons to back up this claim:

1. **Maturity:** Si technology is mature in terms of yield and manufacturability and provides tremendous growth opportunity from the devices and system's point of view [55] [56]. In the image sensors field, this translates into performance improvement including an increase in resolution and high integration with more analog and digital circuits on the same silicon die with the sensor. Moreover, process modifications to standard CMOS technologies are also done to improve image performance and to mitigate various device related issues like dark current.
2. **Scaling:** Its ever shrinking device size allows the fabrication and development of cheap and highly integrated CMOS based THz prototypes and systems.
3. **Compactness:** Compared to some other devices, Si based systems are compact and do not require cooling mechanism to maintain cryogenic

temperature. Of course, this also means that these systems will have to compromise in terms of performance parameters [57] but their lack of performance can easily be traded with the advantages they offer, such as size, low cost and ease of manufacturing.

4. **Commercial aspect:** A monolithic THz system comprising of the sources, detectors and the electronic readout all fabricated on a single chip makes the use of commercially available CMOS technology all the more interesting and much compelling to use from an engineering and industrial point of view.

From the previous chapter, only SBD and FET are the two THz detectors that can be fabricated in the mainstream Si technologies and can take advantage of their numerous properties mentioned above. Thus, the rest of the thesis will be focused on discussing and designing only these Si based detectors and their systems.

2.2 FIELD EFFECT TRANSISTOR AS THZ DETECTOR

The functional and technological limitations of the nanometer CMOS technologies, and why it is difficult to design active circuits in THz region must be briefly addressed before understanding the working of FET as a direct THz detector. The highest operational frequency of CMOS device is limited by the electron transit time 'τ', which is defined by the device cut-off frequency 'f_T'$\left(\tau = \frac{1}{2\pi f_T}\right)$. Indeed, the device exhibits gain below this value and it is possible to design active circuits. Examples include power amplifiers, oscillators, filters and mixers fabricated in RF and microwave region and reported in [58] [59]. In the THz region, the electronic circuits had mostly consisted of heterodyne receivers which were made up of Monolithic Microwave Integrated Circuits (MMIC). However, owing to the absence of active devices due to limited f_T, the Low Noise Amplifier (LNA) in these receivers was typically limited to operate only in microwave range. The advances in Si process technologies have pushed the operational frequency range of the bipolar devices into Millimeter (mm) and lower end of THz regions, making it possible to design silicon integrated circuits here [23] [24] [33]. A review of the FET device physics can help in understanding its working in THz frequency range

It was proposed in [46] that electron inertia at THz frequencies provides delay between applied voltage and electron velocity, giving rise to *oscillations of electron density* known as plasma waves which propagate under the linear dispersion law given by:

$$\omega = sk \tag{2-1}$$

where 'ω' is frequency, 's' is wave velocity and 'k' is the wave factor. Furthermore, wave velocity is given by:

$$s = \sqrt{\frac{eU}{m}} \tag{2-2}$$

Where 'e' and 'm' are the electronic charge and mass, respectively and U is the gate-to-channel voltage signal swing. The wave velocity of plasma waves is of the order of 10^8 cm/s, which is much higher as compared to the drift velocity of the two-dimensional electrons (2DEG) in the FET channel. This factor makes it possible to use FET device in the THz regime, which is typically much above the limited electron transit time of the device.

These plasma waves operate in two modes: overdamped or resonant where the resonant mode can be used to generate THz radiations within the FET channel. Thus, as opposed to the continuous 2D flow of electrons from source to drain terminal within the channel, there are waves of electron density in plasmonic mode, propagating both in gated and ungated regions of the FET device. If the source terminal of the FET device is AC shorted and drain is left open circuited, then the fundamental frequency of oscillation of plasma waves under this particular boundary condition is:

$$\omega_0 = \frac{\pi s}{2L} \tag{2-3}$$

where L is the FET channel length. Consequently, if the resonant quality factor of plasma waves, which is a product of fundamental oscillation frequency ω_0 and plasmon decay time τ_P fulfills the following condition:

$$\omega_0 \tau_P \gg 1 \quad (2\text{-}4)$$

Then the FET device operates as a resonant detector. Otherwise, it operates in non-resonant mode and its response is a decreasing function of signal swing 'U' when the FET is exposed to electromagnetic radiations. It is worth mentioning here that FET device operating at THz frequencies are inseparable from circuits as issues related to the coupling plasma waves to electromagnetic radiation conversion, device sizes and parasitics and the integration with other submillimeter wave circuits need to be addressed. To understand these factors, modeling of the FET detector on the basis of circuit theory is critical which is explained in the folioing paragraphs.

2.3 MATHEMATICAL MODELING OF FET THZ DETECTOR

From an electrical point of view, the behavior of the FET device as a THz detector can be explained either by **Q**uasi-**S**tatic (QS) or **N**on-**Q**uasi-**S**tatic (NQS) modeling, depending on the operating frequency of the FET device. In the following sections, the difference between these two types of modeling is defined followed by the mathematical derivation of the equations that characterize the FET detector based on its operational frequency.

2.3.1 Quasi Static Modeling

QS Modeling is applicable at low frequencies in RF and microwave regions that are below the f_T of the transistor and is thus not limited by the electron transit time. The finite charging time within the channel is ignored as the signal oscillations and voltage variations are slow at the device terminals [60] [61]. FET is modeled as a lumped element and its behavior can be determined by analyzing the device on the basis of its biasing conditions [62]. For example, the channel current of the FET in saturation and linear regions are given by equations (2-5) and (2-6), respectively:

$$I_{DS} = \frac{\mu C_{OX}}{2}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \quad (2\text{-}5)$$

$$I_{DS} = \frac{\mu C_{OX}}{2}\frac{W}{L}[(V_{GS} - V_{th})^2(1 + \lambda V_{DS})] \quad (2\text{-}6)$$

where μ is the electron mobility, C_{OX} is the oxide capacitance, λ is the channel length modulation coefficient while W and L are channel width and length, respectively.

Consider the FET is biased at V_{GS} and an external capacitor C_{GD} couples the gate and drain terminals. In this configuration which is similar to resistive self-mixing principle [63], both channel conductance g_{DS} and drain–to-source voltage V_{DS} are modulated when the FET is excited by the time varying incident signal V_{RF} (t) as shown in Figure 2-1.

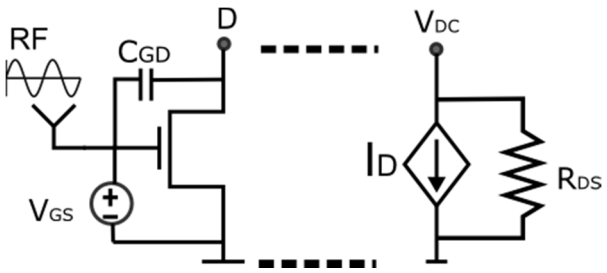

Figure 2-1: Quasi Static modeling of the FET device in RF range

The instantaneous value of the gate-to-source voltage v_{GS} (t) is:

$$v_{GS}(t) = V_{GS} + v_{gs}(t) \tag{2-7}$$

$$v_{GS}(t) = V_{GS} + V_{RF}\sin(\omega t) \tag{2-8}$$

Through the intrinsic capacitor C_{GD}, this signal is coupled to the drain terminal:

$$v_{DS}(t) = V_{RF}\sin(\omega t) \tag{2-9}$$

Since no drain current flows through the FET channel in the cold-biased configuration, FET is considered to operate in the linear region and can be modeled as a voltage controlled current source in parallel with the channel resistance:

$$i_{DS}(t) = v_{DS}(t)g_{DS}(t) \tag{2-10}$$

$$i_{DS}(t) = V_{RF}\sin(\omega t) g_{DS}(t) \tag{2-11}$$

Where $g_{DS}(t)$ is the drain-to-source conductance of the FET channel. In the linear (ohmic) region, it is given by:

$$g_{DS}(t) = \mu C_{OX}\left(\frac{W}{L}\right)\left[(V_{GS} + V_{RF}\sin(\omega t) - V_{th}) - \frac{V_{RF}\sin(\omega t)}{2}\right] \tag{2-12}$$

Putting $g_{DS}(t)$ in equation (2-10) and considering only the DC component:

$$I_{DS} = \mu C_{OX}\left(\frac{W}{L}\right)\frac{V_{RF}^2}{4} \tag{2-13}$$

And using,

$$V_{DS} = \frac{I_{DS}}{G_{DS}} \tag{2-14}$$

The rectified output voltage at the drain terminal is:

$$V_{DS} = \frac{V_{RF}^2}{4V_{OV}} \tag{2-15}$$

Equation (2-15) shows that the detected output voltage is a function of the input power as well as the biasing condition of the FET detector to a first degree of approximation. Moreover, the detected quantity can be either current or voltage which means that any electronic circuitry employed to do the signal processing of the detected signal can be operated both in voltage and current readout modes. It must however be noted that this model does not represent the behavior of the FET detector in the THz regime.

2.3.2 Non-Quasi Static modeling

The QS model and the equation describing the behavior of the FET transistor at RF and microwave frequencies do not remain valid for the THz region. This is because the signal oscillations at the THz frequencies are faster as compared to the charge carriers as they don't have enough time to travel along the entire channel. In this case, the channel can be considered as the distributed model with an infinitely small elements comprising of the unit element of time varying conductance g_N and FET

gate to channel capacitance is divided into unit segments $C_{N,OX}$ [56], as shown in Figure 2-2. The unit capacitance is:

$$C_{N,OX} = W\Delta x C_{OX} \tag{2-16}$$

And unit conductance has a position dependent conductivity 'G' which is a function of channel length segment Δx and time t:

$$g_N(v) = \frac{G(v(\Delta x, t))}{\Delta x} \tag{2-17}$$

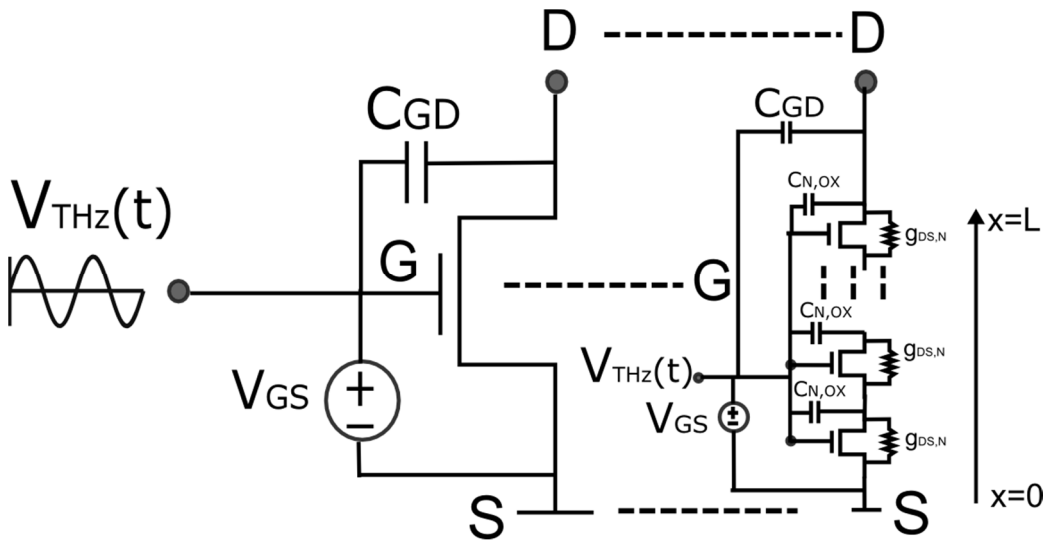

Figure 2-2: Non Quasi Static model of the FET device in the THz frequency range

where $g_N(v)$ is the conductivity per segment length Δx . By applying the Kirchhoff Current Law (KCL) and using the expressions for conductance and capacitance, a Partial Differential Equation (PDE) is derived:

$$\frac{\partial}{\partial l}\left[G\big(v(x,t)\big)\frac{\partial v(x,t)}{\partial x}\right] = C_{N,OX}W\frac{\partial v(x,t)}{\partial x} \tag{2-18}$$

This PDE has been solved in [65] and the results are deduced formulating the mixing process inside the FET channel. It is concurred that this mixing takes place due to the distributed nature of the FET channel which allows distributed resistive self-mixing. Infact, the THz signal doesn't travel through the entire channel and only a small portion of it, close to the gate and source terminals is responsible for the self-mixing.

Equation (2-18) is in close agreement to the result presented by Dyakonov and Shur in [46] which postulates the formation of plasma waves inside the FET channel as per the following PDE:

$$\frac{\partial}{\partial x}\left[G_{ds}(x)\frac{\partial v(\mathrm{x})}{\partial x}\right] = \left[-\left(\frac{c}{e}\right)\frac{\partial v(x,t)}{\partial x}\right] \tag{2-19}$$

which is closely related to the NQS analysis of the FET detector using distributed modelling of the device channel at THz frequencies.

2.4 WHY FET?

Both the FET and SBD which are discussed here and in the last chapter are examples of CMOS based THz detectors and can be employed as a single pixel or in array configuration [66] [67]. These detectors are cheap, easy to fabricate and are operated at room temperature with minimal power consumption. Infact, they can be implemented in large 2D arrays for various commercially driven applications like security imaging. As an example, the world's first 1k pixel THz camera consisting for FET THz detector for video imaging was presented in ISSCC in 2012 [68]. SBD based THz imaging arrays operating at the higher end of the THz spectrum was also presented [69].

The FET THz detector is probably the preferred choice in array implementations for imaging applications as opposed to the SBD due to following reasons:

1. FETs are readily available in all the standard CMOS technologies and can be easily implemented without any process modification. SBD's are also available in these processes but these cells are large, slow and not customizable.
2. FET devices can be easily optimized to increase their performance parameters (responsivity, noise) by changing device parameters like channel length (L), biasing and dimensions (W/L). A good experimental review of this fact will be presented in detail in Chapter 4.
3. Compared to SBD, FET is a 3-terminal device and it offers more degree of freedom as far as the device optimization is concerned. Indeed, channel conditions of the FET can be changed without biasing it with a current.

2.5 CHAPTER SUMMARY

In this chapter, principle of THz detection with reference to plasma wave oscillations inside the FET channel is discussed with the help of device physics. From the circuit theory perspective, QS and NQS models describe the behavior of the FET device when operated in the sub-THz and THz regions respectively. CMOS based devices offer many advantages in terms of low cost, scalability and integration and are considered to be a perfect fit for commercial THz based systems and applications. Moreover differences between two Si based detectors, SBD and FET are discussed. Owing to points mentioned in Section 2.4, the FET device is selected for implementation as a THz detector in this thesis work. The rest of the thesis focuses on the measurement techniques and implementation of the FET based THz systems but most of the underlying principles can also be applied to any direct detector such as SBD.

CHAPTER 3: MEASUREMENT TECHNIQUES FOR DIRECT THZ DETECTORS

Implementation of direct detectors in CMOS technologies and measuring their performance parameters in the real world scenario is not trivial. This chapter discusses various measurement methodologies that can be applied to accurately measure the performance parameters of direct THz detectors. These methodologies are applied on a FET THz detector and the results are presented.

3.1 REQUIREMENTS FOR MEASUREMENT SETUP

The characterization of detectors for imaging applications in general demand much attention and require carefully calibrated measurement techniques. This is even truer in the THz range where the available sources and detectors are limited in power and sensitivity. Some of the underlying challenges are the following:

1. While there are various solutions for the guided-mode characterization, the direct detectors by nature need to be measured using free space propagation. This means that both the optical and electrical setup and apparatus must be used to define a relevant measurement methodology that must be able to deal with a number of issues including the way the THz waves are affected by the atmosphere absorption, reflections, beam focusing, etc.

2. The measurement setup must be able to detect a very low intensity signal in the presence of thermal noise of the detector, as well as to reject the electromagnetically and electronically induced interference signals of the transmission medium and electronic circuitry.

3. Due to the limitation of the emitted power of the commercially available THz sources, the distance between the transmitter and receiver cannot exceed beyond a few tens of centimeters as atmospheric attenuations and path losses become extremely significant [70].

4. High signal-to-noise ratio (SNR) at the output of the detector is necessary for a reliable characterization. A lock-in measurement technique facilitates the detection of this low intensity rectified signal by increasing the SNR of the measurement.

3.2 ELECTRICAL AND OPTICAL PERFORMANCE PARAMETERS

3.2.1 Input power

With reference to the characterization methodology involving free-space test setup used for THz detectors, the power that is available at the interface between the transmission medium and receiving antenna is referred to as the optical input power, while the power that is received by the detector is referred to as the electrical input power. The electrical power received by the detector is a function of the matching network between the receiver antenna detectors along with efficiency, polarization and alignment of the transmitting and receiving antennas. The optical input power is more application and performance oriented as compared to the electrical input power. The optical input power is a function of power density P_D and effective area A_{EFF} and is given by:

$$P_{IN} = P_D A_{EFF} \tag{3-1}$$

Amongst all the measurable quantities required to characterize THz detectors, the most important is the accurate measurement of the input power of the receiver as this directly affects all the performance parameters. A few techniques to measure this input power of the receiver have been reported as part of the characterization process of THz detectors for both single-pixel and focal plane array (FPA) configurations. For example, [68] and [65] reported an active imaging THz scheme for an FET-based FPA in a standard CMOS technology in which the input power was calculated using a Friis transmission equation and a similar approach to characterize an SBD array at an 860-GHz frequency was also reported in [69].

3.2.2 Effective area

The ability of the receiving antenna to extract power from incident THz radiations is defined by the effective area of the detector A_{EFF}. For detectors with only general absorber of the incident radiations or for the so-called aperture antennae (i.e. dish antennae), the physical area (A_{PHY}) of the absorber is coincident with A_{EFF} and measuring only one of them is enough for the effective area and power density calculations. However, in the general case of the detectors that capture incident radiations through an antenna, A_{EFF} is almost always different from A_{PHY} and hence the effective area A_{EFF} must be measured for a precise detector characterization. Mostly, A_{EFF} is larger than A_{PHY} since an antenna typically captures the impinging radiations on a wider area than its physical size. A_{EFF} is also a function of the receiver antenna directivity and the signal frequency. Thus, if D is the directivity of the receiver antenna in the radiation direction, λ is the wavelength of signal frequency f_{SIG} and c is the speed of the light, then A_{EFF} is given by [71]:

$$A_{EFF} = \frac{D\lambda^2}{4\pi} = \frac{D}{4\pi}\left(\frac{c}{f_{SIG}}\right)^2 \tag{3-2}$$

indicating that the more directive antennae will have a larger effective area. One method to characterize FET detector was used in [72] in which the effective area (A_{EFF}) was calculated by measuring the spatial response of the detector.

3.2.3 Polarization matching

Polarization refers to the orientation of the plane which contains the electric field portion of the radiating wave and it is defined in the far field [73]. Mostly, antennae have either linear or circular polarization. Linear polarization can either be vertical or horizontal. Just like electrical matching, the polarization matching is extremely important for the efficient transmission of the radiation waves. The polarization efficiency varies from 0 to 1 with '0' representing a complete mismatch or cross-coupled configuration while '1' represents a complete matching between the radiated wave and the polarization state of the receiver antenna.

THz detectors which are sensitive to linear polarization should be illuminated with proper polarization and those which are sensitive to circular/elliptical polarization or

with dual polarization antennae need to be characterized with both the horizontal and vertical polarization configurations. A complete characterization includes the variation of responsivity and NEP with respect to the polarization angle.

3.2.4 Antenna directivity

The directivity of an antenna is defined by the ratio of its power density in a fixed angular direction to the power density of an isotropic antenna in that direction [73]. Mathematically, it can be written as:

$$D(\theta,\phi) = \frac{P_a(\theta,\phi)}{\left(\frac{P_I}{4\pi r^2}\right)} \tag{3-3}$$

3.3 MEASUREMENT OF IMPINGING POWER

To explain the measurement of impinging power, consider the setup shown in Figure 3-1 consisting of a reference pyroelectric detector placed at a distance (d = 15 cm in this setup) in the line of sight with the THz transmitter antenna. This is a specific setup which can be modified as the same measurement techniques can be used with other sources. The THz source is a continuous wave (CW) frequency synthesizer capable of producing signal of several Gigahertz (GHz) which is further multiplied through the frequency multiplier chain to generate the THz signal making it an electronically tunable THz source. The synthesizer is amplitude modulated, so that lock-in techniques can be used to remove the low-frequency noise and offset, enabling detection of the weak signal of the detector. Moreover, the CW synthesizer base frequency can also be tuned using an automation software program in order to adjust the THz source to do the frequency sweep analysis of the detector. On the receiver side, the detector is biased by a power supply and its voltage response is measured using a lock-in amplifier. The receiver can be properly aligned and positioned in free space using an electrically controlled positioning system, which is capable of adjusting the Device-Under-Test (DUT) in all three dimensions (x, y, and z). Moreover, the THz source can be turned ON or OFF through an electronic switch to measure the noise generated due to the electronic setup. In the following

paragraphs, a comparative analysis of some of the methods used to characterize the optical input power of the THz detector is explained.

3.3.1 Method 1: Input power measurement using a reference detector

This method is based on the use of a reference detector in the characterization measurement setup to measure the optical power density of the reference detector (P_{DR}) at the sensor plane. The P_{DR} is then multiplied with the A_{EFF} of the FET THz detector in order to measure the optical input power P_{IN}. This approach has the following advantages:

1. It eliminates the requirement of knowing the transmitter specifications like the antenna gain, directivity etc.

2. It measures P_{IN} based on the THz waves *after* they encounter the atmospheric path losses and attenuations, and any optical element (lenses, mirrors). This allows an accurate estimation of the impinging THz power since it takes into consideration the signal lost during propagation through the medium.

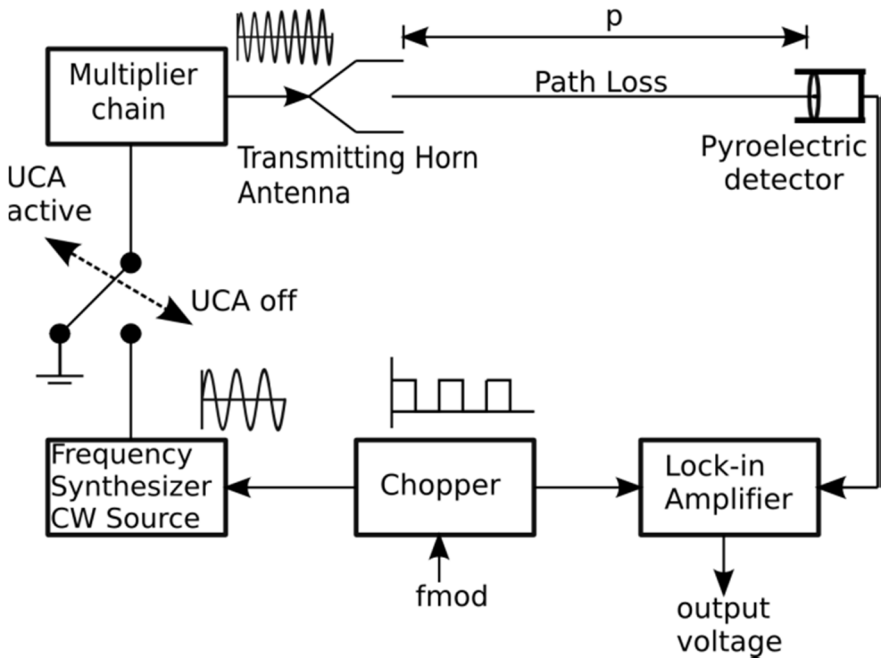

Figure 3-1: Test and measurement setup used to characterize direct THz detectors

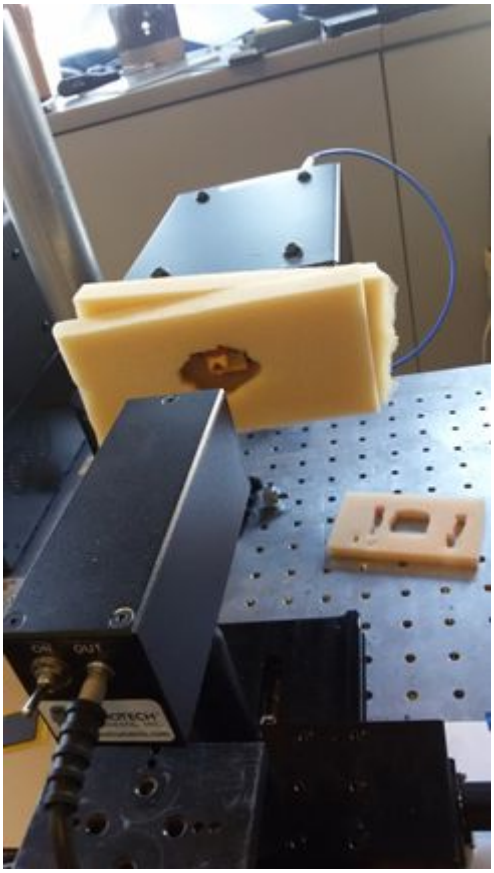

Figure 3-2 Laboratory setup involving a THz source and pyroelectric detector

As shown in Figure 3-2, the reference pyroelectric detector receives THz waves through an opening of diameter and area A_{PYRO}. Its voltage response V_{PYRO} is measured by varying the THz signal frequency source. Due to reflection, the THz waves during propagation through the transmission medium generate nodes and antinodes, as shown in Figure 3-3. This is clearly a measurement artifact which is caused by the constructive and destructive interference of the waves between the source and the receiver and it needs to be corrected for a reliable characterization. Since this artifact is setup specific, it varies if the pyroelectric detector is replaced by the DUT like FET or the SBD; removing it, the occurrence of unrealistic peaks in the responsivity and NEP measurement results is avoided. For example, this can be done by applying a moving average filter in the frequency domain.

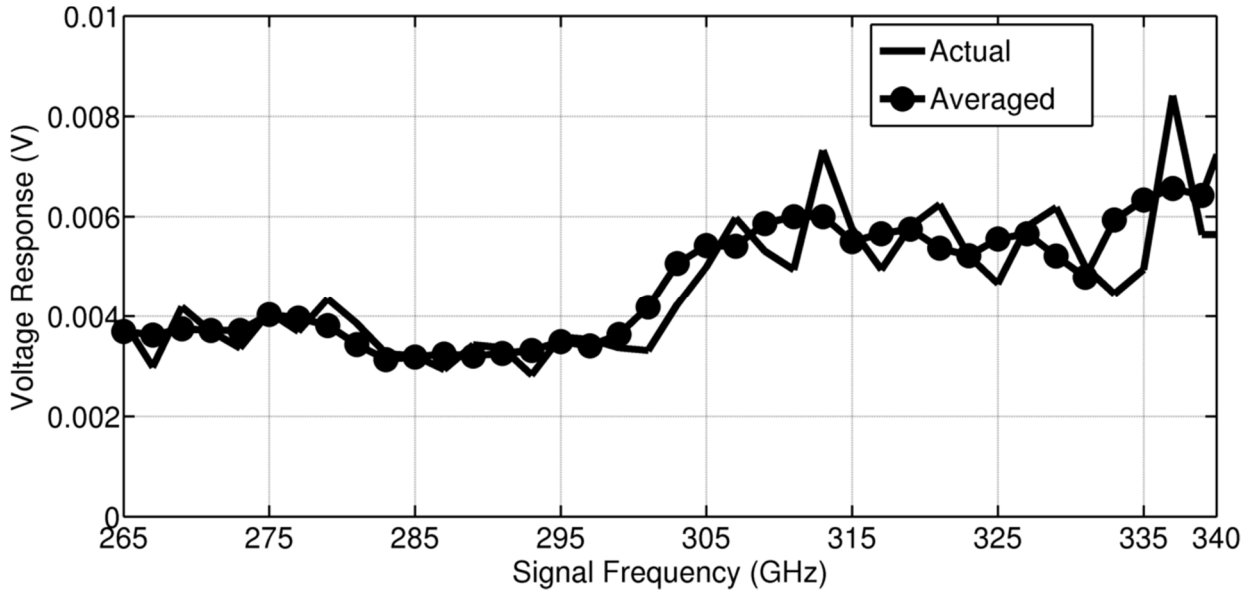

Figure 3-3: Measured voltage response of the reference (pyroelectric) detector vs. THz signal.

Looking at the graph it is evident that the peaks are spaced at several gigahertz signal frequency for a setup with distances ranging in the centimeter between the transmitter and the detector. Thus enough samples need to be taken in order to carry out smooth averaging. Based on the voltage response of the pyroelectric detector, the input power received by it P_{PYRO} is obtained by dividing the detected response V_{PYRO} with the voltage responsivity of the pyroelectric detector R_{PYRO} provided by the manufacturer. This input power received by the pyroelectric detector is shown in Figure 3-4 and using this data, the power density at the pyroelectric detector plane is obtained by dividing P_{PYRO} by its area A_{PYRO}. Note that this input power density of the pyroelectric detector is measured without the use of the transmitter antenna specifications, and it considers path losses. Obviously, proper manufacturer calibration is necessary to calculate the power density by means of R_{PYRO}. The spatial distribution of power is also needed for the evaluation of input power received by the test structure and thus for complete characterization of direct THz detectors. The spatial distribution plot typically reveals the received power distribution in free space [74].

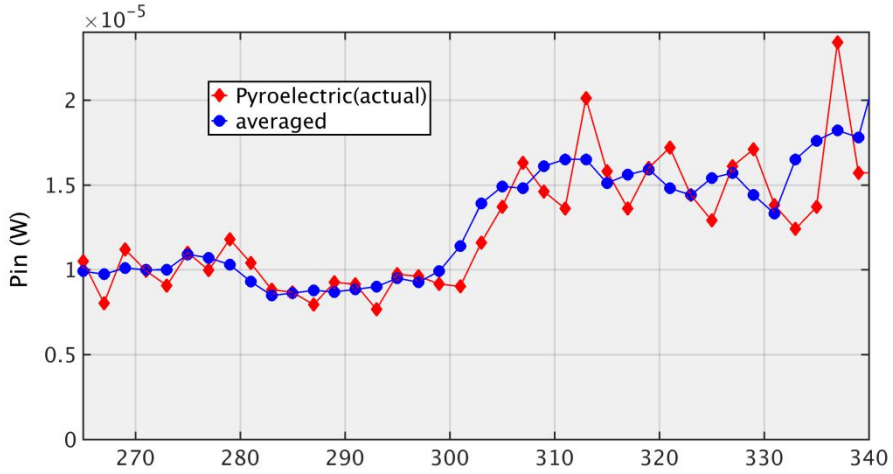

Figure 3-4: Input power of pyroelectric detector vs. signal frequency.

This can be obtained by scanning the detector in geometrical (x, y) coordinates to calculate its impinging power density as a function of these coordinates. The correct evaluation of the impinging power depends on the size of the source beam at the measurement plane and on the dimensions of the DUT. The measurement results of the spatial distribution of the pyroelectric response are shown in Figure 3-5 which can be used to determine the power at the detector plane.

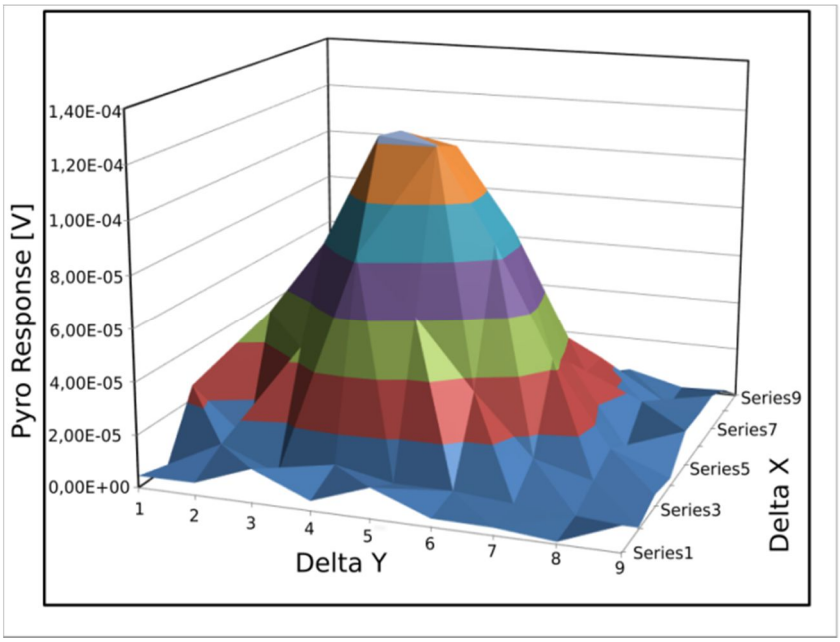

Figure 3-5: Spatial Distribution plot of the pyroelectric response for the source characterization method.

The graph shows the voltage response of the pyroelectric detector as a function of the detector movement from origin in x and y coordinates. This plot helps in determining the spatial resolution which can be obtained by measuring the Full-Width-at-Half-Maximum (FWHM) value by referring to the geometrical coordinates with maximum response.

3.3.2 Method 2: Input power density measurement using Friis transmission equation

Another method to calculate the P_{IN} is the use of the Friis transmission equation [75] [76]. For this purpose, a similar test setup as the one shown in Figure 3-1 was used. Friis transmission equation states that if P_T is the power transmitted by the THz source, G_T is the gain of the transmitting antenna and A_{EFF} is the effective area of the DUT that is illuminated by the THz radiation, then the power P_{IN} received by the DUT is:

$$P_{IN} = \left(\frac{P_T G_T}{4\pi p^2}\right) * A_{EFF} \tag{3-4}$$

It is evident from equation (3-4) that calculation by the Friis transmission equation requires the exact transmitter antenna specifications. Moreover this method does not allow taking into account specific setup and path losses, the most notable of which is the variation of the spectral power distribution in the presence of optical elements (e.g. lenses). Infact, the impinging power at the detector is modified along the transmission path as a significant part of this power is lost in the surrounding atmosphere due to attenuations along the path, and any refractive or reflective optical elements between the source and detector. Anyway, if the source specifications are precise, this method underestimates responsivity and NEP as the calculated P_{IN} is the upper bound of the real impinging power.

3.4 MEASUREMENT OF EFFECTIVE AREA

Equation (3-1) shows that A_{EFF} depends on P_{IN} so the calculation of A_{EFF} on geometrical consideration is generally wrong [77]. In this section, some measurement methods are explained.

3.4.1 Method 1: Effective Area Measurement Using Antenna Directivity

A_{EFF} can be calculated using the directivity of the receiver antenna, which can be determined by measuring the receiver antenna radiation patterns in spherical coordinates [73]. This measurement can be performed in a way similar to the one shown in the test setup of Figure 3-1 but by rotating the receiver antenna over its E and H planes. The radiation patterns on the two cut planes are determined by measuring the detector output voltage. A cut plane is considered to be a 2D slice of a 3D radiation pattern so the directivity can be extracted from these cuts and not just from entire 3D pattern [73]. Polar plots of these normalized radiation patterns are shown in Figure 3-6. Considering these to be narrow beam width radiation patterns with θ_1 and θ_2 as the half-width maximums of the E and H planes respectively, the directivity can be calculated by any of the following two formulas [78]:

$$D = \frac{4\pi}{\theta_1 \theta_2} \tag{3-5}$$

$$D = \frac{32ln2}{{\theta_1}^2 + {\theta_2}^2} \tag{3-6}$$

Generally, the directivity values obtained using equation (3-5) and (3-6) can be used to calculate to calculate A_{EFF} by inserting these calculated values in equation (3-2). As an example, D values based on the antenna radiation patterns of were considered for the resulting A_{EFF} graph in Figure 3-7.

3.4.2 Method 2: Effective Area Measurement Using Deconvolution

Another method to calculate the effective area of the receiver is by measuring the spatial response of the THz beam [79]. For this purpose, the characterization and acquisition of the THz beam is performed and a deconvolution method, such as the fast Fourier transforms or the Richardson Lucy algorithm is applied on the acquired data [80] [81].

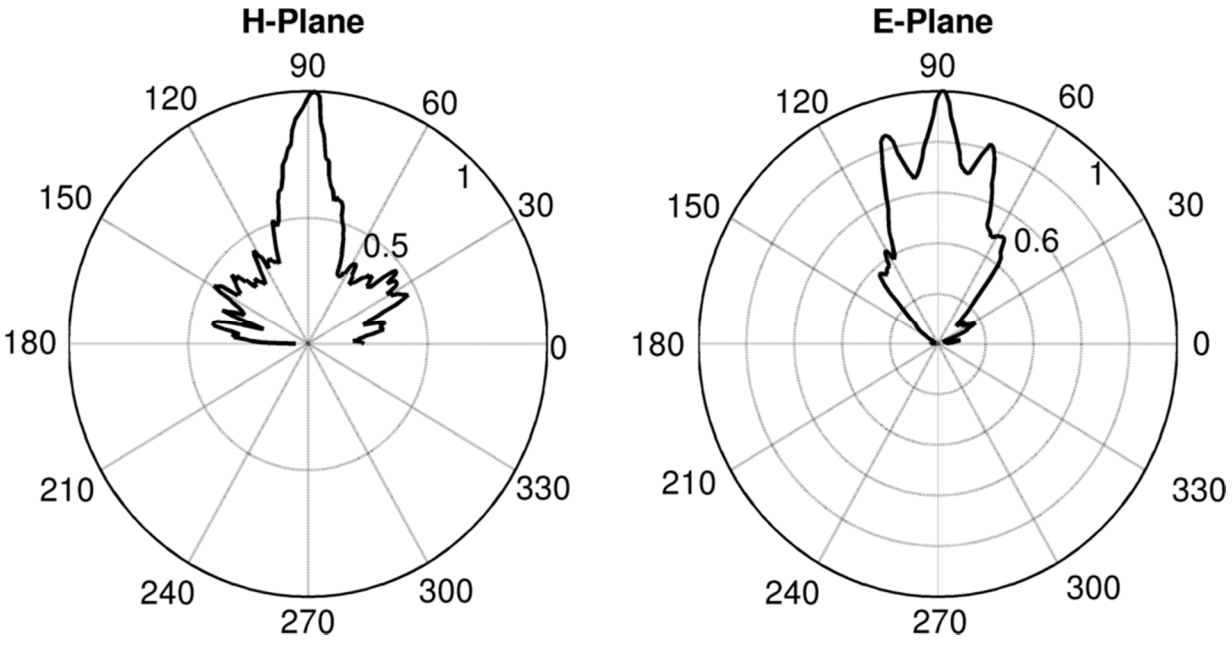

Figure 3-6: Normalized polar plot of the on-chip antenna radiation patterns for H and E planes

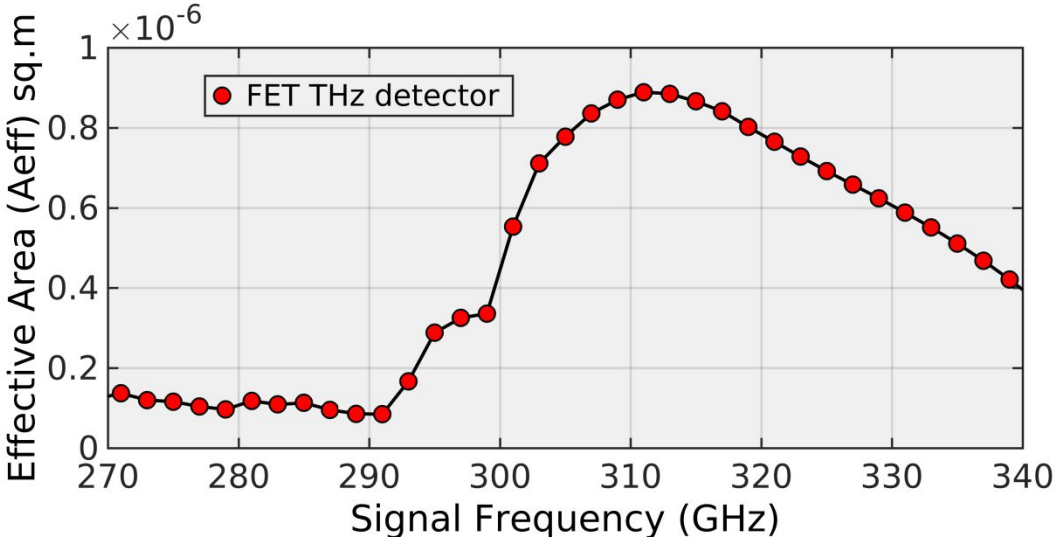

Figure 3-7: Measured effective area illuminated by the impinging THz radiations

Considering that the THz source is tightly focused, under certain hypothesis it can be modeled as a Point Spread Function (PSF) defined by the Airy pattern I(x, y). The PSF describes the response of an imaging system to a point object or source and is sometimes referred to as the impulse response of the source or tightly focused beam. The measured beam S(x, y) at the receiver is a convolution function of I (x, y) and the spatial response of the THz detector R(x, y). Mathematically, it can be written as:

$$S(x,y) = I(x,y) * R(x,y) \tag{3-7}$$

where x and y define the detector plane.

The detector's spatial response R(x, y) can be measured by applying the deconvolution of S (x, y) and I(x, y). As a result of deconvolution, the resulting pattern contains the effective capturing area of the receiver antenna illuminated by impinging radiation. This technique was applied to characterize the FET-based THz detector, and the effective area is shown in Figure 3-8. A_{EFF} calculated using the directivity measurements and spatial response were found to be in close agreement. This approach has both merits and demerits: It gives additional information on the shape of the receiving area that is particularly interesting in the presence of other interfering structures such as in arrays.

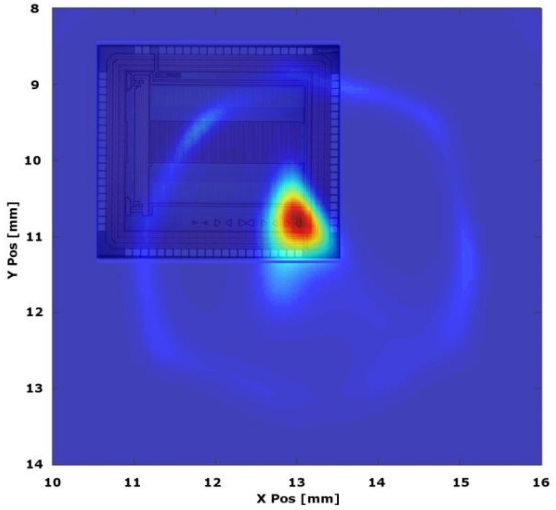

Figure 3-8: Measured effective area of the receiver antenna as determined by the spatial response. The halo is produced by the lens which can be neglected.

One drawback is that it takes a long time to measure the spatial response of the detector. Hence, A_{EFF} calculation using the antenna directivity is more feasible.

3.5 BACKGROUND NOISE

Ideally, there should not be any detector response in the absence of THz waves which means that when the THz source is turned off, the detector output voltage should be zero. However, a common issue in this measurement and test setup is electronically and electromagnetically induced noise [82]. This noise, in presence of low-amplitude signals as in case of THz detectors, can easily reach levels which are comparable to the quantities to measure. This noise is commonly referred to as Background Noise (BN) and there can be many sources depending on the setup configuration. For example, among these sources there is the continuous signal of the power supply hum at a 50-Hz frequency, or the impulse noise due to switching signals such as the amplitude modulation controls of the test setup. Since a free-space measurement method is used for THz detection, the BN can couple to the receiver by both radiation and conduction. Coupling of the BN through radiation has already been considered using the proposed modulation methodology in the previous section. Coupling by conduction takes place through power cables and signal routes.

This noise can be removed by taking measurements readings with and without an optically blocking element (for example, iris) in the propagation path and subtracting them together, obtaining only the signal in the end. However this is a slow and time consuming procedure which is problematic in the cases where a lot of readings need to be taken to calculate performance parameters for bias and frequency response. An automated operation is usually required for efficiently taking these readings. This objective can be achieved by doing a small modification in the test setup is done as shown in Figure 3-1. An electronically controlled switch User-Controlled Attenuation (UCA) is used to turn the final section of the THz source ON and OFF and to perform two measurement readings with all the other RF and modulation signals running. Alternatively, the use of an iris in the radiation path can do the same job but in this case a compromise has to be made in terms of less

measurement automation and speed. The BN subtraction operation takes place by altering the state of the UCA.

When the UCA is active, the THz source is completely attenuated and the noise reading is measured. When the UCA is inactive, the output voltage includes the detector response as well as the BN. By so doing, the net voltage response of the THz detector is achieved after removing the BN from the detector response. The time constant of the filter in the lock-in amplifier defines the settling time of the output and the UCA switching speed is set as a function of this time constant. Referring to the measurement setup, if indeed a lock-in amplifier is used for signal detection and the time constant of the lock in amplifier must be set to a large value, then it is important to wait for enough time periods of the lock-in amplifier for complete settling of the output response before the UCA switches its state. Usually the UCA switching time is set equivalent to 5 times the time constant of the filter in the lock-in amplifier which allows one to see the complete effect on the lock-in signal.

Looking at Figure 3-9, the results indicate that the BN through coupling is more significant whenever the detector output impedance is high, which with FET detectors happens at low bias voltages in the subthreshold region. In these measurements the lock-in time constant was set to 100 ms and thus 500 ms were allocated for a single UCA state, allowing enough time for the UCA to settle.

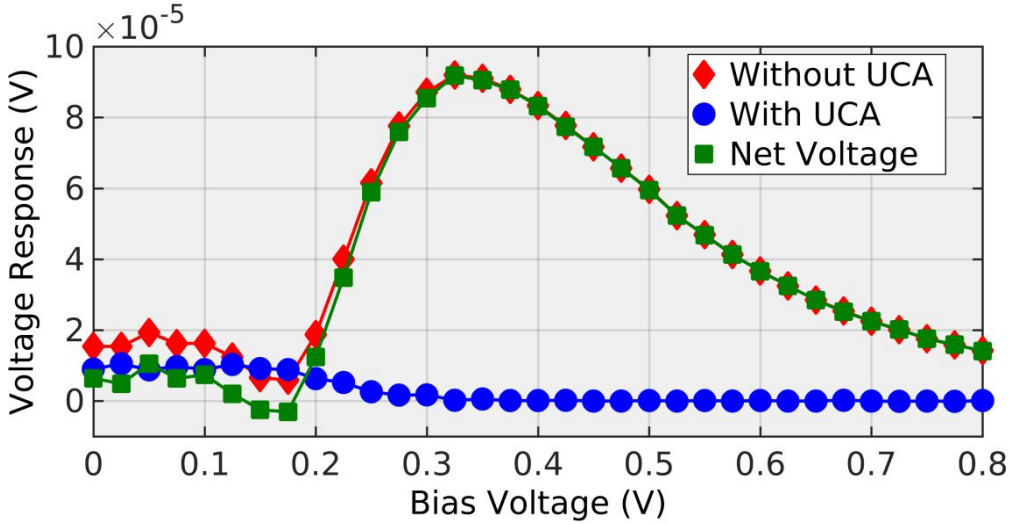

Figure 3-9: Background noise: includes measurement readings with and without the UCA while the net response is determined by subtracting the two readings together.

3.6 EXAMPLE OF FET CHARACTERIZATION RESULT

An antenna coupled FET detector was fabricated in the standard 0.18 µm CMOS technology as shown in the Figure 3-10 and the performance parameters of the detector were measured [83]. Some of the results are presented in the following paragraphs:

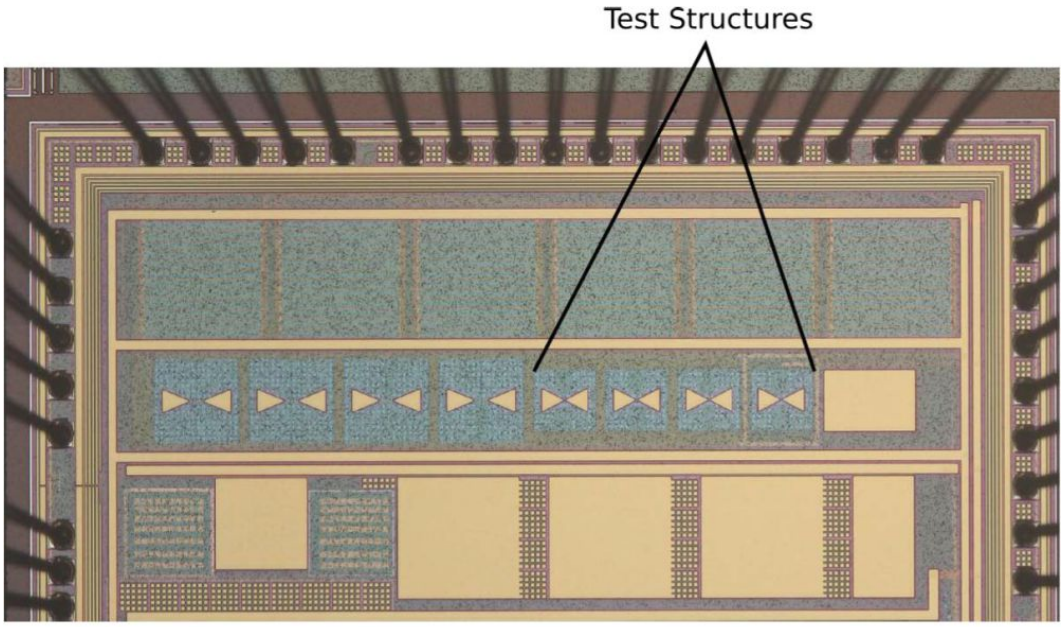

Figure 3-10: Chip micrograph showing antenna-coupled FET structures

3.6.1 Voltage Responsivity and NEP

The measured antenna directivity and the power density of the reference pyroelectric detector were used to calculate the A_{EFF} which in this experiment was calculated to be 0.4 µm^2 at the signal frequency of 300 GHz. This was in close agreement to the physical area, calculated to be 0.25 µm^2. Furthermore, Input power as received by the FET detector was calculated based on area measurements and this is used to calculate the responsivity and the NEP by substituting the values in equations (3-1) and (3-3), respectively.

A frequency sweep analysis was performed by sweeping the THz source at a fixed gate bias voltage V_{GS} of the detector and the responsivity curves were obtained by dividing V_{DET} by input power P_{IN}. The responsivity curves as a function of FET gates bias voltage and THz signal frequency are shown in Figure 3-11 and Figure 3-12, respectively.

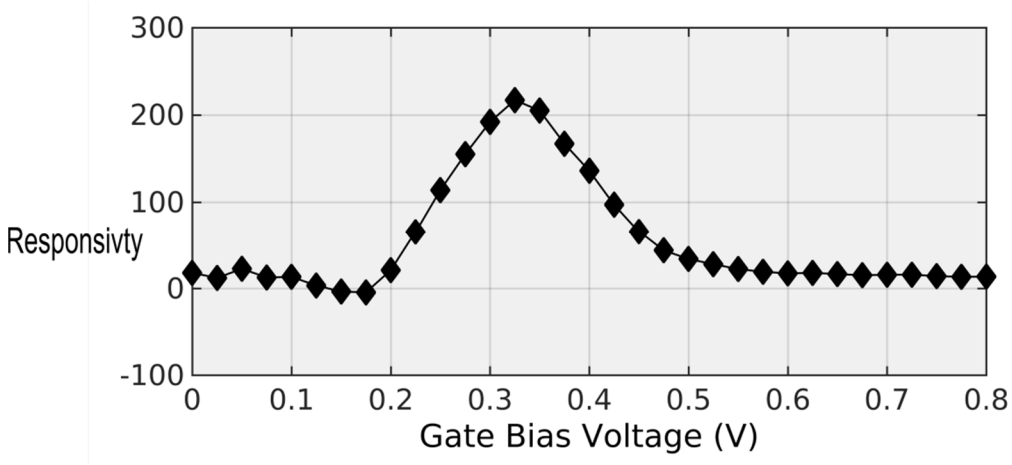

Figure 3-11: FET THz detector voltage responsivity vs. gate bias voltage at 300 GHz

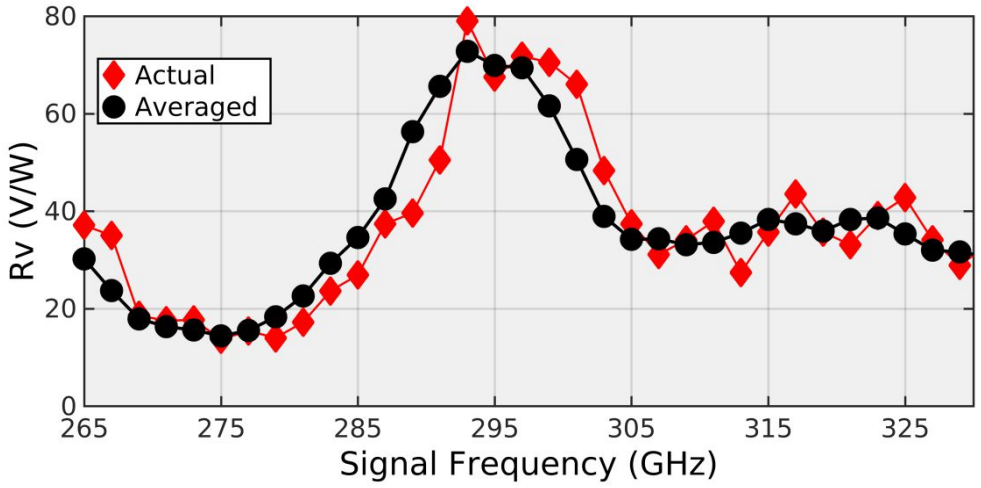

Figure 3-12: FET THz detector voltage responsivity vs. Signal Frequency at 0.45 V

Furthermore, the intrinsic resistance R_{DS} of the FET detector is measured using a DC multimeter. The thermal noise spectral density of the FET is a function of this resistance and is given by:

$$\frac{{V_{TH}}^2}{\Delta f} = 4kTr_{DS} \tag{3-8}$$

Based on the thermal noise values and responsivity graph, the NEP of the FET was calculated and it is plotted in Figure 3-13 as a function of the FET gate bias voltage achieving a minimum value of 140pW/sqrt (Hz).

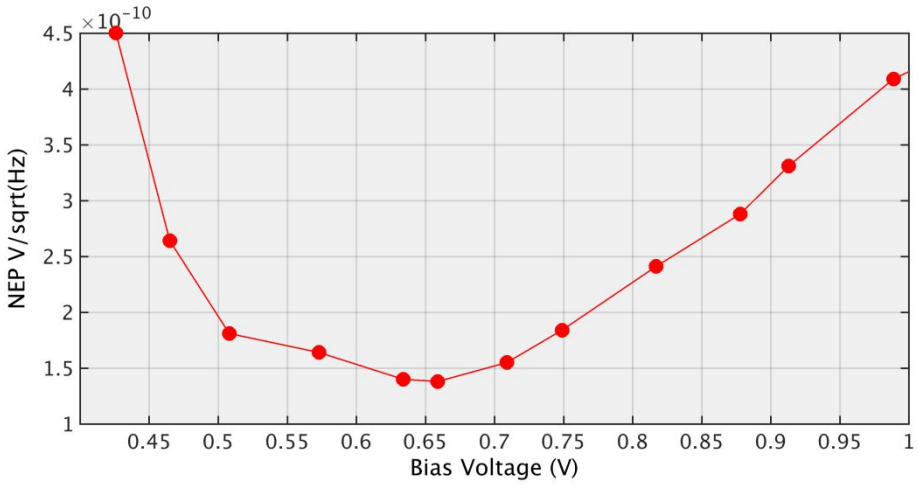

Figure 3-13: NEP vs. gate bias voltage at 300 GHz signal frequency.

3.7 CHAPTER SUMMARY

This chapter presents an overview of the measurement techniques for the measurement of various performance parameters of the FET based THz detectors. Special emphasis has been put on two quantities: the impinging input power and the effective area. The advantages and disadvantages of various measurement techniques are discussed. As an example, a FET detector fabricated in standard CMOS technology is characterized using a reference pyroelectric device and its effective area is measured using the on-chip antenna directivity while input power is evaluated using a pyroelectric detector. This method of power measurement based on the use of a reference device considers path losses and atmospheric attenuation, and is thus more reliable and gives an accurate estimation of performance parameters. Moreover, the measurement setup is very robust to EM induced noise due to the BN subtraction.

CHAPTER 4: SIMULATION AND OPTIMIZATION OF FET-BASED DIRECT THZ DETECTORS

In this chapter, FET-based direct THz detectors are discussed in detail from the design, configuration and optimization point of view. Their performance parameters are defined using various device models and the resulting expressions are simulated using SPICE [84] and MATLAB [85]. In addition, several configurations of the FET detector based on variation in topologies and device sizes have been implemented and tested on-chip in standard CMOS technology. The validation of FET device as a THz detector, the optimization of its performance by changing device parameters as well as the investigation of different FET detector configurations based on THz radiation coupling is important to understand its behavior when implemented as a single pixel or in an array configuration in a real-time environment. This helps in drawing useful conclusion to extract system level requirements in order to design an optimized readout interface.

4.1 PERFORMANCE PARAMETERS OF THE DIRECT THZ DETECTORS

Direct THz detectors are usually characterized by the following main performance parameters.

4.1.1 Responsivity (R)

Responsivity can be expressed either in voltage or current mode, depending on the measured quantity, and it is defined as the detector response for a given input power P_{IN}. The voltage and current responsivity are expressed in the units of [V/W] and [A/W], respectively. If V_{DET} and I_{DET} represent the detected voltage and current responses respectively and P_{IN} is the received input power, then the mathematical expressions of the voltage and current responsivity respectively are given by:

$$R_V = \frac{V_{DET}}{P_{IN}} \quad \left[\frac{V}{W}\right] \tag{4-1}$$

$$R_I = \frac{I_{DET}}{P_{IN}} \quad \left[\frac{A}{W}\right] \tag{4-2}$$

4.1.2 Noise Equivalent Power (NEP)

NEP of the direct detector is defined as the P_{IN} that is required to achieve an SNR of unity at the detector output. Alternatively, it corresponds to the detector intrinsic noise measured at a specific frequency for a bandwidth of 1 Hz divided by the responsivity. If V_N and I_N represents the noise voltage and current spectral density of the detector respectively, then the voltage and current NEPs expressed as [W/sqrt (Hz)] are:

$$NEP_V = \frac{V_N}{R_V} \quad \left[\frac{W}{\sqrt{Hz}}\right] \tag{4-3}$$

$$NEP_I = \frac{V_N}{R_I} \quad \left[\frac{W}{\sqrt{Hz}}\right] \tag{4-4}$$

4.1.3 Dynamic Range

The dynamic range (DR) is defined by the output voltage of the of the FET detector and it is the ratio of the maximum voltage level of the FET output to the Minimum Detectable Signal (MDS) which is defined by the noise floor of the detector [86]. The photo-electric response ΔU is proportional to the derivative of channel conductivity with respect to the FET gate bias voltage V_{gs} [87]. Thus it can be written as:

$$\Delta U = \frac{U_a^2}{4}\left[\frac{1}{\sigma}\left(\frac{d\sigma}{dV_{gs}}\right)\right]_{V_{gs}=0} \tag{4-5}$$

Where σ is channel conductivity and U_a is the impinging signal amplitude coupled to the detector between its source and gate terminals. Efficient detectors have high responsivity and dynamic range, as well as low NEP values [88]. Considering P_{IN} to be the electrical input power of the THz detector, Z_{IN} to be the input impedance of the FET detector and V_{IN} as the input signal amplitude:

$$P_{IN} = \frac{{V_{IN}}^2}{Z_{IN}} \tag{4-6}$$

By inserting this P_{IN} expression in equation (4-1), R_V is:

$$R_V = \left(\frac{{V_{RF}}^2}{4V_{OV}}\right)\left(\frac{Z_{IN}}{{V_{RF}}^2}\right) = \frac{Z_{IN}}{4V_{OV}} \tag{4-7}$$

Equation (4-7) implies that R_V is a function of the input impedance and the biasing voltage of the FET detector [89]. If C_{GS} represents the intrinsic gate-to-source capacitance and R_{DS} is the drain to source resistance, then the input impedance Z_{IN} of the FET detector is:

$$Z_{IN} = \left(\sqrt{\frac{R_{DS}}{j\omega C_{GS}}}\right) || \left(\frac{1}{\mathrm{j\omega C_{GS,OV}}}\right) \tag{4-8}$$

4.2 SPICE SIMULATIONS

4.2.1 BSIM model

In order to analyze FET behavior, SPICE simulations are performed using simulation testbench of Figure 4-1 assuming that the antenna feeds the THz signal to the FET detector with 50Ω characteristic impedance. FET is biased at V_{GS} and a sinusoidal voltage source emulating the THz signal is used to excite the transistor.

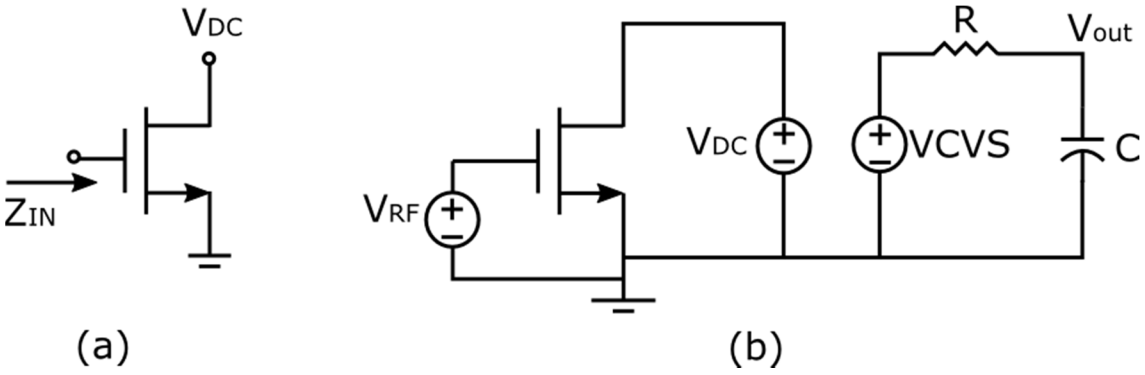

Figure 4-1: Simulation setup used to determine the performance parameters

A **V**oltage **C**ontrolled **V**oltage **S**ource (VCVS) reads the FET output signal which is then passed through a Low Pass Filter (LPF) with a very low cut off frequency set by the resistance R and capacitor C values, to extract the DC signal. The V_{DC} generator in simulation testbench senses the voltage detected at the drain terminal of FET device. The FET detector was simulated in a standard 0.35 µm CMOS process with main technology and device parameters [90] as outlined in Table 4-1.

Table 4-1: Technology and device parameters

Parameters	Description	Values
V_{th}	Nominal Threshold voltage	0.72 [V]
η	Subthreshold factor	1.4
µ	mobility	330 [m^2/V.s]
k_N	Transconductance parameter	140µ [A/V^2]
L	Channel length	0.35 [µm]
W	Device width	varying

4.2.2 EKV model

This model analytically describes the behavior of transistor in weak, strong and moderate inversion, both in saturation and linear regions. In EKV model, MOS drain current is considered to be a combination of forward (I_F) and reserve (I_R) currents and is given by:

$$I_D = I_F - I_R \tag{4-9}$$

$$I_D = 2k_n V_T^2 \eta \left(\frac{W}{L}\right)(i_F - i_R) \tag{4-10}$$

Where V_T is the thermal voltage and the normalized forward and reverse currents i_F and i_R are given by:

$$i_F = \left[\ln\left(1 + exp\left(\frac{V_P - V_S}{2V_T}\right)\right)\right]^2 \quad (4\text{-}11)$$

$$i_R = \left[\ln\left(1 + exp\left(\frac{V_P - V_D}{2V_T}\right)\right)\right]^2 \quad (4\text{-}12)$$

where V_D and V_S represent drain and source voltages referred to substrate and V_P is effective pinch-of voltage given by:

$$V_P = \frac{V_{gs} - V_t}{\eta} \quad (4\text{-}13)$$

Referring to [91], using equations (4-11) and (4-12) and doing Taylor expansion, the drain current expression becomes:

$$I_D = \mu_n C_{OX} \frac{(2-\eta)}{8}\left(\frac{W}{L}\right)\frac{exp\alpha}{2cosh\alpha} \quad (4\text{-}14)$$

If Z_{ANT} is the input impedance of the antenna, then the current responsivity is:

$$R_I = \mu_n C_{OX} \frac{(2-\eta)}{8}\left(\frac{W}{L}\right)\frac{exp\alpha}{2cosh\alpha} Z_{ANT} \quad (4\text{-}15)$$

while factor α is give as:

$$\alpha = \frac{V_G - V_{th}}{2\eta V_T} \quad (4\text{-}16)$$

Equation (4-15) defines the current responsivity of the FET detector valid in all regions of operation based on the EKV model whereas technology parameters of Table 4-1 are used for BSIM simulations.

4.2.3 Voltage response

Using above testbench, the voltage response of the FET detector is determined as a function of FET bias voltage with 50µV signal at 600 GHz frequency. Considering a 50Ω input impedance of the FET detector, the impinging radiation power is:

$$P_{rf} = \frac{{V_{DS}}^2}{R} \tag{4-17}$$

This voltage response is divided by P_{rf} and it is plotted in Figure 4-2 for comparison purposes against the theoretical response obtained using ideal square law (equation (2-15)). At higher biasing values, BSIM simulations show a qualitative agreement with square law. However, they drastically deviate at low bias values due to the unrealistic nature of square law of equation (2-6).

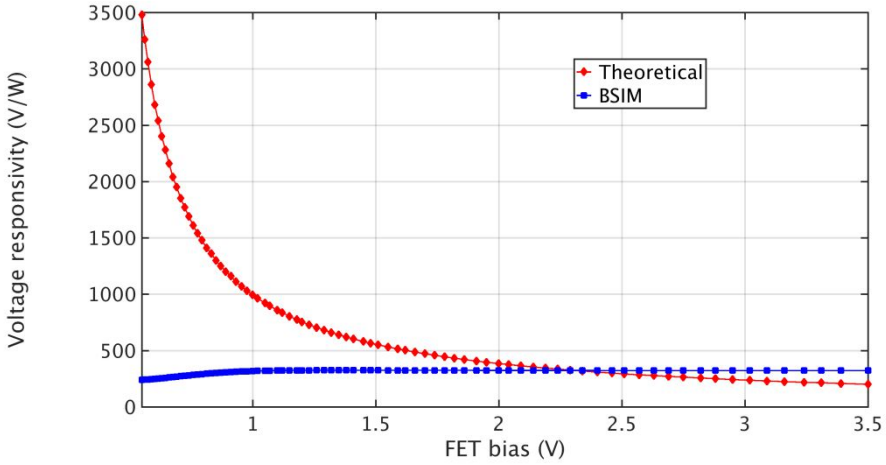

Figure 4-2: Simulated R_V vs. V_{GS} as per ideal square law relationship and BSIM modeling

4.2.4 Current response

Recalling equation (2-13), it is understood that the FET drain current is a function of transistors aspect ratio (W/L) and input signal amplitude V_{RF}. This is proven by carrying out the SPICE simulations, by biasing the FET detector at 1V voltage and stimulating it with a 600 GHz for varying deice width as shown in Figure 4-3.

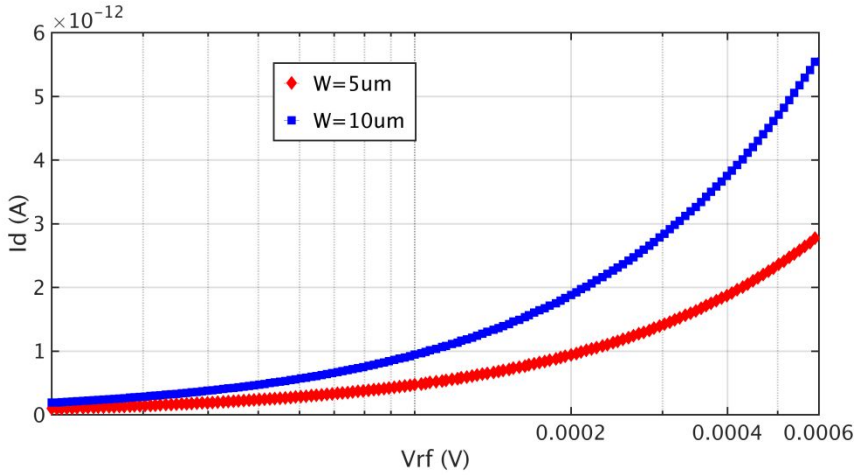

Figure 4-3: Id vs. Vrf when FET is simulated with 600 GHz frequency signal at 1V bias voltage.

Furthermore, the theoretical current responsivity as a function of FET bias voltage can be obtained by simply multiplying voltage responsivity and FET drain-to-source conductance (g_{DS}) as shown by the small signal model of the FET device in Figure 4-4.

$$R_I = R_V * g_{DS} \tag{4-18}$$

where

$$g_{DS} = \mu_n C_{OX} \left(\frac{W}{L}\right) V_{OV} \tag{4-19}$$

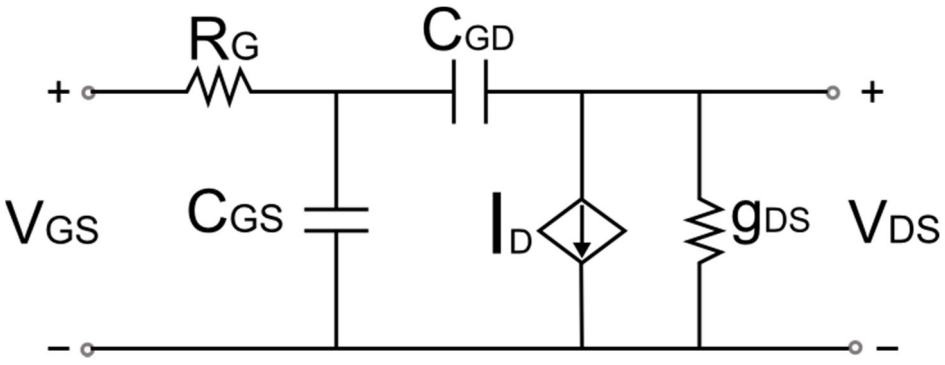

Figure 4-4: FET small signal model

Current responsivity based on BSIM simulation, theoretical modeling of equation (4-18) and EKV modeling of equation (4-15) as a function of bias voltage is plotted in Figure 4-5 for varying device widths which shows that responsivity increases as the width of the device increases.

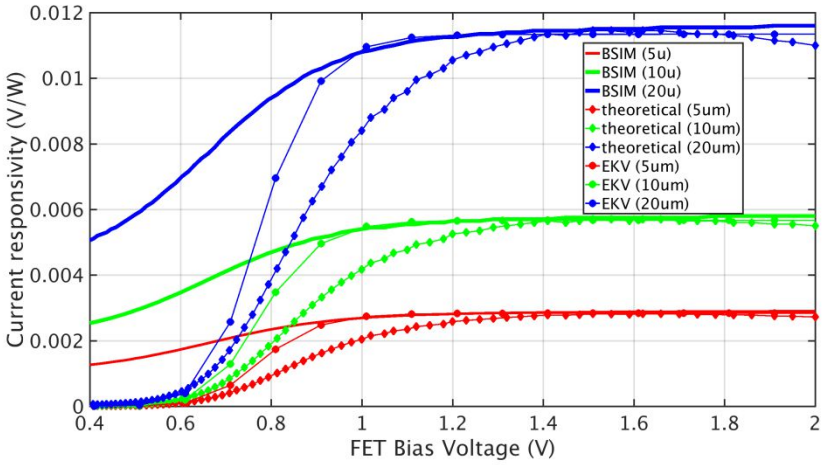

Figure 4-5: Simulated R_I vs. V_{GS} for varying device widths

4.2.5 Simulated Noise Equivalent Power

The thermal noise of the FET device is obtained by determining the simulated R_{DS} as a function of bias voltage. Figure 4-6 shows the NEP plots vs FET bias for varying device dimensions. The graph shows BSIM NEP obtained by dividing simulated noise and simulated current responsivity and theoretical NEP is obtained by using simulated R_{DS} and dividing it by theoretical current responsivity of Figure 4-5. Looking at the R_V and NEP graphs, it is worth noticing that the FET bias voltage points at which the detector achieves the minimum NEP and maximum R_V are different. This consequently means that there exists a trade-of between these two performance parameters.

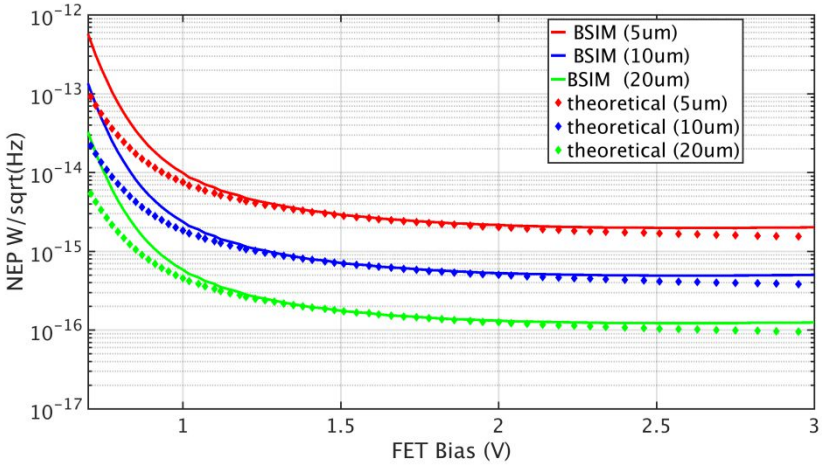

Figure 4-6: Simulated NEP (W/√Hz) vs. V_{GS}

4.3 SOURCE DRIVEN AND GATE DRIVEN CONFIGURATIONS

In literature some of the works demonstrate FET detectors in different configurations where the THz radiations are fed to FET transistors at different terminals. The underlying objective of this section is to investigate the effect of putting FET transistor in different configurations.

For this purpose, two variants of the FET THz detectors based on the radiation coupling and biasing have been designed and implemented in a standard 0.18µm CMOS technology. The main objective was to do the comparative analysis of the FET detectors by implementing and fabricating them on the same silicon die under similar boundary conditions. Considering SPICE simulations, it is expected that the performance parameters of the FET detectors change drastically by changing the way the THz radiation is coupled to the FET detector through antenna, as well as by changing device parameters.

A total of 4 test structures with aspect ratios of (2µm/0.18µm) and (5µm/0.18µm) were fabricated and tested for both the Source Driven (SD) and Gate Driven (DG) configurations. Each structure is driven by an on-chip antenna designed to resonate at 300 GHz frequency. In GD configuration, the THz signal is coupled to the FET detector by connecting the antenna feed between the source and the gate terminals of the device [92].

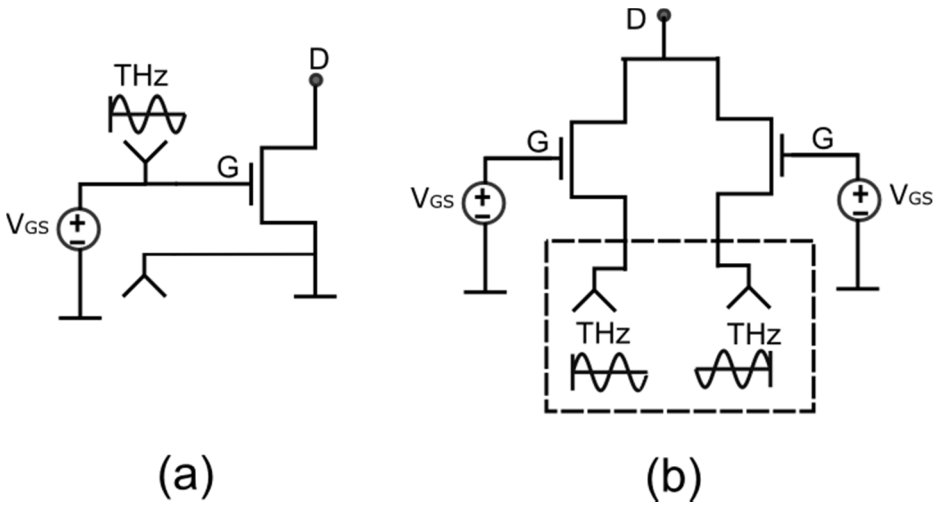

Figure 4-7: FET based (a) gate driven and (b) source driven configurations

In SD configuration, THz radiation is coupled to the detector through source terminal while the gate terminal is DC biased as shown in Figure 4-7. A differential bow-tie antenna is used to feed the source terminals with the THz signal. In both these configurations, the signal response is measured at the output drain terminal. The input impedance of the SD FET has a reduced contribution of the parasitic capacitances of the gate terminal because this terminal behaves as an AC ground. Consequently, in theory, the SD FET should be more broadband as compared to the GD.

Moreover, since the FET is operated in triode region and the channel can be modeled as a voltage controlled resistor R_{DS}, which is a function of aspect ratio (W/L), the size of the transistor also plays a role in determining the responsivity. Based on equation (4-7), the devices with smaller dimensions produce high voltage responsivity as it increases the input resistance which is inversely proportional to the aspect ratio (W/L) of the FET detector. However on the other hand, the downside of this approach is that the antenna must also be designed with high impedance to match it with the detector input resistance for maximum power transfer.

4.4 MEASUREMENT SETUP

To characterize the FET THz detector, the same measurement methodology proposed and discussed in Chapter 03 is used and which is shown in Figure 4-8 for quick reference. It involves the use of a Continuous Wave CW tunable THz source and an Amplitude Modulation (AM) generator. The structures are illuminated by a THz source at a signal frequency of 300 GHz and a pyroelectric detector is used as a reference device to measure the input power density of the detectors. A lock-in amplifier is used for the measurement of the rectified DC signal. The effective pixel area that is illuminated by the impinging power is calculated by measuring the antenna directivity in E and H planes using a mechanical positioning system and their normalized radiation patterns.

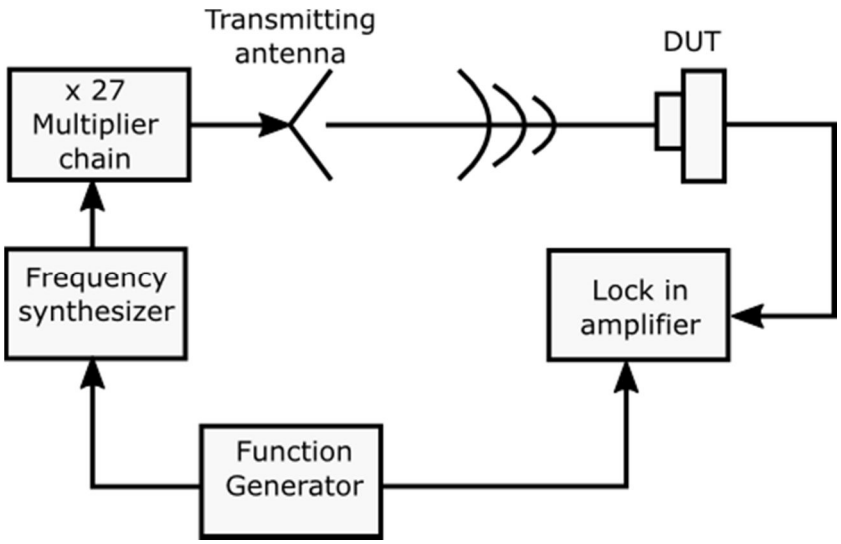

Figure 4-8: Setup for THz measurements

4.4.1 Measurement Results

4.4.1.1 Voltage responsivity

Voltage responsivity is plotted as a function of the FET gate bias voltage at a signal frequency of 300 GHz in Figure 4-9. Moreover, the responsivity as a function of the

THz frequency, at a fixed gate bias voltage of 600mV and 40 Hz source chopping frequency is shown in Figure 4-10.

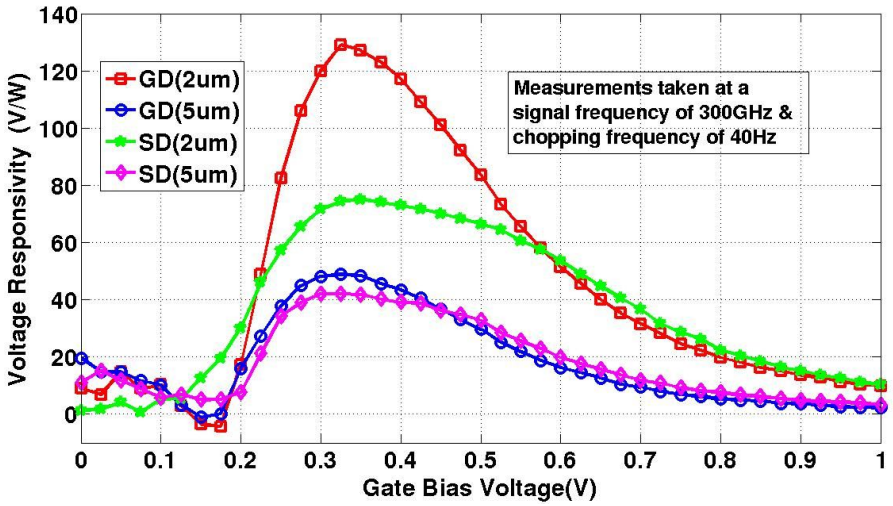

Figure 4-9: Voltage responsivity graphs of GD and SD structures with different dimensions vs. Gate bias

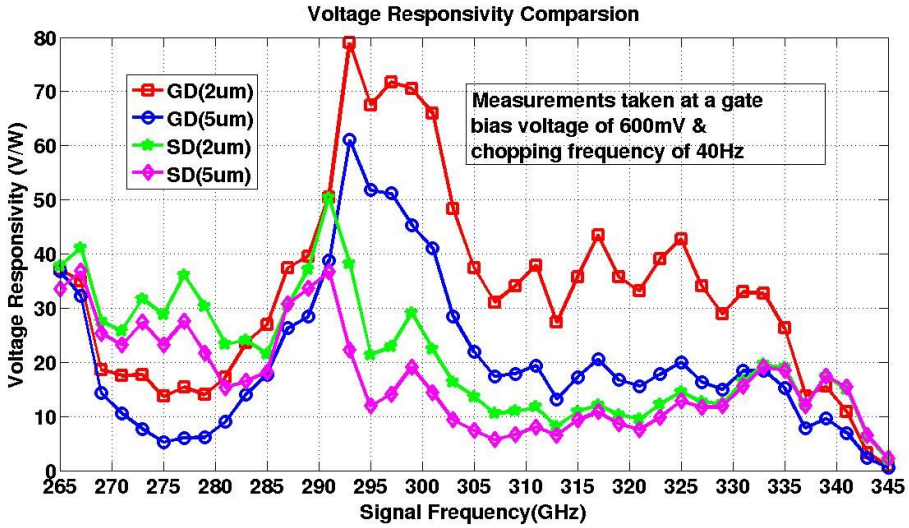

Figure 4-10: Voltage responsivity graphs of GD and SD structures with different dimensions vs. Signal frequency

In Figure 4-11 frequency analysis is further elaborated by normalizing the responsivity graph of Figure 4-10 by dividing the values with the maximum responsivity.

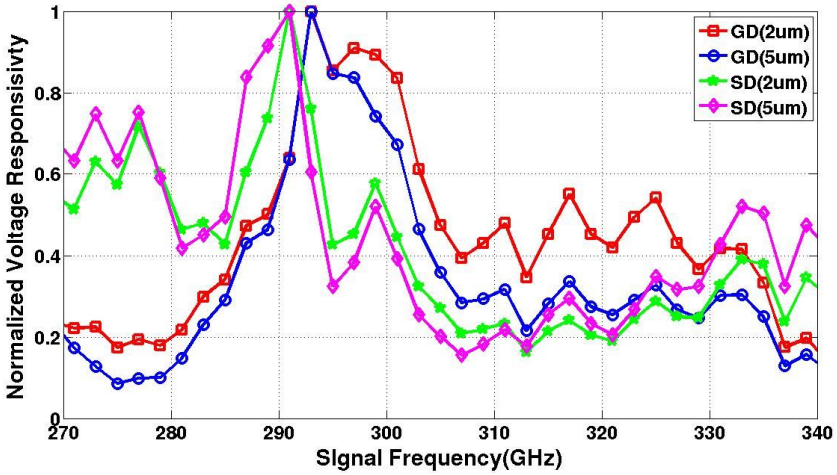

Figure 4-11: Normalized responsivity graphs of GD and SD structures with different dimensions vs. Signal frequency

4.4.1.2 Noise Equivalent Power

The resistance of the FET detector is calculated by using a DC millimeter. From R_V data and measured R_{DS} values, the NEP value of all the FET structures are calculated and are plotted as a function of FET gate bias at the 300 GHz signal frequency as shown in Figure 4-12. The minimum NEP value of 147 pW/sqrt (Hz) is achieved by the SD structure with 2µm width.

Table 4-2 presents the summary of the results in terms of the measured performance parameters of all the test structures

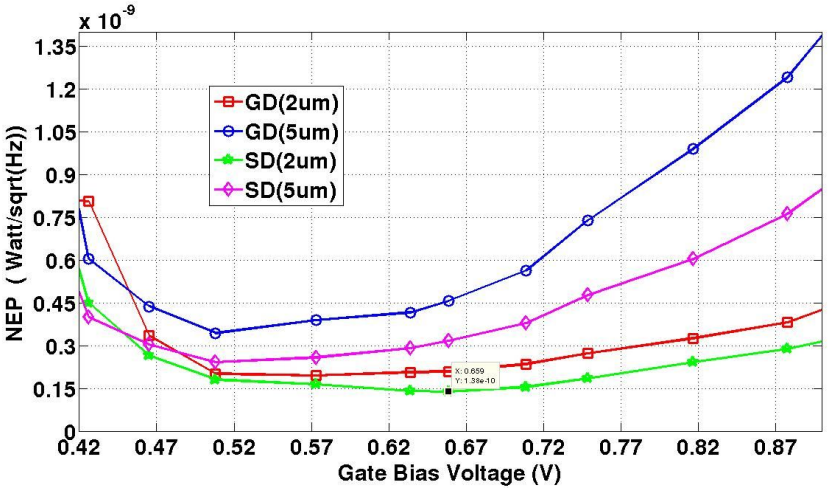

Figure 4-12: NEP of test structures as a function of FET gate bias voltage

Table 4-2: Measured performance parameters of the FET structures in different configurations and dimensions

FET structure configuration	GD (2µm/0.18µm)	GD (5µm/0.18µm)	SD (2µm/0.18µm)	SD (5µm/0.18µm)
Maximum Responsivity	128	48	75	40
Minimum NEP	200	363	147	228

4.5 DISCUSSION OF THE RESULTS

The observations are listed below:

4.5.1 Biasing response

Referring to Figure 4-7, the SD test structures see only half the incident voltage across the two transistors but the detected voltage is not summed up at the drain terminal, consequently their responsivity is lower than the GD structures as shown in the graphs of Figure 4-9. The FET structures with smaller dimensions are more responsive at a given bias voltage, which is proven by the high responsivity values achieved by these test structures as shown in Figure 4-9 and Figure 4-10.

4.5.2 Frequency response

In the region of interest around 300 GHz of the frequency sweep graph of

Figure 4-11, the GD structures show high responsivity. However, moving away from the resonant frequency of antenna the SD structures show a smaller drop in the responsivity values as compared to the GD counterparts. This is also evident from the relatively flat nature of the responsivity values of the SD structures as the signal frequency drops below 290 GHz while the GD structures show a sharp drop in their responsivity values. Looking at the normalized frequency response, the SD structures have a large bandwidth which makes them suitable to be used in broadband applications.

4.5.3 NEP

Smaller detectors provide better results in terms of both responsivity and NEP. However, at the same time it will be difficult to fully match the detector's input impedance with the antenna impedance given its impractically high value. Thus, achieving the maximum responsivity and minimum NEP by keeping the device dimensions small might not be the sole criteria for obtaining an optimal solution while designing the FET based THz detectors.

4.6 CHAPTER SUMMARY

This chapter discusses design, simulation and optimization of FET-based direct THz detector sand its variants based on the coupling of THz radiations and design dimensions. Based on the discussion inferred from simulated and experimental results, it is interesting to note that high performance parameters values present a trade-off in terms of various design parameters of the FET detector. To summarize, for applications requiring high sensitivity and resolution the GD structures can be employed in the imaging arrays while the SD structures are more suitable for applications which require high bandwidth.

CHAPTER 5: SINGLE PIXEL DESIGN

Despite the simplicity and ease of fabrication of the FET THz detectors, their weak output signal in response to the impinging THz radiation still needs to be processed. In this regard, the challenges are manifold while designing the readout interface:

1. **High gain:** the readout interface must be able to significantly amplify the detected signal in order to be processed by the external Analog to Digital Converters (ADC) having Least Significant Bit (LSB) in the order of several millivolts and to ensure the integrity of the signal.

2. **Low noise:** the noise generated by the readout channel must be lower than the noise produced by the detector, which in the case of an FET device depends on the region of operation and device dimensions, as well as the system bandwidth. If the FET detector is biased to attain minimum NEP, the total integrated input-referred noise of the channel must be lower than the intrinsic detector noise, which therefore defines the Minimum Detectable Signal (MDS).

3. **DC Offset level:** CMOS amplifier offsets in the readout circuitry may reach levels of several tens of millivolts. In the absence of any cancellation mechanism, this offset can easily saturate the readout chain due to the high-gain requirements.

4. **Robustness:** the implementation of a repeatable readout architecture which should also be compatible with commercially available THz sources, both in terms of the emitted power and modulation frequency values.

5. **Power consumption:** The power consumed by the readout interface must be minimized if the pixel is to be used in an array configuration.

6. **Small size:** Small area is also a key requirement while designing readout interface for THz imaging array applications. The channel area should be

minimized to make it compatible with the physical size of the on-chip antenna and it has to fit the required pixel dimensions.

5.1 STATE-OF-THE-ART REVIEW

Several architectures have been reported in literature in an attempt to achieve the objectives mentioned in last paragraph.

5.1.1 Schuster, 2011, 3x4 imager

A 3x4 imager fabricated in 0.13µm CMOS technology was reported in [67]. By virtue of in-pixel 31 dB amplification provided by the circuit of

Figure 5-1 an impressive voltage responsivity of 90 kV/W at 300 GHz frequency was obtained, but the NEP value for a 2 MHz system bandwidth was not reported.

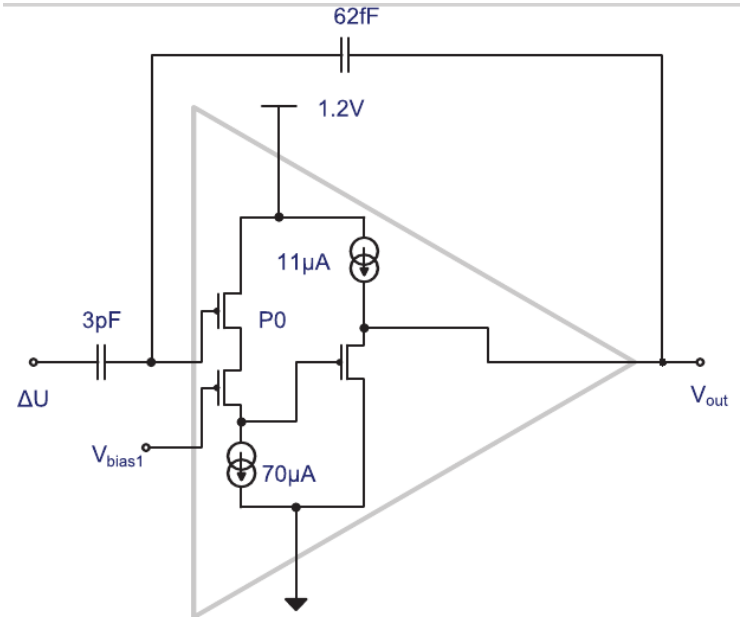

Figure 5-1: In pixel amplifier schematic used in [67]

5.1.2 Ojefors, 2009, 3x5 Imager

In [65], a 3x5 Focal Plane Array (FPA) based on the FET THz detectors was presented. Thanks to the readout channel comprising of the active devices to provide high amplification, the FPA achieved a voltage responsivity of 80 kV/W. However, the readout interface added significant noise. This architecture required anyway the use of a separate lock-in amplifier to detect the signal.

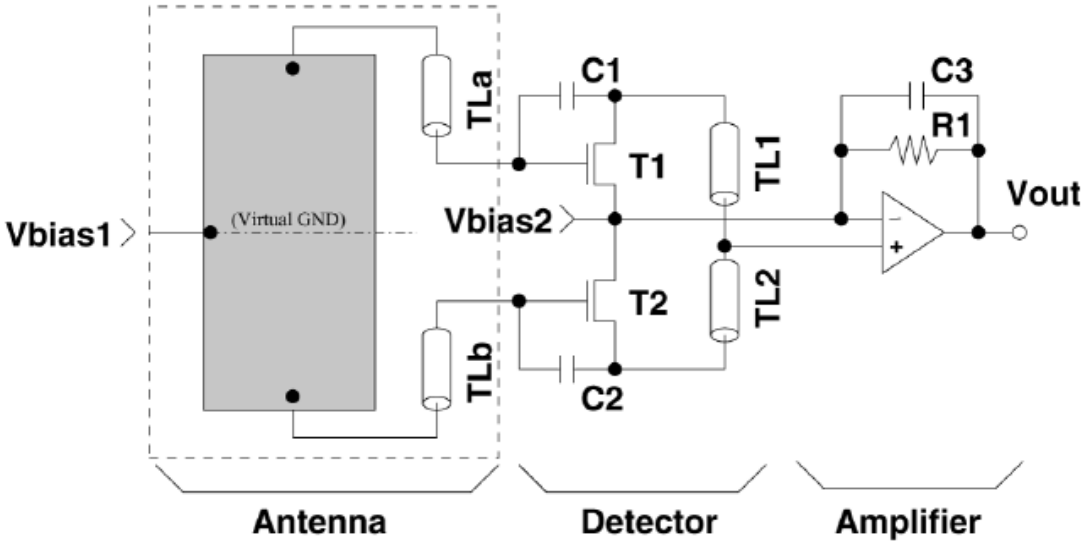

Figure 5-2: Pixel schematic comprising an on-chip differential antenna, FET detectors and voltage amplifier used in [65]

5.1.3 Hadi, 2012, A 1 k pixel camera

A FET based 1k pixel THz camera for video imaging applications was presented in [93] featuring readout channel composed by an amplifier and an 8pF integration capacitor (Figure 5-3). Despite of using this large capacitor inside each pixel, the camera system was not optimized for the typically low frame rates (100 Hz) of the video imaging applications. The system bandwidth was still in the range of several kHz-MHz, which degraded the NEP of the detector with respect to a lower

bandwidth. The lower system bandwidth minimizes the integrated noise, improving the NEP.

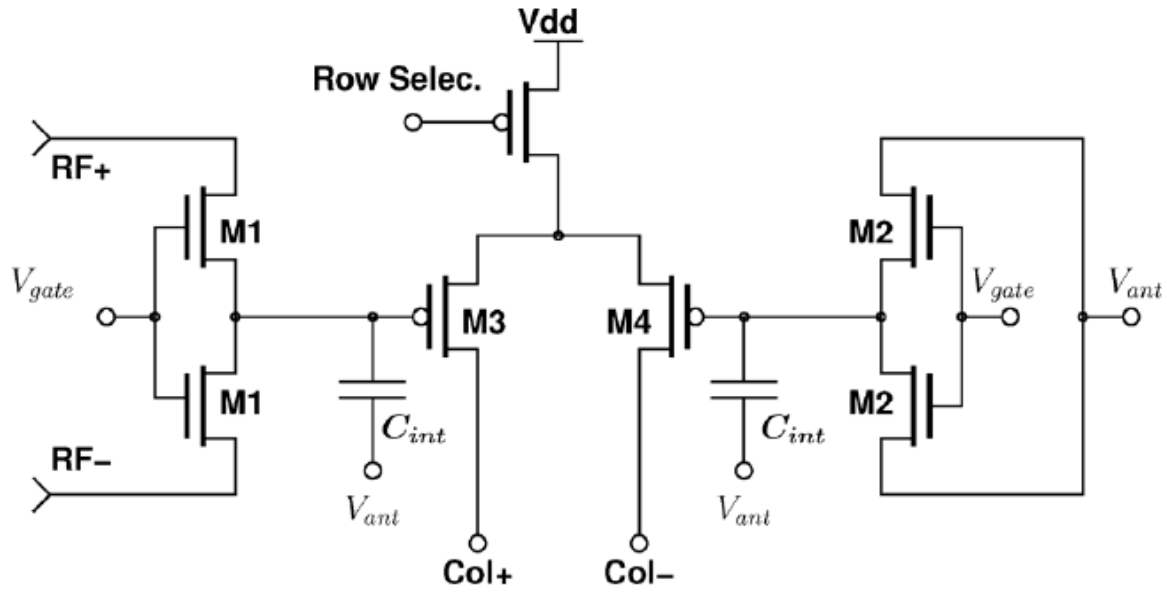

Figure 5-3: Pixel schematic of the differential cascode configuration used in [93]

5.1.4 Boukhayma, 2014, 31 x 31 FPA

A more recent work in [94] [95] presented a CMOS THz imager based on an in-pixel high Quality Factor (Q=100) Bandpass Filter (BPF) as shown in Figure 5-4. This approach drastically reduced the readout channel noise while simultaneously providing amplification, thus enabling the measurement of the output signal without using the lock-in amplifier. However in order to properly operate the BPF, the THz source must be modulated to several hundreds of kHz which is not always an available feature with the commercial sources.

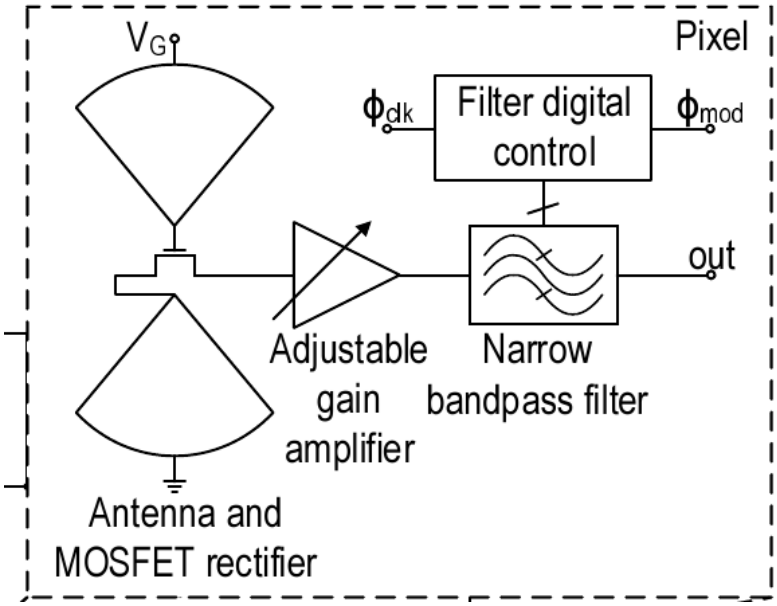

Figure 5-4: System level design of the pixel used in [94] [95]

5.1.5 Kim, 2016, 8 x 8 Imager

This same limitation can also be observed in [96] which require the THz source to be modulated at 1MHz in order to operate an 8x8 diode-connected NMOS transistor array at 0.82 THz frequency.

5.2 PIXEL SPECIFICATIONS

In any efficient and well-designed sensor system, the noise produced by the readout channel should be lower than the noise generated by the detector, which means that the overall system's performance should be limited only by the intrinsic limit of the detector's noise. In a cold biased configuration, the thermal noise defines the intrinsic noise limit of the FET detector:

$$V_N^2 = 4k_B T R_{DS} \Delta f \tag{5-1}$$

where k_B is the Boltzmann constant, T is the room temperature in Kelvin and Δf is the noise bandwidth. For a low noise operation, the NEP of the system must be minimized. This can be achieved in the following two ways:

- By biasing the FET detector at the gate voltage that ensures the minimum NEP.
- By reducing the system bandwidth Δf: In fact as the detected signal is at the DC level, the overall noise can be minimized by reducing the bandwidth of the readout interface.

In this work, the system bandwidth is set to 1 kHz which is based on the trade-off between minimizing the readout noise and fully recovering the FET detected signal at the systems output. Moreover, minimum dimensions (W/L) of the FET detector were used, as permitted by the technology. The length of the FET channel must be larger than the plasma wave build-up length, but as small as possible to reduce resistance and to minimize noise. The width should be wide to reduce noise but small to improve antenna matching, which actually is a dominant factor. As reported in [97], the NEP of the FET detector having an input resistance R_{IN} and biased at V_{GS} is given by:

$$NEP = \sqrt{\frac{4^3 k_B T (V_{GS} - V_t)}{\mu_N C_{OX} \left(\frac{W}{L}\right) (\mathrm{R_{IN}})^2}} \qquad (5\text{-}2)$$

Where V_t is the transistor threshold voltage.

The FET detector was fabricated in a standard 0.15µm CMOS technology and it exhibits the lowest NEP at the gate bias voltage of 400mV, which was found out to be in close agreement with the theoretical value obtained using equation (5-2). Using equation (5-1), the R_{DS} value of 600 kΩ at this bias voltage generates a thermal noise power of 99.6 nV^2/Hz, which corresponds to the noise voltage of only $4\mu V_{RMS}$ for 1 kHz bandwidth. This value sets the maximum limit for the input referred noise of the readout channel that can be tolerated to preserve the detector NEP and is as such called as the **M**inimum **D**etectable **S**ignal (MDS) of the detector.

5.2.1 System level design

For the MDS of $4\mu V_{RMS}$, output voltage amplitude in excess of several mV is desired to increase the SNR and also to meet the minimum signal specifications set by the LSB of an external ADC. This requires a system voltage gain in excess of 60 dB. Moreover, the system bandwidth must be kept within 1 kHz to meet the integrated input referred noise requirements. Table 5-1 outlines the system level specifications.

Table 5-1: System level specifications of the readout interface

Minimum detectable signal	MDS (rms)	4µV
Desired output	V_{OUT} (pp)	40 mV
Required signal amplification	A_{VT} (dB)	70
Maximum tolerable Input referred noise	$V_{N,IN}$ (rms)	Less than 4µV
Maximum noise bandwidth	BW (kHz)	1.0
Power consumption		As low as possible
Supply voltage	V_{DD} (V)	1.8 V

The low-noise and high-gain requirements can be met with only a multistage architecture design approach: Indeed, the single stage design presents a tradeoff between achieving either high gain or low input noise. Therefore, a chopper based Switched Capacitor (SC) multistage readout is employed to meet the specifications.

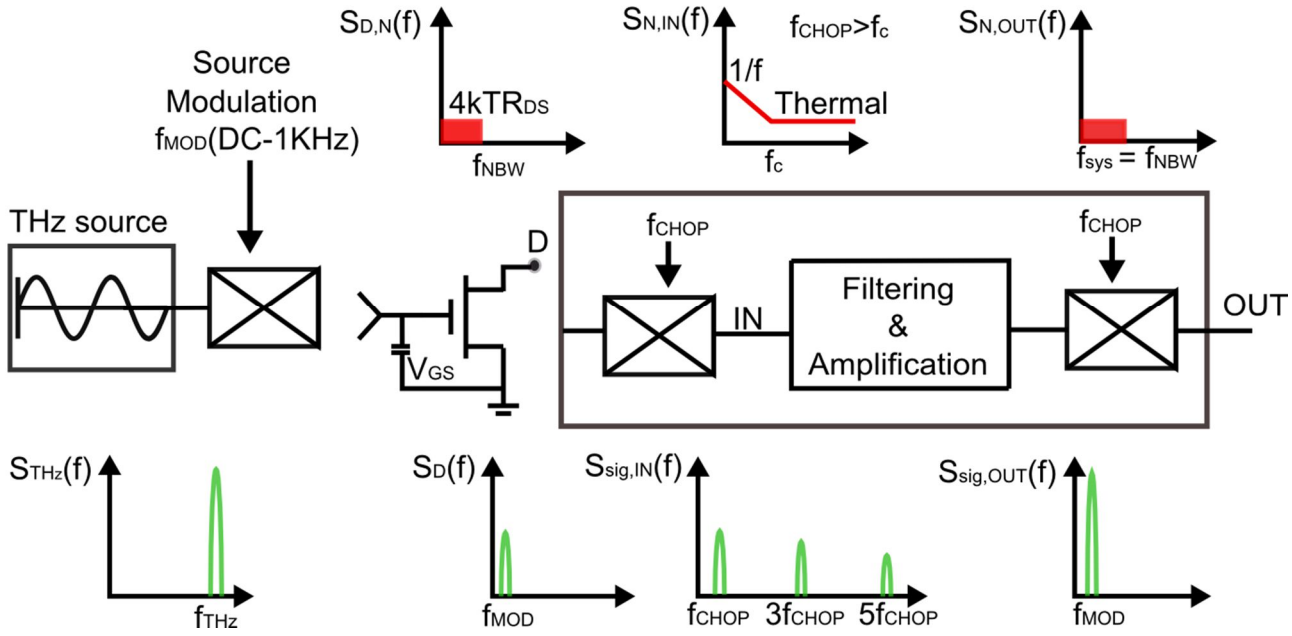

Figure 5-5: System level design of the pixel showing the signal and noise spectra alongside different stages

Figure 5-5 shows the pictorial overview of the how the signal and noise are shaped in the frequency domain as they progress through the readout chain. The THz radiation, electrically modulated to f_{MOD}, is received by the on-chip antenna and converted to the baseband signal by the FET detector. Then, the signal passes through the readout channel where it is first modulated to the chopping frequency f_{CHOP}=50 kHz, amplified and filtered using a High Pass Filter (HPF) and then demodulated back to the baseband. Two cascaded LPFs are finally used to provide more amplification and also to reduce the system bandwidth to 1 kHz, consequently minimizing the integrated thermal noise. This scheme ensures that the offset and flicker noise of the MOS devices are moved to the high frequency, out of the band of interest while only the rectified input signal is amplified. System level modelling and verification of the readout interface based on these theoretical specifications was performed in MATLAB and the details with simulation plots are given in Appendix C.

Figure 5-6 shows the circuit diagram of the readout interface while the chopper symbol is depicted in Figure 5-7.

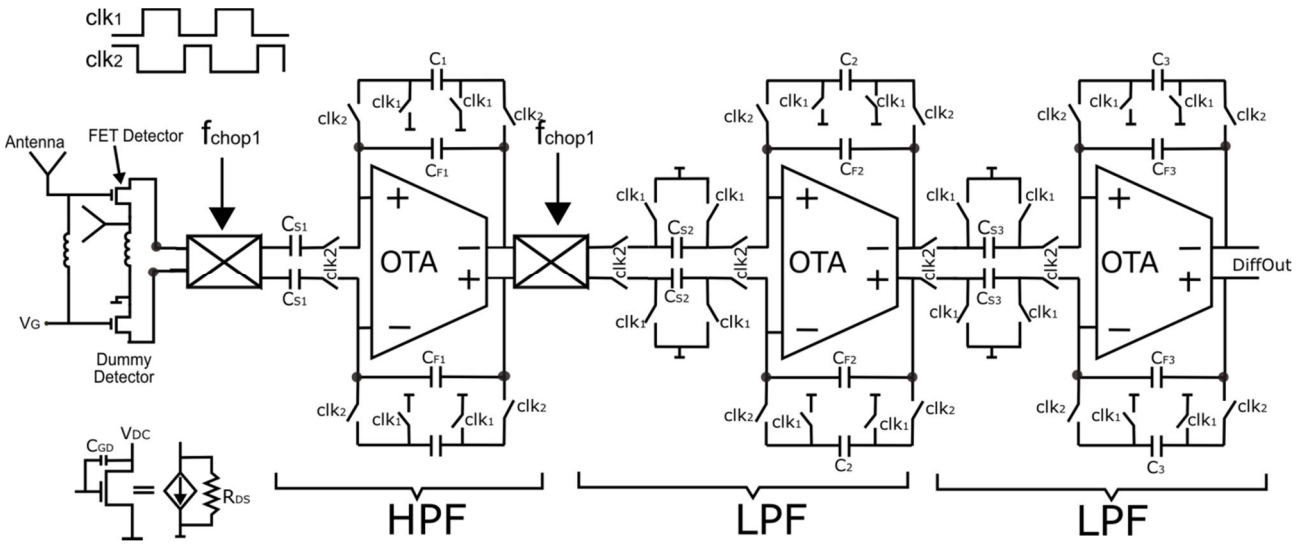

Figure 5-6: Circuit schematic of the pixel showing antenna-coupled FET detectors and SC based multistage readout interface

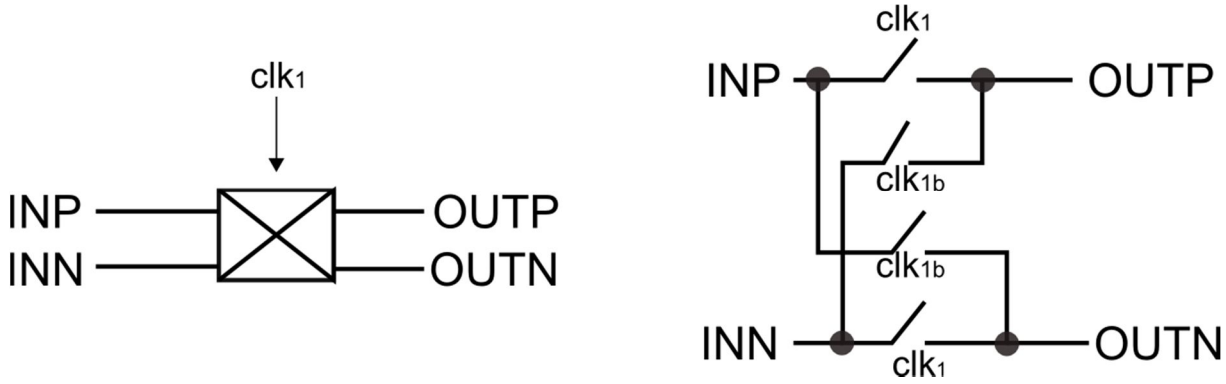

Figure 5-7: Chopper symbol and circuit schematic

5.3 CIRCUIT LEVEL DESIGN

5.3.1 Switched capacitor high pass filter

Figure 5-8 shows the Continuous Time (CT) HPF. C_S and C_F are the sampling and feedback capacitors respectively while R_F represents the feedback resistance [98]. The Signal Transfer Function (STF) of this filter is:

$$H_{HPF}(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{sC_1}{sC_3 + G_F} = \frac{sC_1R_F}{sC_3R_F + 1} \tag{5-3}$$

The SC-HPF is designed for a cut off frequency of 30 kHz and a high frequency gain of 20 (26 dB). Taking into consideration the accumulated charge on the capacitors during both the clock phases and applying the charge conservation principle, the transfer function of the SC-HPF is:

$$\frac{V_{OUT}(z)}{V_{\mathrm{IN}}(z)} = \frac{-\left(\frac{C_1}{C_2+C_3}\right)[1 - z^{-1}]}{\left[1 - z^{-1}\left(\frac{C_3}{C_2+C_3}\right)\right]} \tag{5-4}$$

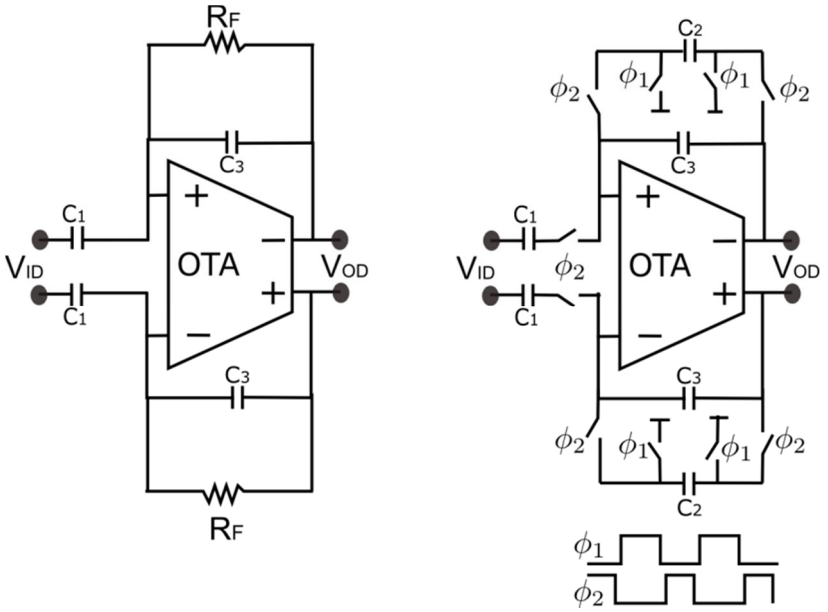

Figure 5-8: Circuit schematic of the switched capacitor high passes filter and non-overlapping clock signals

Using this approach, also the 2nd and 3rd stage of the readout interface (a cascade of LPF) were designed to achieve the required signal gain and to limit the system's bandwidth to 1 kHz. A description of the design process is explained in Appendix B.

5.3.2 Noise Analysis

The noise arising from the 2nd and 3rd stages can be neglected as it is divided by the relatively high voltage gain of the 1st stage. Thanks to the chopper action, the flicker noise and offset are strongly attenuated, which leaves the switches kTC and OTA noise as the two dominant noise sources [99] [100]. Figure 5-9 depicts the noise sources and the single-ended half circuit configurations for cock phases Φ_1 and Φ_2. The output noise voltage in configuration (a) is:

$$\overline{V_{N,OUT}{}^2} = \frac{8k_B T}{3(C_L + C_3)} \tag{5-5}$$

In configuration (b), one kTC noise is added on C_1 which is multiplied by the system's closed loop gain when referred to the output:

$$\overline{V_{N,C_1}{}^2} = \frac{k_B T}{C_1}\left(\frac{C_1}{C_3 + C_L}\right)^2 \tag{5-6}$$

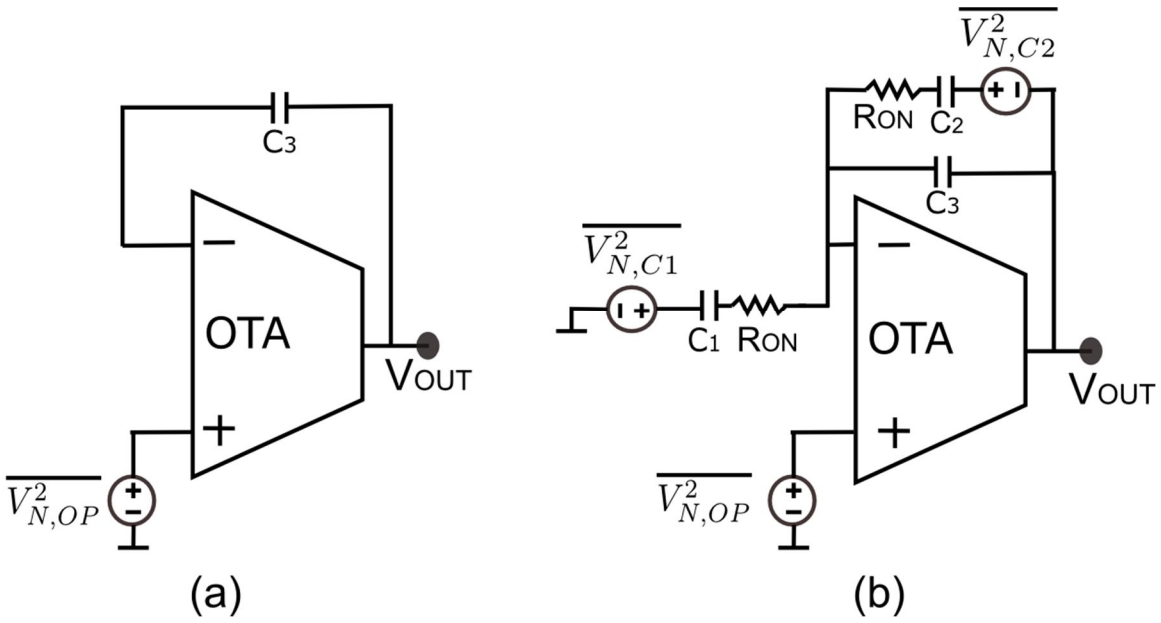

Figure 5-9: Configurations of the first stage SC-HPF for noise analysis

Similarly, the noise due to C_2 and amplifier are:

$$\overline{V_{N,C_2}{}^2} = \frac{k_B T}{C_2 + C_3 + C_L} \tag{5-7}$$

$$\overline{V_{N,OP}{}^2} = \frac{8k_B T}{3(C_L + C_2 + C_3)} \tag{5-8}$$

Thus the total output noise voltage for the differential configuration is given by:

$$\overline{V_{N,OUT}{}^2} = 2 * \left\{ \frac{8k_B T}{3(C_L + C_3)} + \frac{k_B T}{C_1} \left(\frac{C_1}{C_3 + C_L} \right)^2 + \frac{k_B T}{C_2 + C_3 + C_L} + \frac{8k_B T}{3(C_2 + C_3 + C_L)} \right\} \tag{5-9}$$

Owing to the chopper action, device flicker noise is transposed to the chopping frequency so the kTC remains the dominant noise source. This consequently puts a constraint on sampling capacitor C_S value. Setting a small value of C_S ensures small area but would result in large kTC noise as evident from equation. In order to avoid it, the sampling capacitor C_S is set to a relatively large value of 5 pF to keep the input referred noise voltage of the readout circuit within the specifications. The HPF is designed to achieve a closed loop gain of 26dB in the first stage, while the remaining 48 dB gain is contributed by the 2nd and 3rd stages to make up for a theoretical system gain target of 72 dB. Based on this noise analysis and other constraints, the system and circuit level design specifications of each stage is listed down in Table 5-2.

Table 5-2: System & circuit level design specifications of individual stages

Stage	*1st (SC-HPF)*	*2nd (SC-LPF)*	*3rd (SC-LPF)*
Capacitor values	C_1 = 5pF ; C_3 = 0.25pF	C_1= 4pF ; C_3=0.25 pF	C_1= 2 pF; C_3=0.15 pF
Sampling clock	200		
DC gain	26 dB	24 dB	22 dB
Cut off frequency	30 kHz	70 kHz	1.0 kHz
Chopper frequency	50 kHz		

5.3.3 Operational Transconductance Amplifier

A fully differential telescopic cascode OTA is designed to be used in the filters [99] [101]. This choice was motivated by the requirements for high voltage gain, small noise and low power. A folded cascode OTA would have achieved a higher signal swing compared to telescopic cascode, but it consumes more power and generates more noise. In an open loop configuration, the voltage gain of a telescopic cascode OTA is:

$$Av = g_m R_{OUT} = g_m(R_{UP}||R_{DOWN}) \tag{5-10}$$

where g_m is the transconductance of the amplifying device, R_{OUT} is its output resistance while R_{UP} and R_{DOWN} are the up and down resistances as seen from the output node. *Assuming* $g_{m1}=g_{m3}=g_m$ *and* $r_{DS,3}=r_{DS,1}=r_{DS}$

$$Av \approx (gmr_{DS})^2 \tag{5-11}$$

$$Av \approx \left(gm \frac{V_A^{'} L}{I_D} \right)^2 \tag{5-12}$$

where $V_A^{'}$ is the early voltage per unit channel length and 'L' is the length of the channel. Furthermore, the Gain Bandwidth product (GBW) of the OTA is obtained by multiplying DC voltage gain A_V and BW:

$$GBW = \frac{gm_1}{2\pi C_L} \tag{5-13}$$

Equation (5-13) defines the required value of input pair transconductance to obtain a specified GBW while driving the load capacitance C_L. The trainset output of the OTA must settle with an accuracy of less than 1% which defined the settling error (ε). In a negative feedback system, the static error is given by:

$$Ao = \frac{1}{\epsilon_s \beta} \tag{5-14}$$

where A_0 is the open loop gain and β is the feedback factor. The closed loop voltage gain 'G' is defined by the capacitor ratios and is given by:

$$\beta = \frac{1}{G} = \frac{C_F}{C_S} = \frac{0.25pF}{5pF} = \frac{1}{20} \tag{5-15}$$

For a static error of 80%, the required open-loop DC gain of the OTA is at least 68 dB as per equation (5-14). The dynamic error characterizes the timing properties of the OTA output such as slewing, settling time, overshoot etc) and it is set to 20% (0.002) of the total error. If τ is the settling time constant, then ϵ_d is:

$$\epsilon_d = e^{-t/\tau} \tag{5-16}$$

The time period related to the system clock frequency of 200 kHz is given by:

$$T_{clk} = \frac{1}{f_{clk}} = \frac{1}{200\ kHz} = 5\mu sec$$

Considering that the OTA must settle within half the sampling time (2.5µsec), the required settling time constant τ is calculated to be 0.4µsec. Then the GBW is:

$$GBW = \frac{1}{\tau\beta} = 49\ M\frac{rad}{sec} = 7.9\ MHz$$

Based on this, the design specifications of the OTA are given in Table 5-3.

Table 5-3: OTA design specifications

Power Supply (V)	V_{DD}	1.8
Gain Bandwidth (MHz)	GBW	8
Open loop DC gain (dB)	A_0	67
Settling error	ε	<1%
Load Capacitor (pF)	C_L	4pF
Power consumption		As low as possible

The telescopic cascode OTA was designed based on the gm/id approach [102] [103] [104] and the circuit specifications including transistor aspect ratio (W/L), drain currents (I_D) and transconductance (g_m) are listed down in Table 5-4.

Table 5-4: Theoretical and simulation design details of the telescopic cascode OTA

Transistor	I_D sim) (µA)	g_m (sim) (µS)	g_m/I_D (sim)	V_{OV} (sim) (mV)	L (µm)	W (µm)	Multiplying Factor (m)
M1-M2	17	321	19.5	82	2	10	4
M3-M4	17	329	20.1	78	1.2	7.5	4
M5-M6	17	221	13.5	105	1.2	7.5	8
M7-M8	17	140	8.5	170	2	7.5	2
M_{TAIL}	34	182	6	252	1	2	1

5.3.3.1 Common Mode Feedback Configuration (CMFB)

C**o**mmon **M**ode **F**eed**b**ack circuitry (CMFB) is required to settle the output DC voltage level at half the power supply for the differential telescopic cascode to attain the maximum signal swing. A SC CMFB shown in the Figure 5-10 is used for this purpose [99] [101]. The operation is controlled by two non-overlapping clock phases' clk1 and clk2, operating at a clock frequency of 200 kHz and the values of the capacitors C_1 and C_2 are fixed at 200 fF and 50 fF respectively. The Common Mode signal output (V_{CM}) of the OTA is compared to a reference voltage Vbias and the resulting signal (V_{CMFB}) is used to control the bias voltage of the PMOS transistor pair M7-M8.

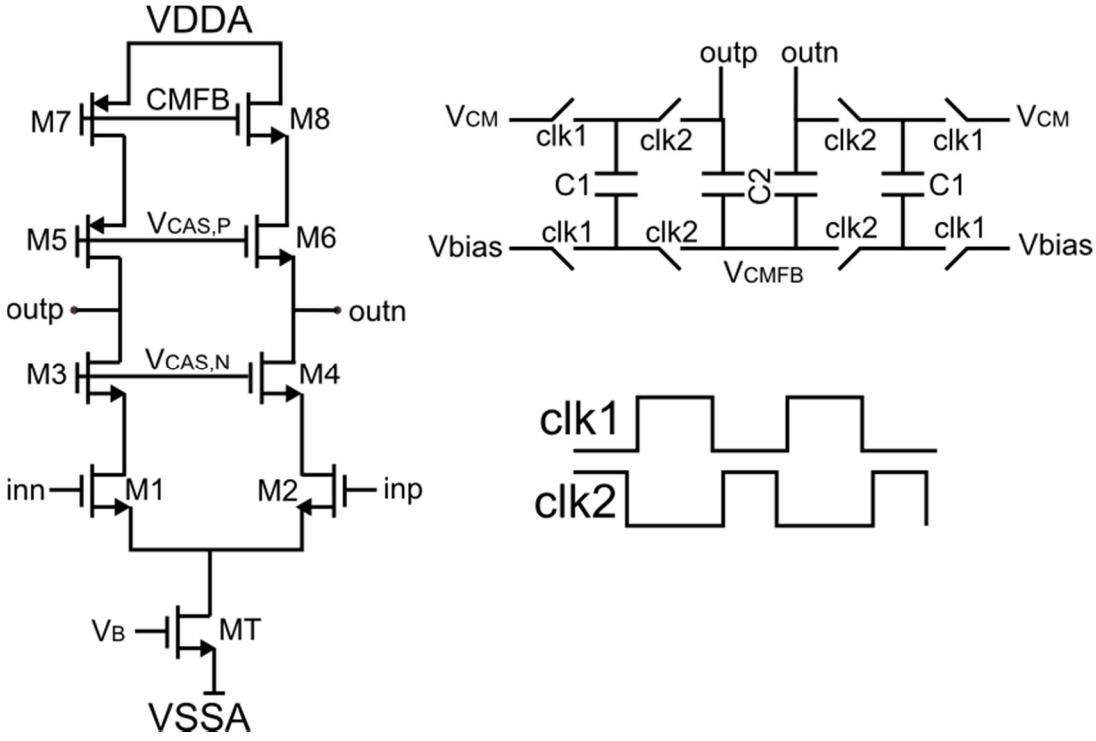

Figure 5-10: Telescopic cascode OTA and SC-CMFB with non-overlapping clocks

5.3.3.2 Simulation Results

Figure 5-11 shows the test bench used to evaluate the frequency response of the OTA in an open loop configuration, as well as the simulated response. The OTA achieves a DC gain of 72 dB with a GBW of 10 MHz which is within the specifications.

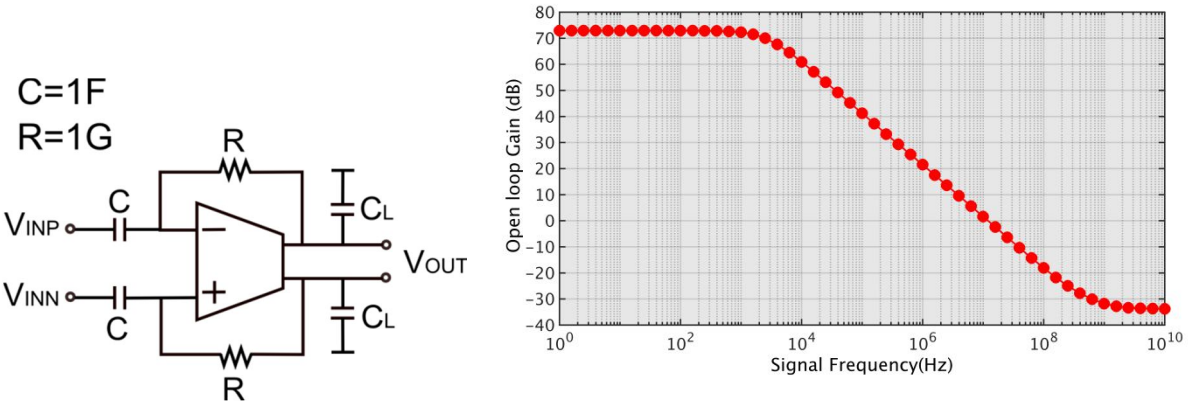

Figure 5-11: Simulated frequency response of OTA in open loop configuration and the testbench.

The noise simulation of Figure 5-12 shows that the OTA flicker noise is minimized, thanks to the fact that the amplifying devices are operated in the weak inversion as is explained in detail in Appendix A.

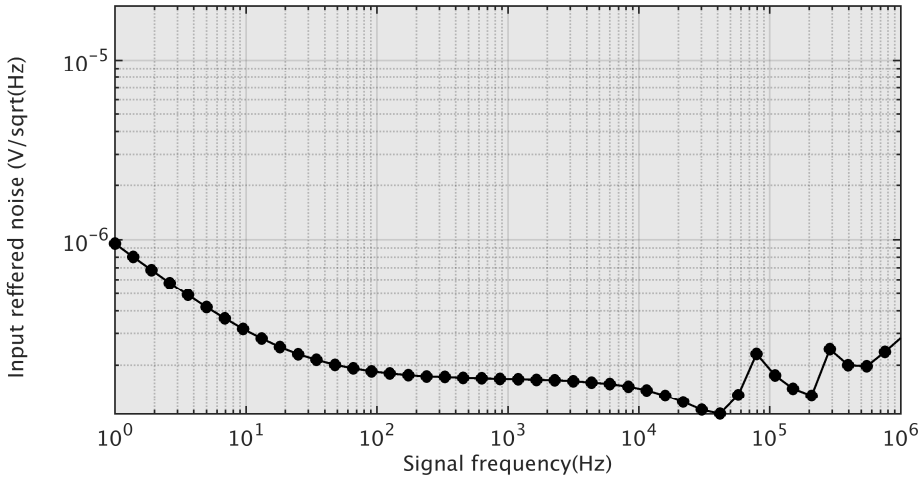

Figure 5-12: Simulated frequency response of OTA in open loop configuration

5.4 CHIP FABRICATION

The designed readout channel has been fabricated in a 0.15µm 6M standard CMOS technology with Metal Insulator Metal (MIM) capacitors. For test purposes, two readout channels have been implemented: one is a standalone channel which can be electrically tested and the other was connected to an on-chip antenna-coupled FET detector for THz characterization [105]. The readout channel occupies an area of 400 µm × 250 µm and with minor modifications it can be adapted to a pixel with a 300 GHz on-chip antenna, making it compatible to be used in imaging arrays. The analog and digital parts operate at 1.8V supply voltage and the total power consumed by the pixel is approximately 200µW.

Figure 5-13 shows its micrograph and the zoomed part depicts the antenna and readout channels.

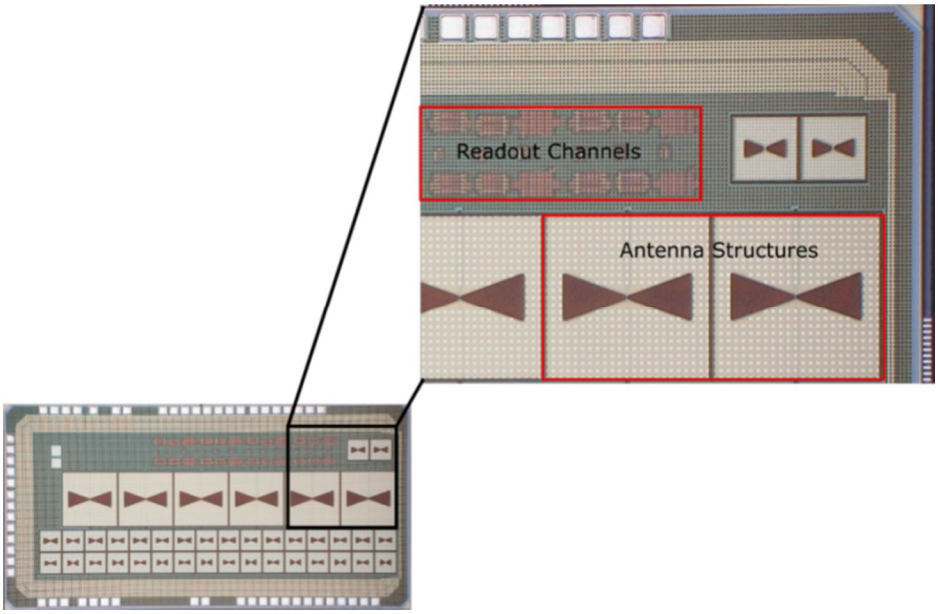

Figure 5-13: Chip micrograph (Inset shows the fabricated antennae and the readout channels)

5.4.1 Electrical Interface

The overall chip architecture and pin configurations and descriptions are described in this section.

5.4.1.1 Core

The core of the chip has three main parts: on-chip antenna, readout interface for external and antenna stimuli.

5.4.1.2 Layout

The chip layout, including the core and padring is shown in the Figure 5-14

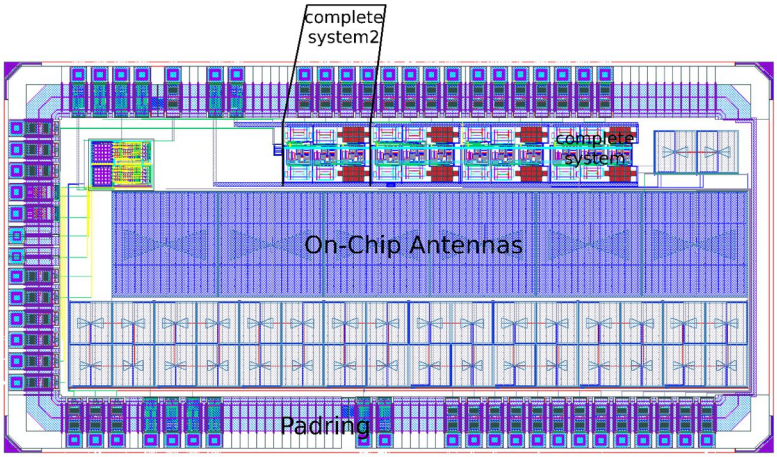

Figure 5-14: Chip layout showing the antenna, readout and the padring

5.4.1.3 Pins description

List and description of the various pins are listed in Table 5-5.

Table 5-5: Pins description

NAME	TYPE	DIR	DESCRIPTION
VDDD	PWR	I	Digital Power Supply
GNDD	PWR	I	Digital Ground
GNDA	PWR	I	Analog Ground
VDDA	PWR	I	Analog Power Supply
Vgate	ANA	I	antenna gate (terminal) voltage
Vsrc	ANA	I	antenna source (terminal) voltage
Vdummy	ANA	I	Dummy antenna gate (terminal) voltage
Out2p	ANA	O	Positive output of pixel connected to the external input
Out2n	ANA	O	Negative output of pixel connected to the external input
CMFBBias	ANA	I	Common mode feedback bias (fixed at 1 V)
CM	ANA	I	Common mode voltage (fixed at 0.9 V)
Out4p	ANA	O	Positive output of pixel connected to the antenna
Out4n	ANA	O	Negative output of pixel connected to the antenna
In1p	ANA	I	Positive terminal of pixel input
In1n	ANA	I	Negative terminal of pixel input
Vbn	ANA	I	OTA Biasing voltage
chop/DIO-11	DIG	I	Chopper clock
clk2/DIO-10	DIG	I	System clock for last stage (LPF) of the channel
clk1/DIO-09	DIG	I	System clock for the first 2 stages of the channel

5.4.2 Test & measurement setup

A test board (daughter board) is designed for testing chip functionalities. The motherboard is powered up by a DC power supply of 8V and the required analog voltage and current reference signals are provided and fine-tuned using trimmers, while their values can be measured using digital multimeter. The digital signals can be generated either by using Digital Waveform Generator of the LabVIEW program or by using pulse generator. Figure 5-15 shows the designed daughterboard to perform electrical characterization.

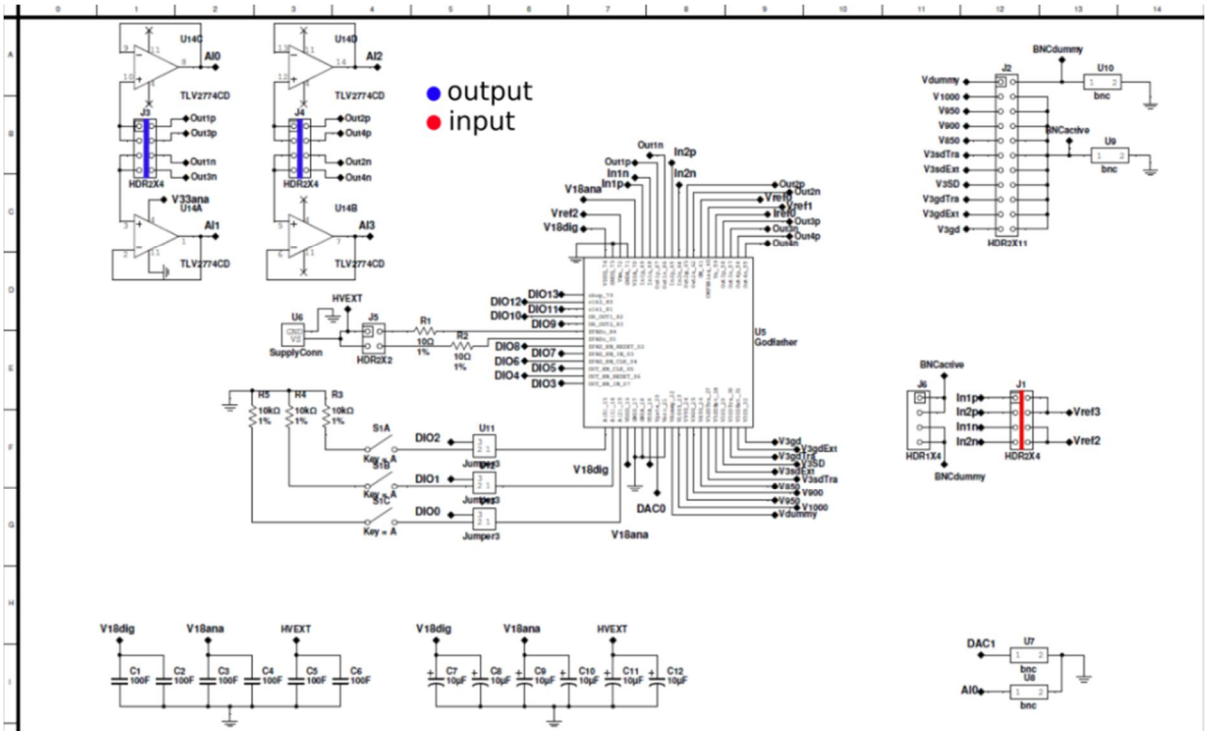

Figure 5-15: Daughter board for chip characterization

5.5 CHIP CHARACTERIZATION

The chip characterization includes testing and measuring the electrical parameters of the designed readout interface when stimulated with an external input and/or with THz radiations. In this section, the measurement setup and the characterization results are presented.

5.5.1 Electrical Characterization

Electrical characterization is performed by applying an external stimulus to one of the channels. This is achieved by doing a frequency sweep of sinusoidal waveform and measuring the output amplitude using oscilloscope. For example, Figure 5-16 shows the transient response of the readout channel when it is simulated by a 0.5 kHz sinusoidal waveform with a signal of 400μV_{PP} amplitude.

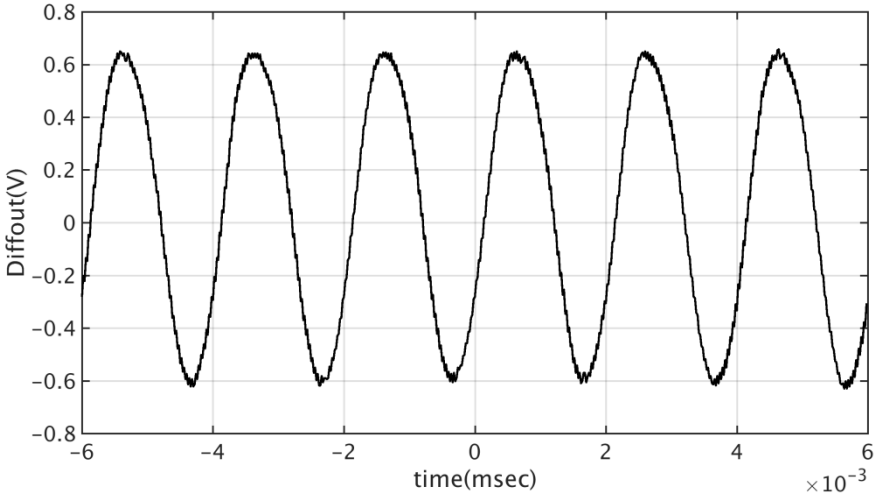

Figure 5-16: Differential transient output of the pixel when stimulated by 400 μV_{PP} sine wave

In this way, the transient response of the pixel to a fixed signal frequency sinusoidal waveform with varying amplitude is determined. Similarly, the frequency response is obtained by using fixed amplitude but varying signal frequency sinusoidal input. The comparison between the measured frequency response and the Periodic AC analysis (PAC) simulations indicates that the readout channel achieves a DC gain of 70 dB with a 1 kHz system bandwidth close to the simulated DC gain of 70 dB as shown in the Figure 5-17. The noise characterization measurement shows that the total integrated input referred noise of the readout channel is less than 2.15µVrms for 1 kHz bandwidth.

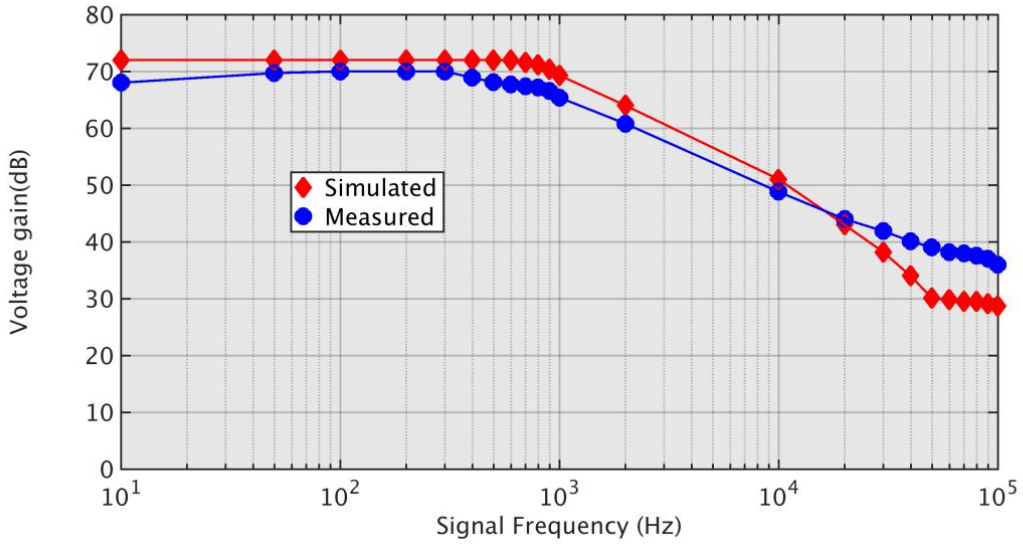

Figure 5-17: PAC simulated and measured frequency response of the pixel

5.5.2 THz characterization

In order to do the THz characterization of the designed pixel, a test setup similar to the one described in Chapter 3 is used. As shown in Figure 5-18, it consists of a continuous wave THz source which can be electrically modulated up to 1 kHz frequency and an automated acquisition board to capture the pixel output. Moreover, the measurements regarding the input power P_{IN} and the effective pixel area (A_{EFF}) are also completed by using the reference pyroelectric detector [83]. On the basis of receiver antenna directivity, the pixel area illuminated by the impinging THz radiations is calculated to be 0.197mm^2. This is very close to the physical area of the on-chip antenna, which, based on its dimensions of 500µm x 500µm is calculated to be 0.25 mm^2. Finally, by using the measured values of A_{EFF}, the P_{IN} received by the test pixel is calculated with a maximum value of 0.62µW.

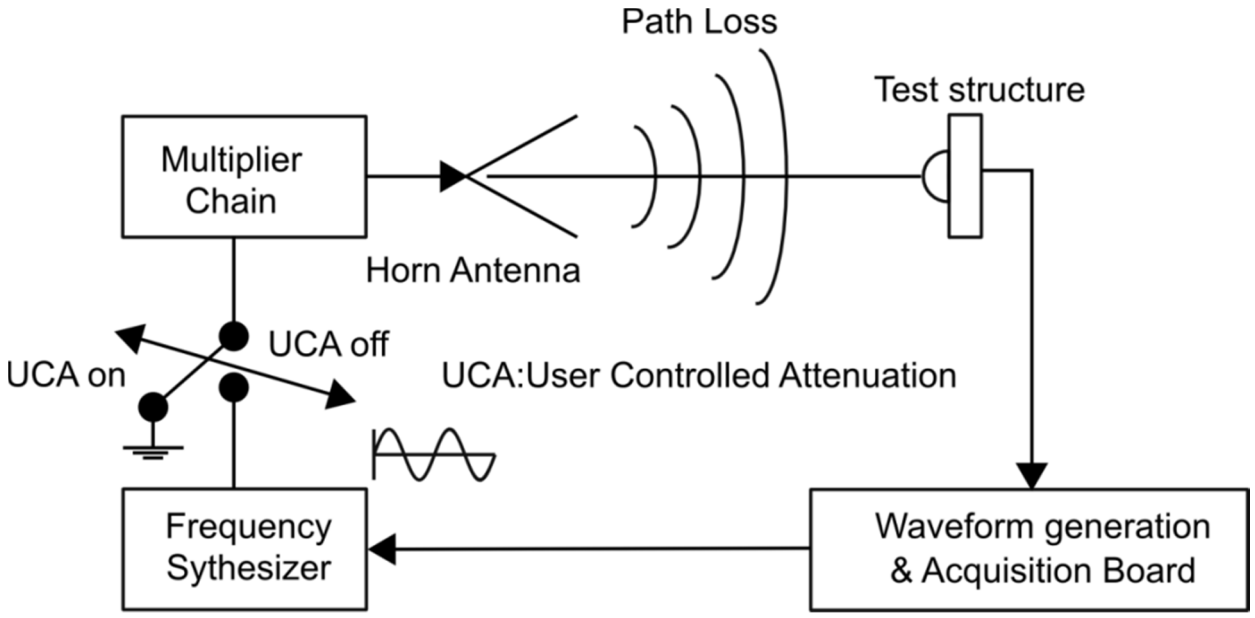

Figure 5-18: Test and measurement setup for THz pixel

5.5.2.1 Transient output

For the transient output voltage response, the pixel is exposed to a fixed THz frequency while electrically modulating the THz source at f_{MOD} and acquiring the pixel output using the data acquisition software. Due to the in-pixel signal processing, the FET voltage response is amplified by the DC gain of the channel and produces a robust signal level at the pixel output. Figure 5-19 shows the transient output when the THz source is modulated at 110 Hz, while the in-pixel chopping frequency f_{CHOP} is set to 50 kHz and the FET bias voltage is fixed to four different values. i.e. 450mV, 650mV, 850mV and 1V. The pixel output is sampled at 200 kHz, the clock frequency of the SC circuits. For a source modulation frequency of 110 Hz, the corresponding modulation time period of 9ms represents a single measurement which defines the amplitude of the output signal. This amplitude is obtained by averaging the sampled data points in both halves of the modulation cycle and subtracting them together.

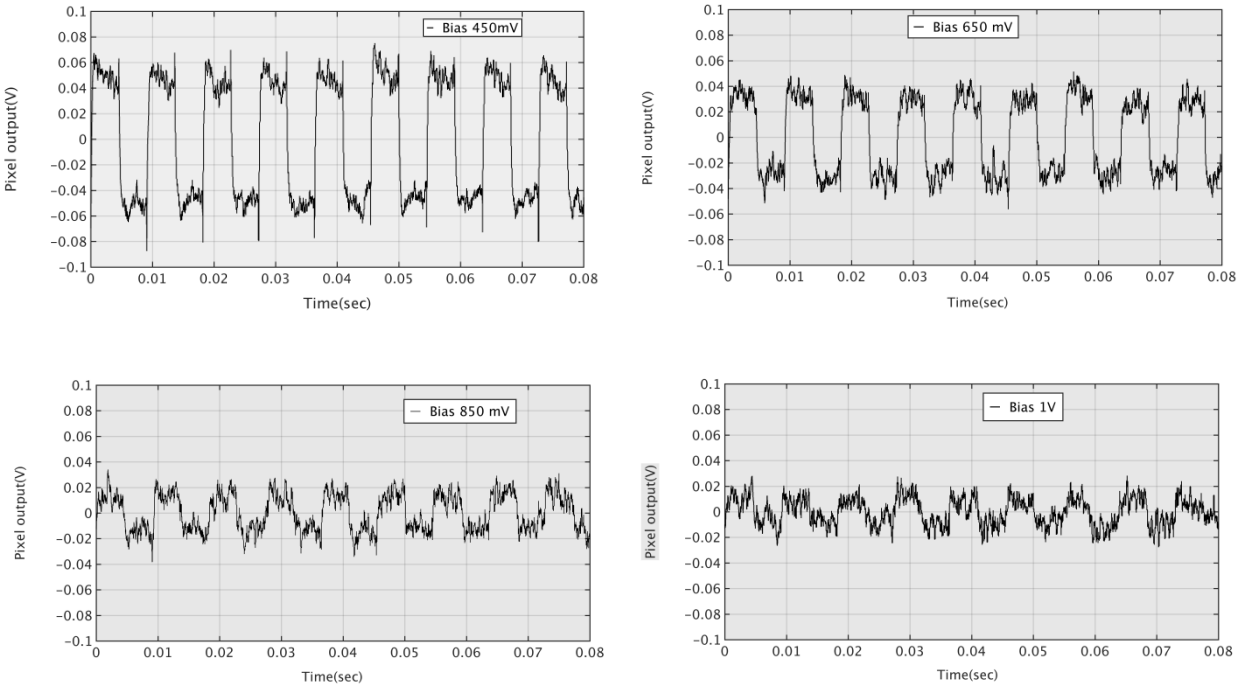

Figure 5-19: Pixel output at different gate bias voltages when illuminated with THz radiation

This process is repeated several times for multiple modulation cycles of 9ms, in order to extract the average signal amplitude and the standard deviation between measurements. The resulting amplitude for these bias voltages were calculated to be 110mV$_{PP}$, 80mV$_{PP}$ 45mV$_{pp}$ and 35mV$_{PP}$ respectively depicting how the amplitude decreases with an increase in the FET bias voltage due to bandwidth limitations. Anyway, a robust and highly amplified signal at the pixel output is obtained confirming the functionality of the readout channel.

5.5.2.2 Frequency response

The frequency analysis is performed by sweeping the THz source frequency, measuring the transient output of the pixel and determining the amplitude using the same procedure described above.

Figure 5-20Figure 5-20 shows the pixel output voltage as a function of the THz source for various modulation frequency values, when the FET is biased at 550 mV. The detector responds to the impinging radiation from 300 GHz onward, peaking at the antenna frequency of 370 GHz. In order to determine the voltage responsivity, the pixel response is divided by the calculated P_{IN} as explained in Chapter 3 and the

responsivity as a function of signal frequency is plotted in Figure 5-21. The voltage responsivity as a function of the FET gate bias voltage is also plotted in Figure 5-22 which shows the maximum responsivity value of 470 kV/W at 29 Hz source modulation frequency. It is worth noticing from these graphs that the responsivity decreases with an increase in the source modulation frequency. This is because of the limited system bandwidth of 1 kHz due to which the DC gain of the readout channel gain decreases from 70 dB. Moreover, the channel resistance of the FET detector R_{DS} makes a low pass filter with the sampling capacitor C_1 of the first stage, causing amplitude attenuation at high modulation frequency.

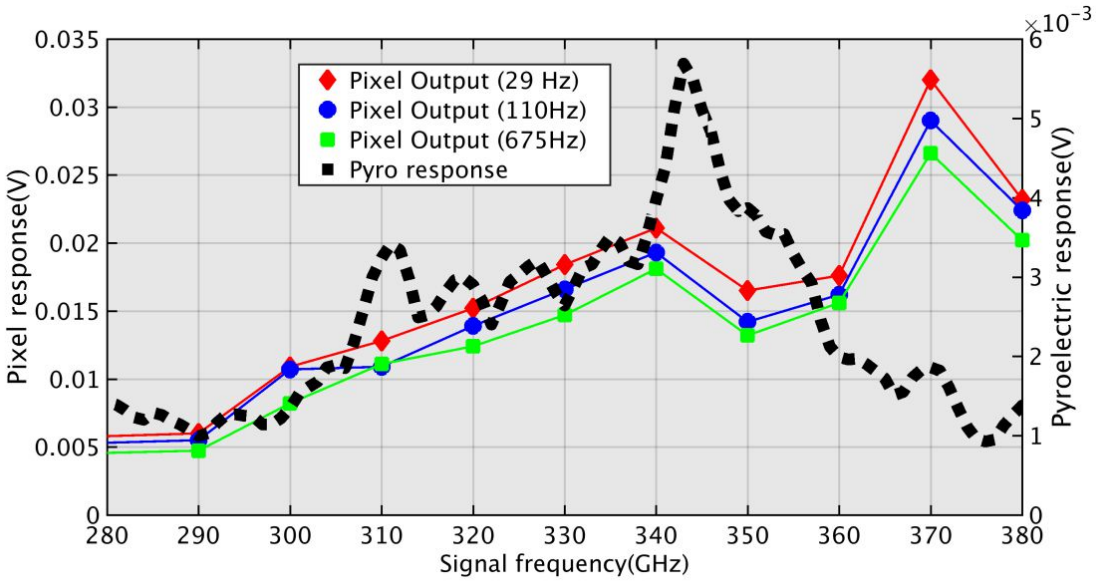

Figure 5-20: Pixel response as a function of THz frequency. The pyroelectric response (averaged) is also shown

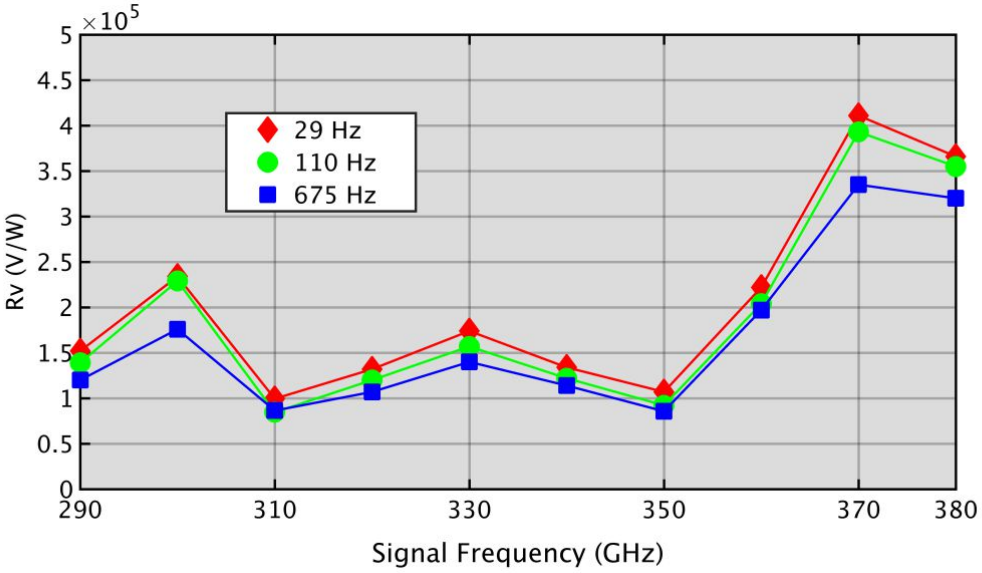

Figure 5-21: Voltage responsivity as a function of THz source frequency

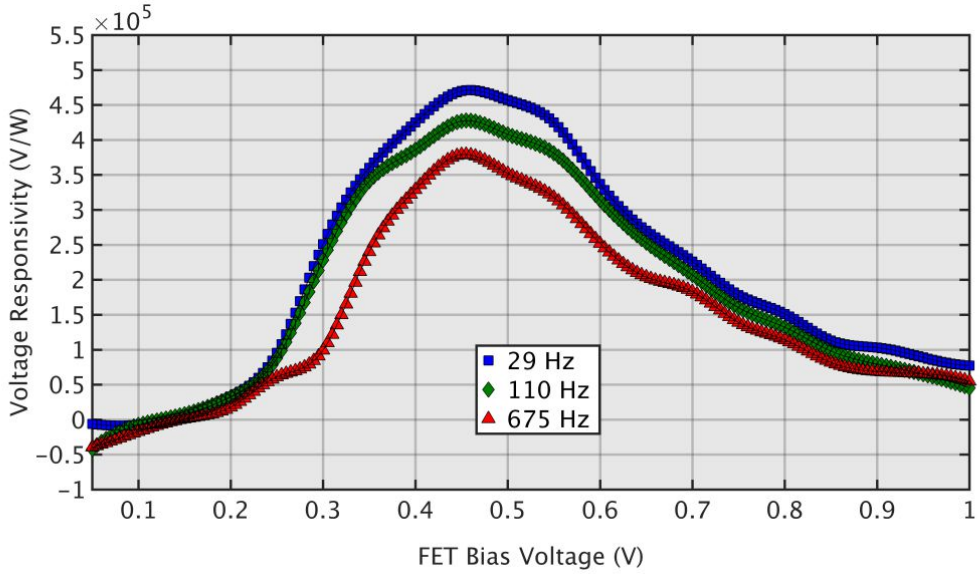

Figure 5-22: Voltage responsivity as a function of FET gate bias

5.5.2.3 Noise Equivalent Power

The NEP of the pixel can be calculated by measuring its noise voltage (V_N) and dividing it by R_V. This V_N is obtained from the transient output data, by taking the standard deviation of measurements [94]. By acquiring multiple measurements of

the transient output data, enough statistical data is gathered for accurate noise measurement readings. Using these values of the noise voltage, the NEP as a function of the gate bias voltage is plotted in Figure 5-23. The NEP of the standalone FET detector and the on-chip antenna (NEP_{FET}) is also plotted in the same Figure depicting its minimum value of 278 pW/√Hz while the minimum NEP of the readout interface is less than 90 pW/√Hz. By considering that both the active and dummy FET devices are used to realize the on-chip detector, it is to be noted that their NEP values are added in quadrature to make up for the total NEP of the detector (NEP_{DET}):

$$(NEP_{DET})^2 = (NEP_{FET})^2 + (NEP_{FET})^2 \tag{5.18}$$

Thus, the actual value of the detector NEP (NEP_{det}) is:

$$NEP_{det} = \sqrt{2}NEP_{FET} = 393\ pW/\sqrt{Hz} \tag{5.19}$$

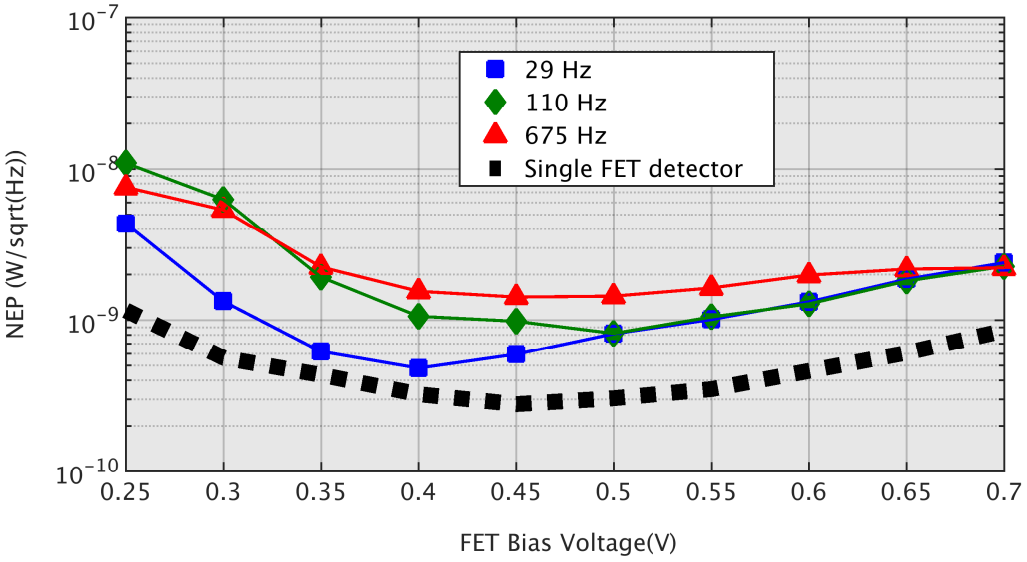

Figure 5-23: NEP as a function of FET gate bias

By looking at the graph and the NEP values, it is evident that the readout channel is introducing a very small amount of noise in the optimum bias conditions since it only increasing the NEP value from 393pW/√Hz to 480pW/√Hz. This confirms the low noise readout operation of the channel and also asserts that the NEP_{Pixel} is limited by the FET detector. From the graph it is also evident that the NEP_{Pixel} is

higher at low bias voltages. This is due to the high intrinsic resistance of the FET detector which increases the thermal noise. As the bias voltage increases, the resistance decreases which causes a strong decrease in the NEP_{det} until the $NEP_{readout}$ becomes dominant: this happens because the detector responsivity decreases whereas the readout noise remains constant. This noise is dominated by the thermal (kTC) noise of the SC configuration since the flicker noise of the readout channel is removed due to chopping.

5.5.3 Performance comparison with the SOA

Table 5-6 lists down the comparison of various design and performance parameters of the pixel with some of the published work. The pixel attains high responsivity at a very low source modulation frequency. Thanks to the carefully designed readout interface, the total integrated input referred noise of the interface is only 2.15µV for a system bandwidth of 1 kHz. This makes it possible to preserve the minimum NEP of the FET detector.

5.7 CHAPTER SUMMARY

A SC readout architecture for the signal processing of FET-detected THz radiation is presented in this chapter. The electrical characterization results indicate that the pixel achieves a maximum DC gain of 70 dB, while the total input-referred noise voltage of the interface is 2.15µV. The THz characterization of the pixel shows that the pixel achieves a large voltage responsivity value of 470 kV/W. Moreover, the channel is able to read and process the MDS of the FET detector and it is therefore optimized to preserve the NEP. The THz source is modulated at low frequency, making this pixel design able to work with commercially available THz sources with limitations in modulation frequency. This SC architecture is highly repeatable, as the channel gain and the transfer function can be adjusted using the clock frequency. Together with low power consumption, low noise and a small size, this pixel is suitable for a THz array configuration for an imaging application

Table 5-6: Comparison with the state-of-art

	This work [105]	[65]	[93]	[94] [95]	[96]	[67]
Technology (nm)	150	250	65	130	130	130
Gain (dB)	70	43	50	31-71	13.5	31
Power Consumption (mW)	0.2	5.5	0.0025	0.174	0.150	0.097
Input noise	2.15 µV	-	2.45 µV	0.2 µV	-	16nV/√Hz @ 30 kHz
Source Frequency (THz)	0.37	0.64	0.85	0.27	0.82	0.3
Modulation Frequency (kHz)	0.01-1	30	5	156	1000	0.400–30
Max. R_V kV/W	470	80	140	300	3.46	90
Min. NEP pW/√Hz	480 @ 29 Hz	300 @ 30 kHz	100 @ 5 kHz	18.7 @156 kHz	12.6 @1 MHz	-
Pixel size (µm x µm)	500x750	150x200	80x80	240×240	170x170	190x190
Lock-in Required	No	Yes	No	No	Yes	Yes

CHAPTER 6: THZ IMAGING ARRAY

In the previous chapter, the design of the readout interface for a FET based THz detector had been presented. The functionality of the single pixel employing this readout scheme was demonstrated with the help of simulation and measurement results. Still some aspects of the designed readout interface needed to be improved, especially for designing the THz imaging array.

1. **Power**: It was found out that the power consumed by the single pixel could be further reduced

2. **Area**: The readout channel comprised of a 3-stage design, with comparatively large capacitor values for the SC operation. Since these factors contribute in an increase in the chip area, it was found to essentially reduce the pixel area by reducing the number of stages and/or minimizing the capacitor sizes.

For this purpose, a new readout interface to be used for FET based THz detectors has been designed and fabricated in the standard 0.15µm CMOS technology. The new architectures limits the number of stages to two while also minimizing the capacitor sizes, thereby reducing both power and area. In the following sections the details of the readout channel of a single pixel are discussed. The simulation results are also presented which demonstrate the proper functionality of the design. Based on this, an 8 x 6 THz imaging array has been fabricated.

6.1 SYSTEM LEVEL DESIGN OF THE READOUT CHANNEL

The system level design of the readout channel is shown in Figure 6-1 along with the signal and noise spectra at individual stages: A FET detector with an on-chip antenna is connected to a two-stage readout chain. Additionally, a dummy FET detector without antenna is used to provide the reference voltage for the differential configuration. The readout chain consists of a chopper based **S**witched **C**apacitor **B**and **P**ass **F**ilter (SC-BPF) followed by a **C**orrelated-**M**ultiple-**S**ampling (CMS) stage

for voltage accumulation and noise subtraction, thereby increasing the SNR while also performing the in-pixel noise removal of the first stage.

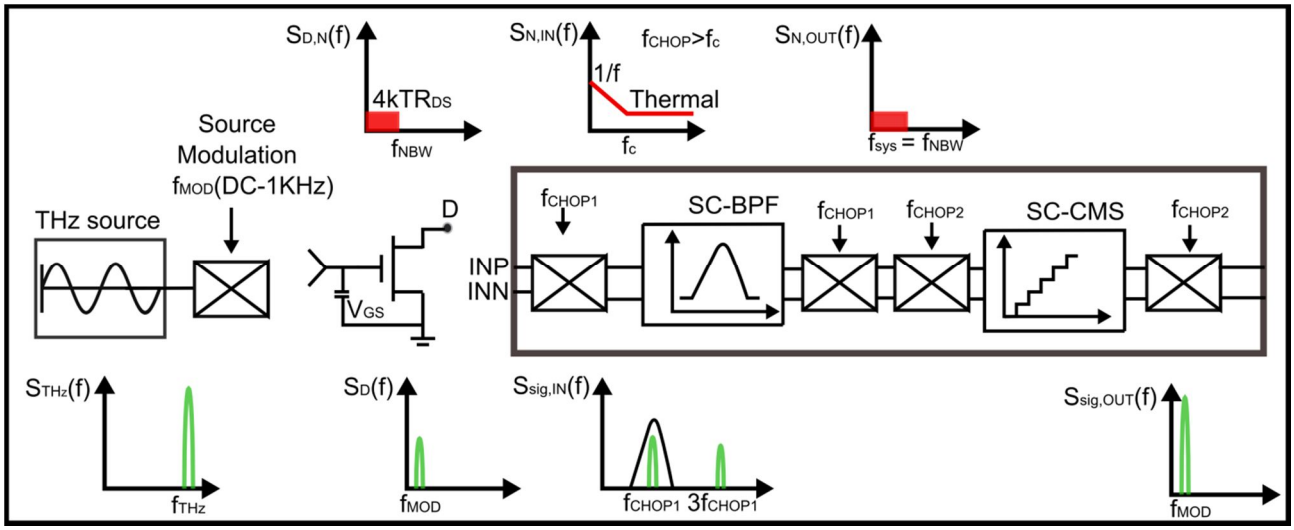

Figure 6-1: System level design of the readout channel

6.2 PROGRAMMABLE BANDPASS FILTER

In this section, the system and the circuit level design details of the bandpass filter are given. First, the theoretical analysis is presented with the help of the mathematical equations which is later followed by the practical implementation resulting in a **F**ully **D**ifferential (FD) SC-BPF.

6.2.1 Theoretical Analysis

Figure 6-2 shows the prototype of a multiple feedback, single operational amplifier **C**ontinuous **T**ime BPF (CT-BPF). This architecture is particularly useful to provide BPF functionality for low **Q**uality **F**actor (Q). The general **T**ransfer **F**unction (T.F) of a CT-BPF with a DC gain $H_{0,}$ angular frequency ω_0 and the capacitor coefficient ratio α is:

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = -\left(\frac{H_0\omega_0(s)}{s^2 + \alpha\omega_0(s) + {\omega_0}^2}\right) \qquad (6\text{-}1)$$

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = -\frac{s\left(\frac{1}{R_1 C_1}\right)}{s^2 + s\left(\frac{C_1+C_2}{C_1 C_2 R_3}\right)} + \frac{1}{C_1 C_2 R_3}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \quad (6\text{-}2)$$

where Q, H_0 and ω0 are given by:

$$Q = \frac{\omega_{CENTER} C_2 R_3}{2} \quad (6\text{-}3)$$

$$H_0 = \omega_{CENTER} C_2 R_1 \quad (6\text{-}4)$$

$$\omega_{CENTER} = 2\pi f_{CENTER} \quad (6\text{-}5)$$

Equations (6-1)-(6-5) present trade-offs involved in achieving quality factor, DC gain and area for a specific center frequency. Since small area is the main requirement for this readout interface, capacitor C_2 was minimized which consequently results in low Q and H_0. The low value of Q doesn't affect the filtering operation as the detected THz signal of the FET detector is bandlimited. The small value of H_0 in this stage is compensated with an additional (2nd) stage in the readout channel. The SC-BPF is designed for a center frequency f_{CENTER} of 125 kHz, the same value as the chopping frequency f_{CHOP1} of the first stage modulator which ensures that the signal of interest is amplified while the noise out of band is filtered. This filtering operation removes the offset and low frequency noise of the input devices of the BPF.

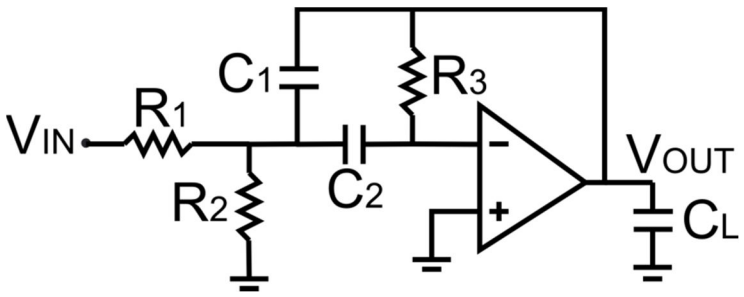

Figure 6-2: Single ended CT-BPF prototype

The actual implementation of the BPF is obtained by replacing the resistors of the CT filter prototype with the SC network [106] operating by using a pair of non-overlapping clock signals as shown in Figure 6-3.

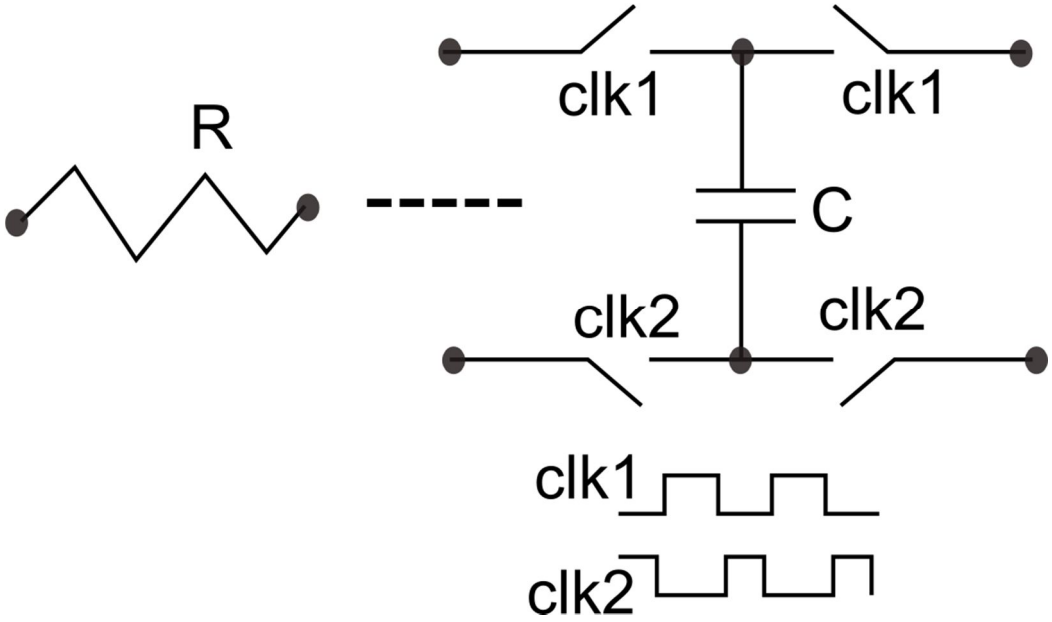

Figure 6-3: SC Equivalence of a resistor

6.2.2 Principle of operation

Figure 6-4 shows the chopper-stabilized FD SC-BPF where the resistors are replaced with their equivalent SC networks and its operation is as follows: The detected microvolt (µV) level DC signal is first transposed to the chopping frequency f_{CHOP1} of the chopper while the BPF then performs the filtering of this signal with its center frequency f_{CENTER} fixed to f_{CHOP1} after which the signal is demodulated back to the baseband. In this way the offset and 1/f noise of the amplifying MOSFET devices is removed. The chopping operation not only removes the low frequency noise of the readout front-end but also reduces the effective signal bandwidth, consequently reducing the total integrated thermal noise.

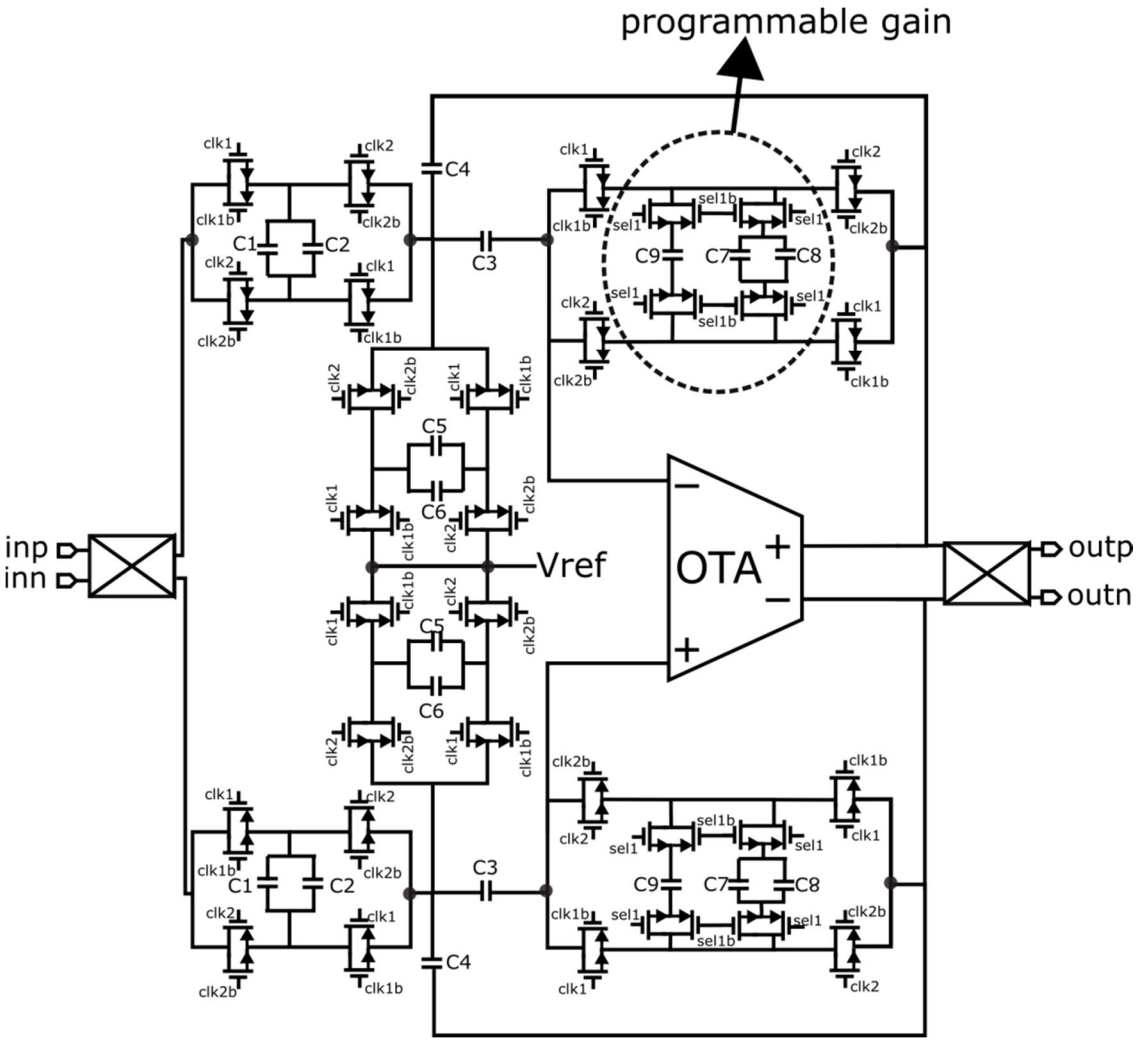

Figure 6-4: Chopper-stabilized FD SC-BPF based on the CT prototype of Figure-6.2

A programmable gain feature was added in this stage enabled by a digital signal 'sel' which changes the feedback capacitor values, thereby changing the center frequency, Q and gain.

6.3 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Single-stage OTA eliminates the need of employing any compensation network for stability purposes which makes the design process simpler compared to a multi-stage architecture [101], consequently decreasing the power and area. Moreover a multistage architecture produces more noise. Keeping in view these factors, a single stage FD folded cascode OTA configuration shown in Figure 6-5 is used.

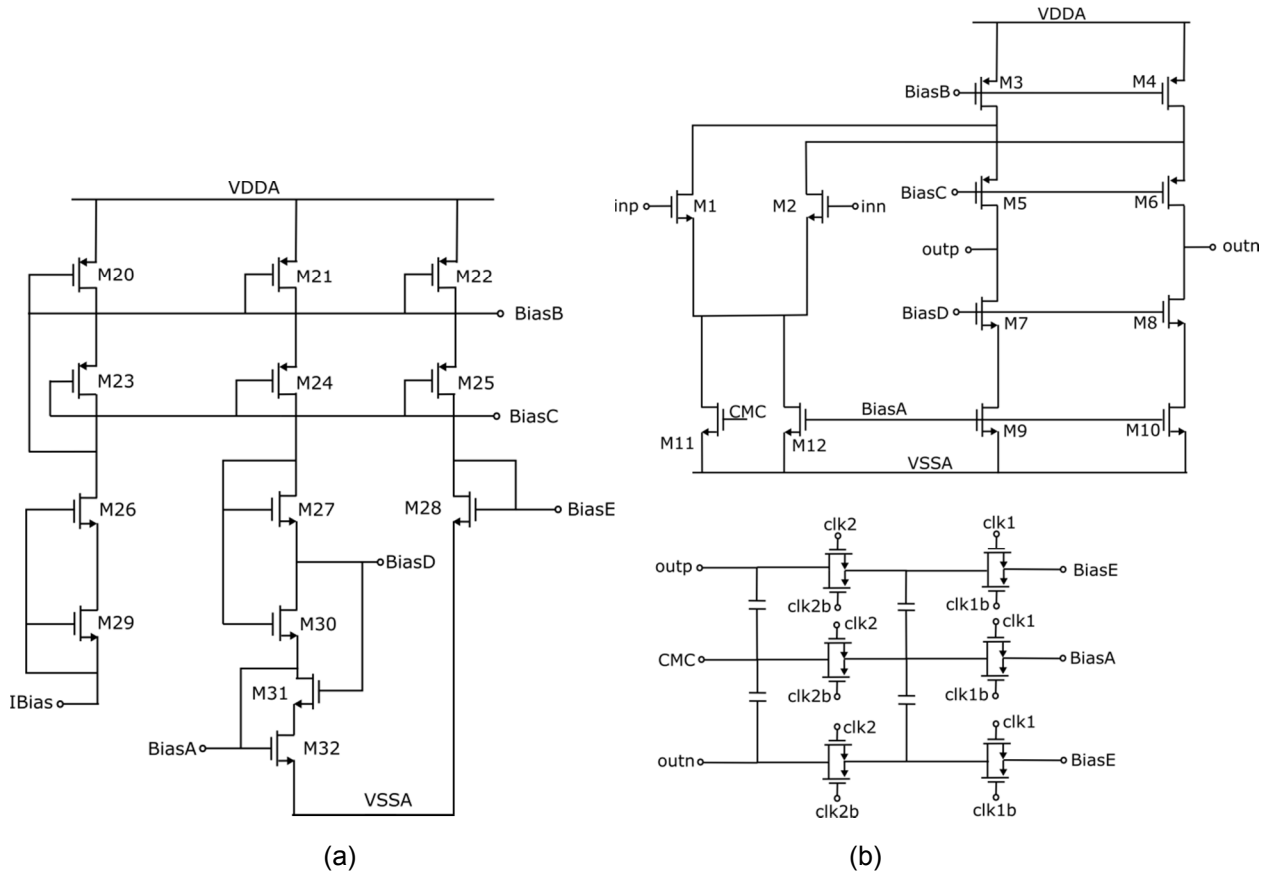

Figure 6-5: (a) Biasing circuitry (b) Folded Cascode OTA and SC CMFB Schematics

The system level specifications are listed down in Table 6-1 while the design details of the OTA and biasing circuitry are given in Appendix A. As previously mentioned, the design process was completed based on the g_m/i_d approach which helps in ensuring the optimal device sizes to achieve the required performance parameters.

The theoretical and simulated values of the important design parameters are listed down in Table 6-2.

Table 6-1: OTA system level specifications

Technology		0.15µm
DC gain	A_{DC}	70 dB
Gain Bandwidth	GBW	5 MHz
Phase Margin	PM	60°
Supply voltage	V_{DD}	1.8V
Bias current	I_{BIAS}	4 µA

Table 6-2: OTA: device level specifications

Transistors	***Region***	g_m/I_D ***[1/V]***	I_D ***[µA]***	V_{OV} ***[mV]***	***L [µm]***	***W/L [µm/ µm]***	***Multiplier***	***nf***
M1-M2	weak	23	3	60	2	5/2	4	1
M3,M4	strong	12.5	8	110	2	40/2	1	4
M5,M6	moderate	15	5	90	1	20/1	1	2
M7,M8	weak	20	5	75	1	10/1	1	1
M9,M10	weak	20	5	75	2	2.5/2	5	1
M11	weak	20	2	75	2	2.5/2	4	1
M12	weak	20	4	75	2	2.5/2	2	1

Table 6-3: OTA bias: device level specifications

Transistors	*L [µm]*	*W/L [µm/µm]*	*Multiplier*	*nf*
M20	2	20/2	1	2
M21	2	10/2	1	1
M22	2	20/2	1	2
M23	2	20/2	1	2
M24	2	10/2	1	1
M25	2	20/2	1	2
M26	2	2.5/2	1	1
M27	2	20/2	1	2
M28	2	10/2	1	4
M29	2	1/2	1	1
M30	10	0.5/10	1	1
M31	2	5/2	1	2
M32	2	5/2	1	2

6.3.1 OTA simulation results

6.3.1.1 Frequency response

The AC simulations of the OTA indicate that in an open-loop configuration the OTA achieves a DC gain of 70 dB with a 75°PM as shown in Figure 6-6.

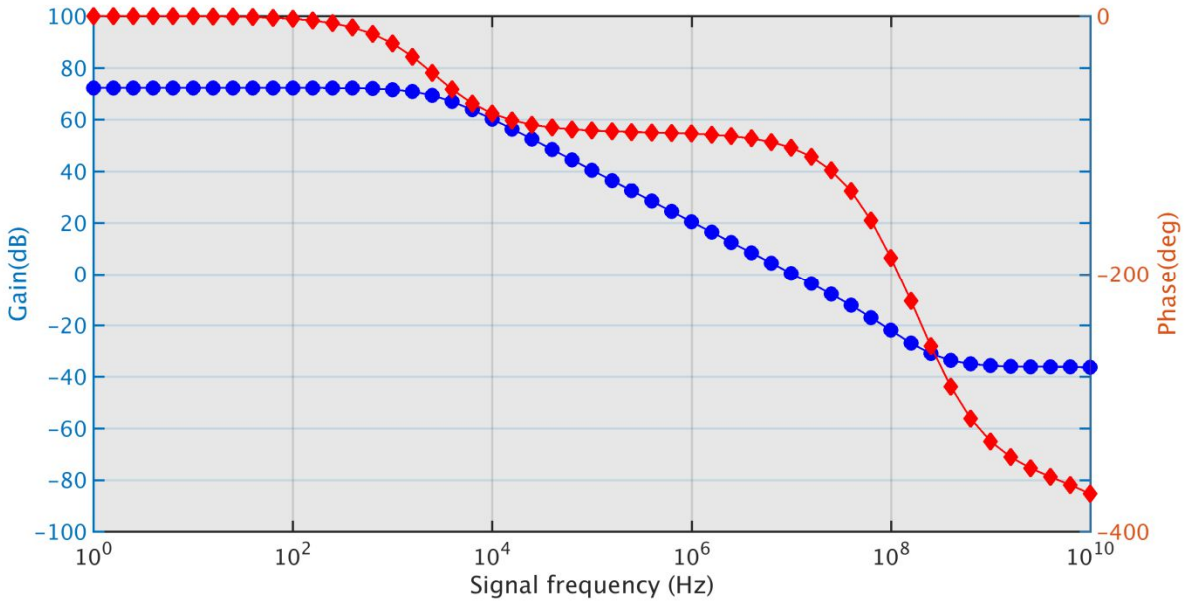

Figure 6-6: Open loop frequency response of the OTA

6.3.1.2 Noise analysis

The noise simulations of the OTA reveal that the RMS value of the total integrated input referred noise is 6.2µV with the bulk of the noise contribution as the flicker noise generated by the amplifying devices $M_{1,2}$ and $M_{5,6}$ as listed down in Table 6-4.

- Total Summarized Noise = 0.0546026
- Total Input Referred Noise = 6.23243e-06

Table 6-4: Noise contribution of OTA devices

Devices	Type	Noise Contribution	% Of Total
/I63/M6	flicker	0.0320378	34.43
/I63/M5	flicker	0.0320378	34.43
/I63/M1	flicker	0.0215076	15.52
/I63/M2	flicker	0.0215076	15.52
/I63/M1	thermal	0.000988823	0.03
/I63/M2	thermal	0.000988823	0.03
/I63/M6	thermal	0.000753137	0.02
/I63/M5	thermal	0.000753137	0.02

6.3.1.3 Monte Carlo Simulations

The device mismatches as well as random variations during the fabrication process can greatly affect the behavior of the designed circuit/chip. For this particular reason, the Monte Carlo (MC) simulations are performed in order to study the electrical behavior of the circuit under device mismatch and process variations by analyzing a large set of circuit instantiations by randomly varying devices [107]. The MC simulations of the OTA frequency response for 200 samples were performed and the results are shown in Figure 6-7. The mean value of the OTA GBW and PM are 5.22MHz and 83◦, respectively.

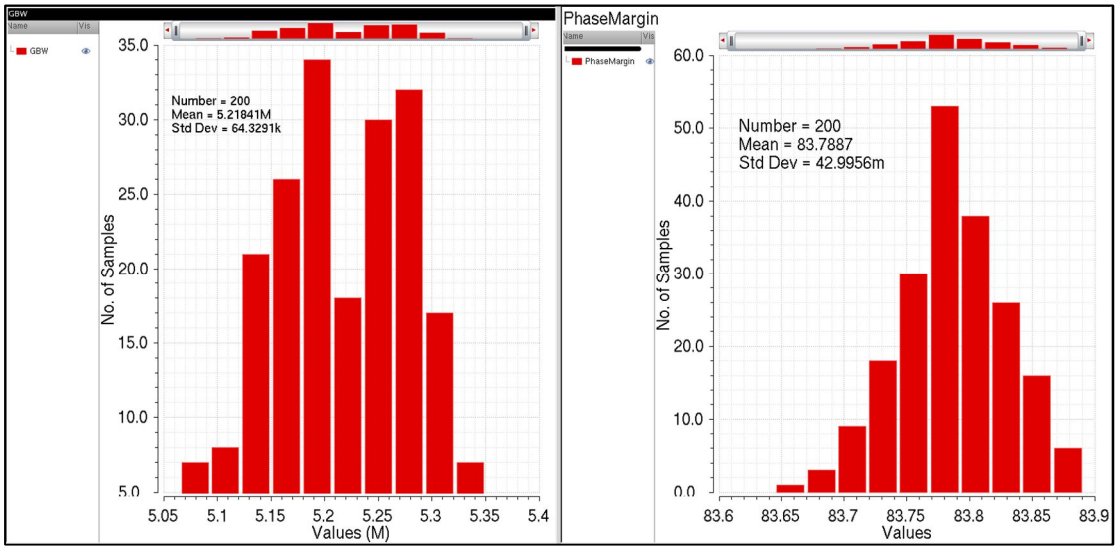

Figure 6-7: MonteCarlo simulations of the folded cascode OTA GBW and PM

6.3.2 Simulation Results of the SC-BPF

The Periodic AC simulations (PAC) shown in the Figure 6-8 depict the frequency response of the chopper-stabilized SC-BPF, achieving a DC gain in excess of 14 V/V.

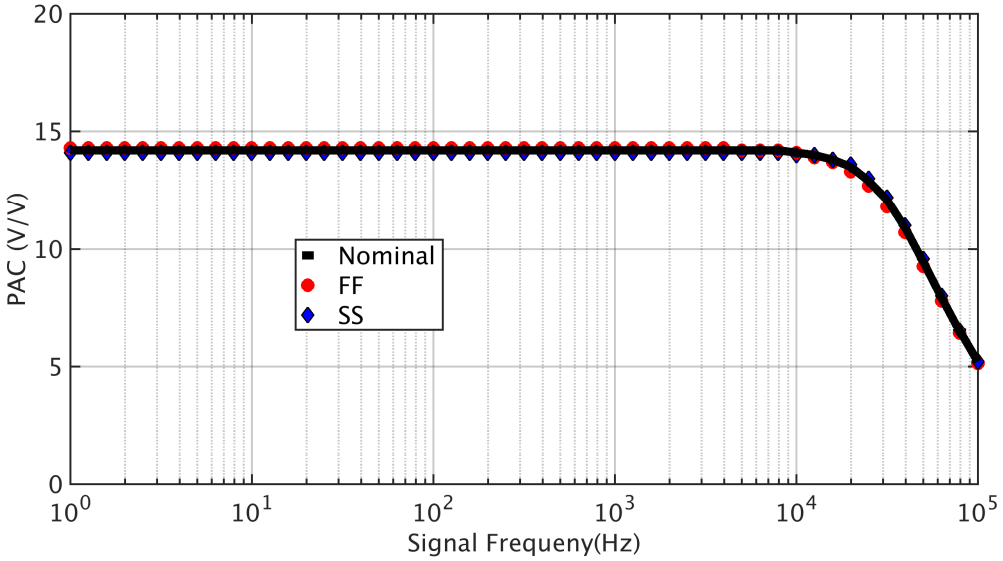

Figure 6-8: PAC gain of SC-BPF

6.4 CORRELATED MULTIPLE SAMPLING

6.4.1 Principle of operation

The second stage of the readout interface is the Correlated Multiple Sampling (CMS) [108] [109].Figure 6-9 shows the circuit diagram of this stage and the relevant transient signals. Its operation starts with the resetting of the OTA to remove the offset by storing it on the feedback capacitor C_2. This offset is later subtracted from the input signal the following cycle. Thereafter, the BPF output is sampled on the sampling capacitor C_1 by closing the switch 1a. In the next phase 2a, the charge stored on C_1 is transferred to C_2 which contributes to the *voltage accumulation* at the output node and the ratio of C_1/C_2 defines the voltage gain.

After the voltage accumulation, the noise subtraction of the first stage output is performed by first sampling the noise on C_1 during 1a phase and then transferring it to C_2 during phase 2b with the opposite polarity. This charge is subtracted from the charge already deposited on C_2 during 1a. This process of voltage accumulation and noise subtraction can be performed multiple times within one time period, making this a highly repeatable system which increases the SNR of the system. Due to the continuous voltage accumulation, the resetting of the OTA can be performed only once before the first signal sampling starts.

The downside of this approach is the accumulation of the OTA offset and flicker noise in every integration cycle, leading to the saturation of the stage. To remove this low frequency noise, the OTA is enclosed by a modulator/demodulator, operating at the chopping frequency f_{CHOP2} which shifts the offset out of the system bandwidth. This approach is validated by performing the MC simulations explained in the later section.

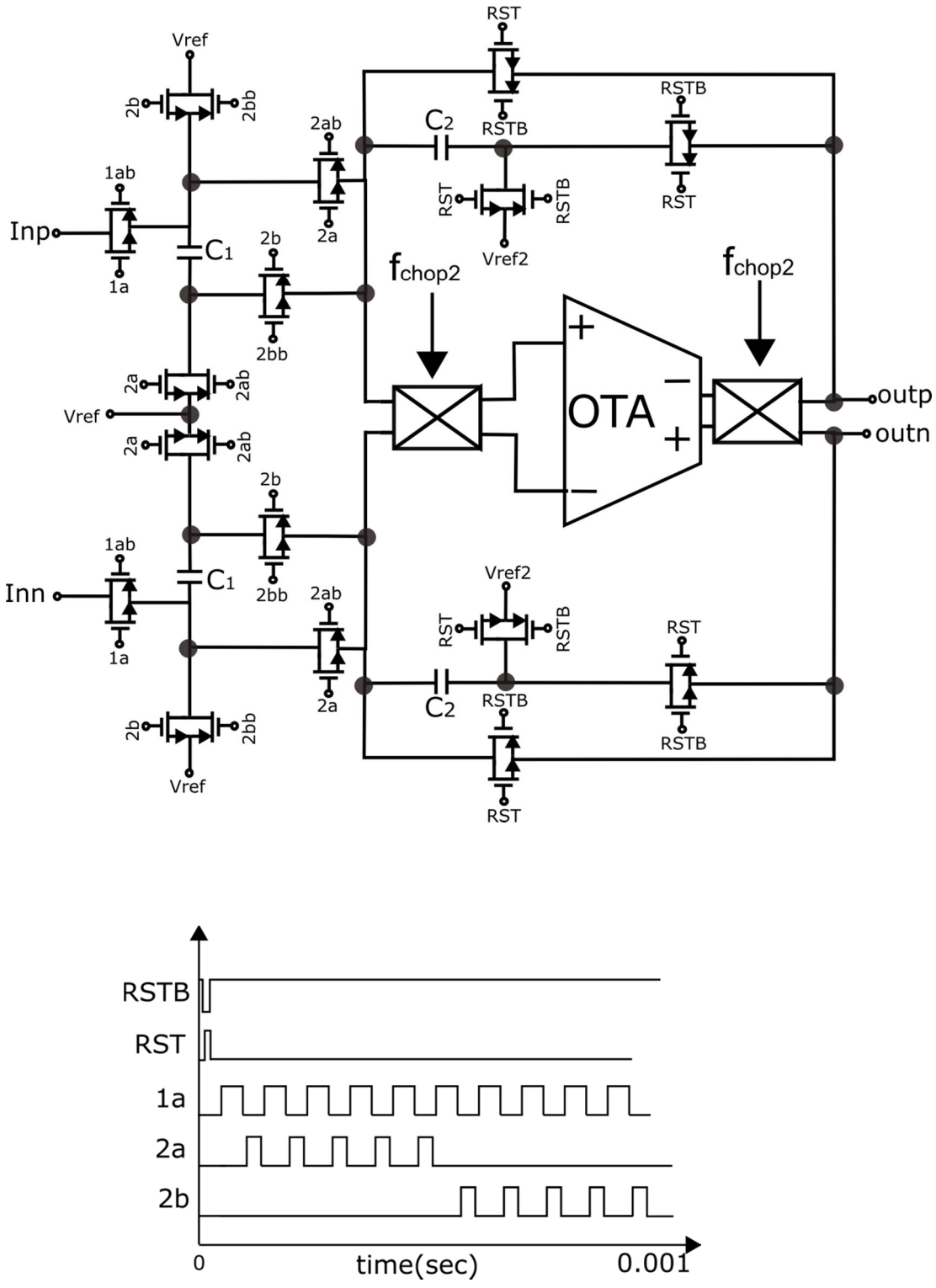

Figure 6-9: Circuit diagram of the SC-CMS (top) and the transient signal (bottom)

6.4.2 Simulation Results

To confirm the functionality of this stage, both AC and transient simulations are performed in Cadence. The value of the sampling (C_1) and integration (C_2) capacitors were fixed to 500 fF and 100 fF, respectively with a voltage gain of 5 V/V. The charge transfer takes place 5 times in each integration cycle, leading to a total integrated voltage gain of 25 V/V as depicted by the frequency response of Figure 6-10.

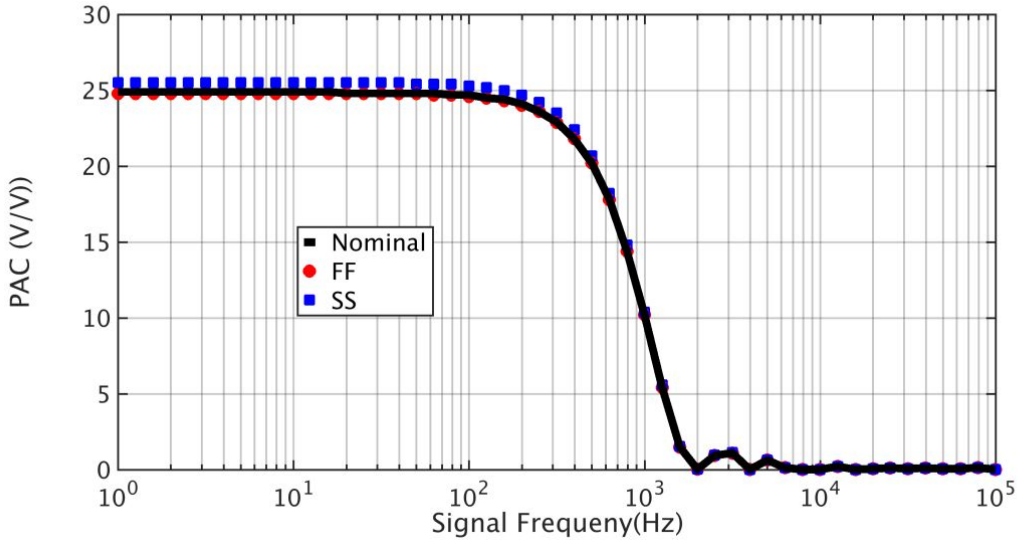

Figure 6-10: PAC simulated frequency response of SC-CMS

Figure 6-11 shows the transient response of the SC-CMS stage when it is stimulated with a $5\mu V_{PP}$ input signal. The circuit shows a voltage integration of 5 V/V during each charge transfer phase (1a and 2a) in every integration cycle, leading to a final output voltage of 125µV, confirming the expected functionality of the stage.

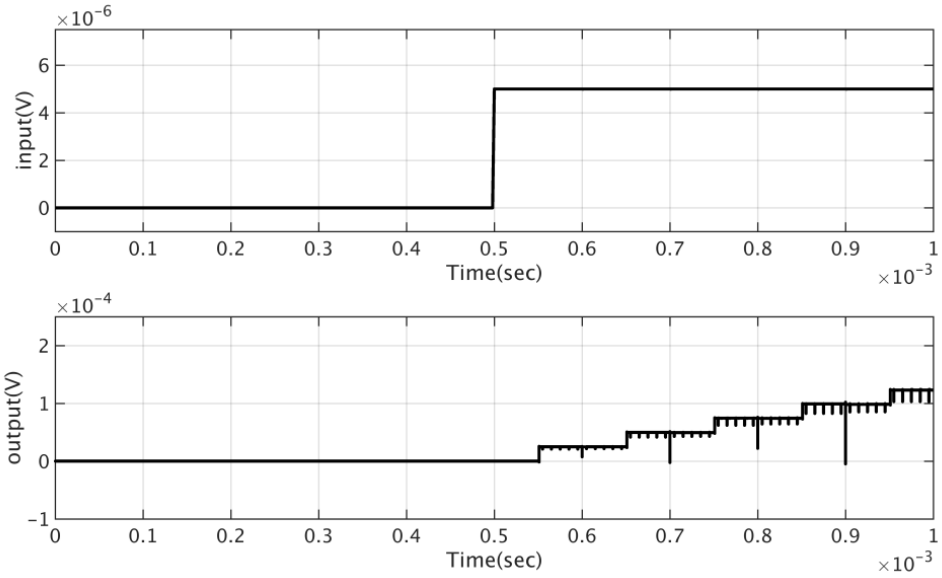

Figure 6-11: Simulated time response of SC-CMS when stimulated with 5µVPP input signal

6.5 PIXEL SCHEMATIC

The overall circuit architecture of the pixel is shown in Figure 6-12.The readout interface is designed to achieve an overall programmable gain of either 325 or 800 V/V. The programmability feature is implemented in the BPF stage, by selecting the appropriate capacitor values using digital signal 'sel'. In turn, the filter can be fine-tuned to a center frequency of either 125 kHz or 200 kHz to properly implement the filtering in both the cases. The timing diagram involving digital signals to perform the pixel circuit operation is shown in Figure 6-13. The functionality of the signals is explained below.

a) chop1

This signal drives the modulator/demodulator of the SC-BPF. Its value depends on which configuration of SC-BPF is selected using 'sel' signal. There are two options to configure this signal:

1. ***sel: high***

   Fixing this setting will result in selecting the feedback capacitance value of 28.5 fF. The SC-BPF will be configured to the center frequency of 125 kHz

while the clock frequency is fixed to 750 kHz. The BPF attains a DC gain of 32 V/V while the overall voltage gain of the pixel is around 800 V/V.

2. ***sel: low***

   Changing 'sel' signal to low value results in selecting the feedback capacitor of 80 fF value, which helps in achieving a DC gain of 13 V/V. This also changes the center frequency of the BPF to 200 kHz and the overall voltage gain of the pixel is approximately 325 V/V.

Table 6-5: System level specifications

sel	f_{CHOP1} *[kHz]*	f_{CLK1} *[kHz]*	f_{CENTER} *[kHz]*	*BPF gain [V/V]*	*Feedback cap [fF]*	*Pixel gain [V/V]*
high	125	750	125	31	28.5	800
low	200	800	200	13	80	325

The capacitor values used in both stages of the readout interface, as well as to implement the programmability feature of SC-BPF are listed down in Table 6-6.

Table 6-6: Capacitor values

sel	C_1,C_2	C_3	C_5,C_6	C_7,C_8	C_9	C_{10}	C_{11}
high	0.8pF	1pF	0.4pF	-	28.5fF	0.5pF	0.1pF
low	0.8pF	1pF	0.4pF	40fF	-	0.5pF	0.1pF

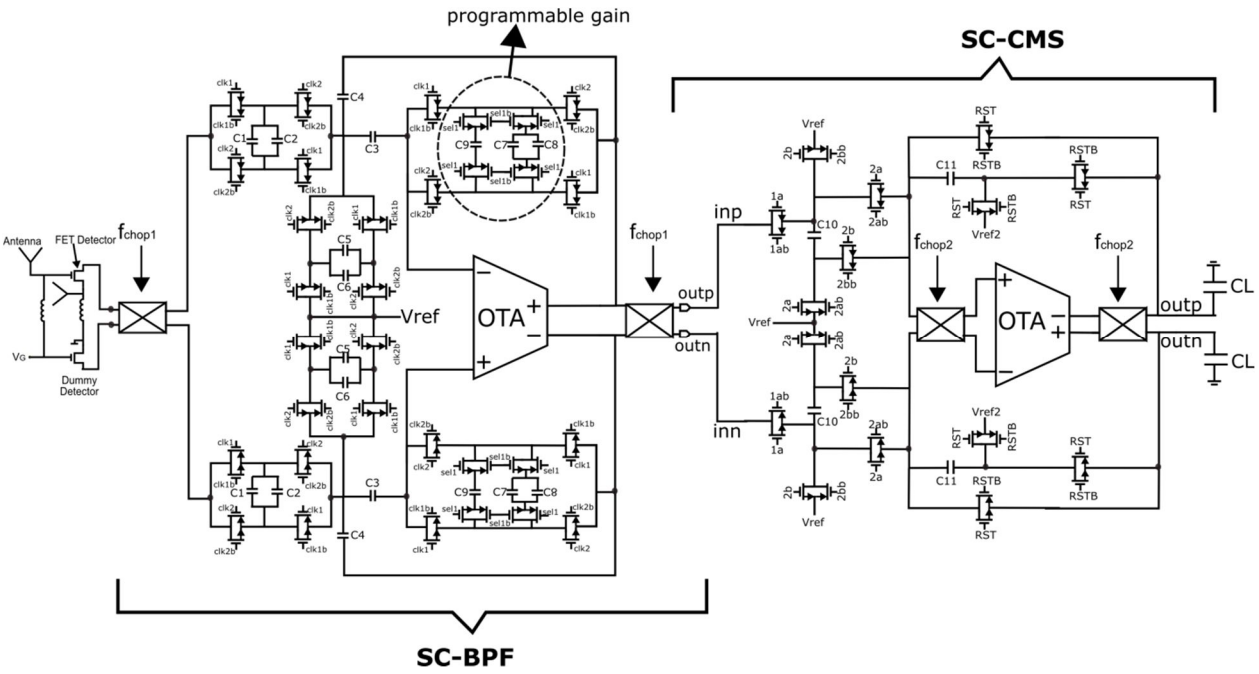

Figure 6-12: Circuit diagram of pixel schematic

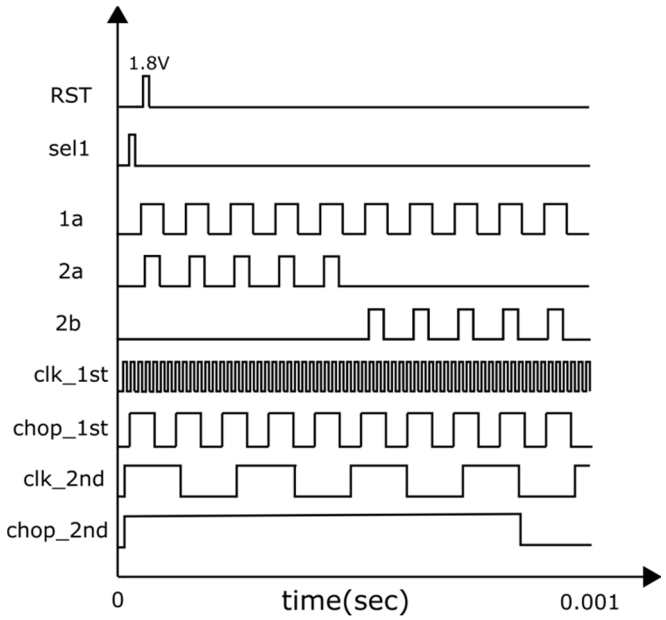

Figure 6-13: Timing waveforms

6.5.1 Simulation Results

6.5.1.1 Frequency and transient response

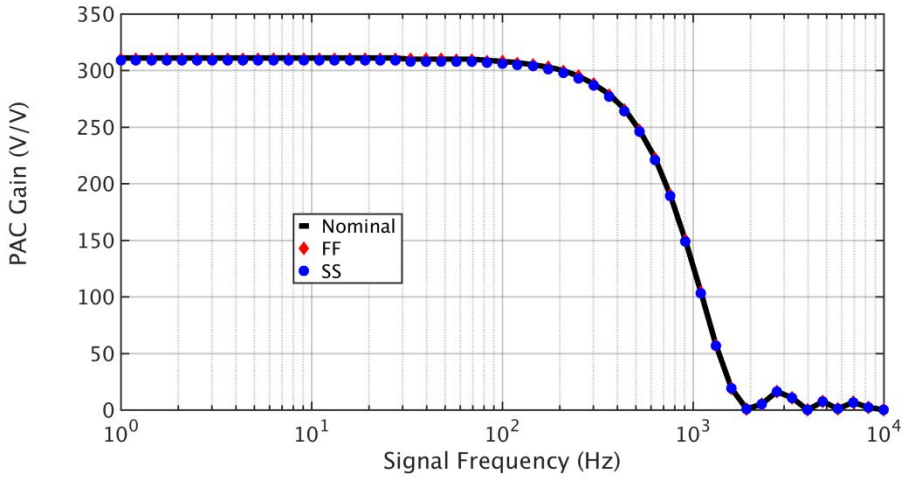

Figure 6-14: PAC frequency response of the pixel (sel: high)

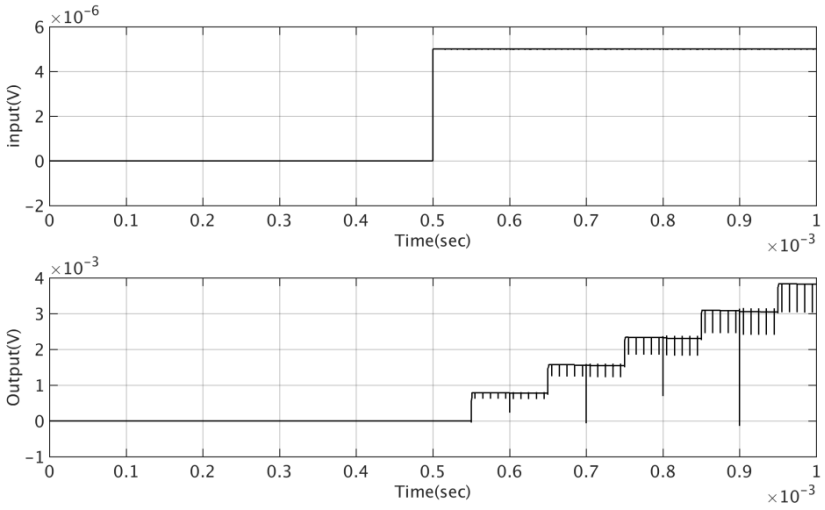

Figure 6-15: Transient response of the pixel when stimulated with 5μV input signal (sel: low)

6.5.1.2 MonteCarlo Simulations

In order to determine the effectiveness of the offset removal operation made by the chopper and CMS, MC simulations were performed.

a) Without Chopper based Correlated Multiple Sampling

The effect of the input offset on the readout interface is clearly visible from the MC simulations of Figure 6-16. These simulations are performed without the modulator/demodulator of the CMS stage [109]. For example, in (a) the MC simulations of 50 samples with no stimulus is shown. It is evident that the input offset is amplified as the voltage integration progresses, which is very visible at the end of one period (1ms). The same effect is evident in (b) and (c) when the channel is stimulated with a 2.5µV and 100µV input signal which shows that in the absence of a chopper stabilized CMS stage, the input offset saturates the readout channel.

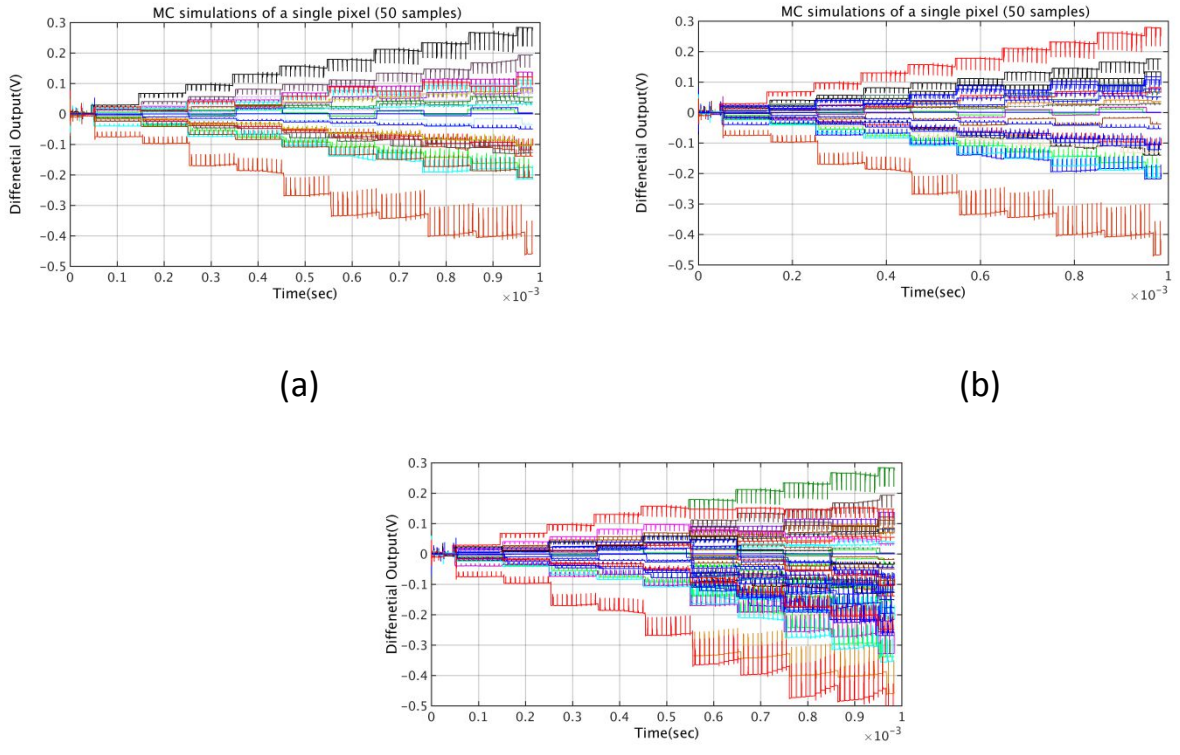

Figure 6-16: MC simulations of the pixel showing the presence of an input offset saturating the readout channel in the presence of (a) no input signal (b) 2.5µV and (c) 100µV input signal

b) <u>With Chopper based Correlated Multiple Sampling</u>

To verify whether the inclusion of chopper in second stage works, the same set of MC simulations is repeated and Figure 6-17 shows that the offset is removed, thanks to the chopper action. Moreover the low frequency noise is cancelled as well. This is more clearly visible by comparing the simulations in (a) and (c) which depicts the progressive voltage integration when the readout channel is stimulated with a 100µV input signal. Anyway, this graph also tells that the channel is not able to distinguish a 2.5µV signal from the non-uniformities. A further external frame calibration is therefore needed.

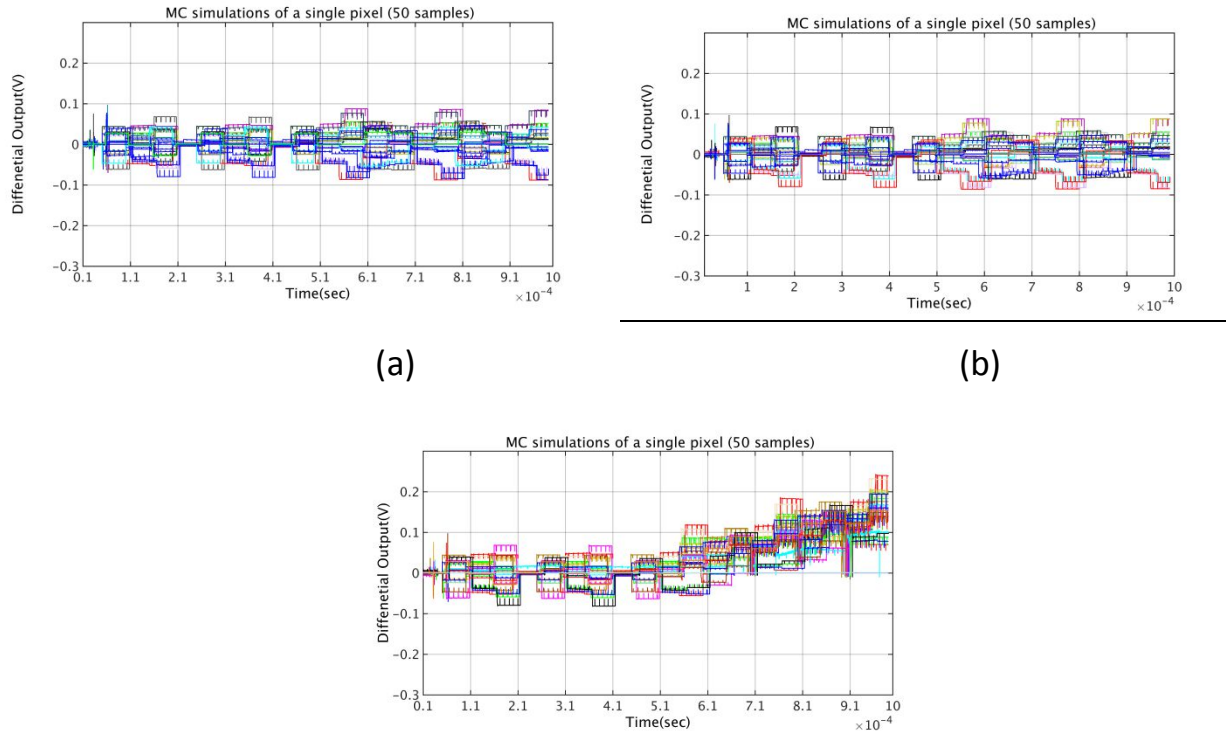

Figure 6-17: MC simulations of the pixel with a chopper stabilized SC-CMS stage in the presence of (a) no input signal (b) 2.5µV al and (c) 100µV input signal

6.6 THz IMAGING ARRAY

Based on the readout interface described above, an 8x6 array as shown in Figure 6-18 is designed and implemented in the same 0.15µm technology. Some of the building blocks are discussed below.

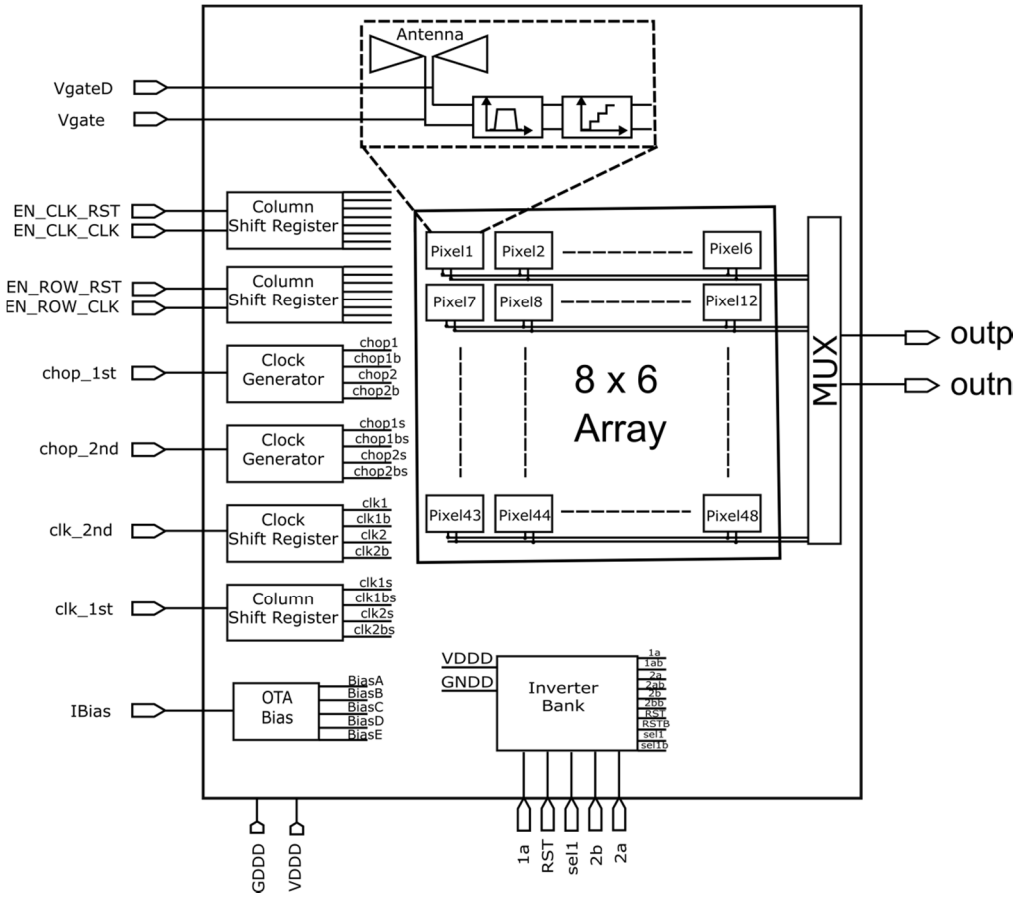

Figure 6-18: An 8 x 6 THz imaging array and the relevant building blocks

6.6.1 Shift Register

The THz imaging array is operated using row and column **S**hift **R**egisters (SR) consisting of the **D** type **F**lip **F**lops (DFF) as shown in the Figure 6-19. The EN_RST signal resets the FF which then changes the state on the rising edge of the EN_CLK signal. The pixel outputs are selected by using an analog multiplexer (A-MUX) which consists of a total of 8 complementary MOSFET switch configuration. The device

sizing of the MOSFETs was fixed to minimum dimensions in order to reduce the loading of the array output.

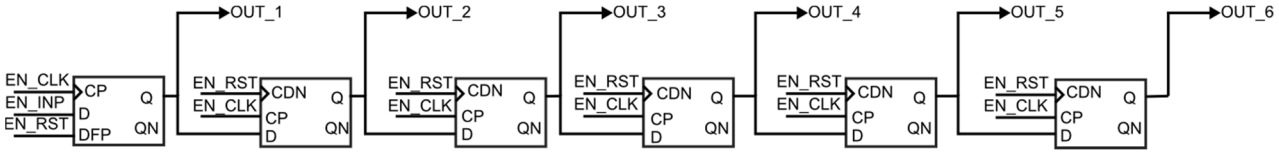

Figure 6-19: A 6-bit SR configuration

6.6.2 Layout

The layout of the single pixel including the on-chip antenna is shown in Figure 6-20. The readout interface is compatible with antenna size the pixel occupies an area of 455µm x 455µm, thus reducing the pixel area by almost 2 x compared to the pixel in Chapter 5. Large capacitors were used to decouple the supply rails of 1.8V and ground.

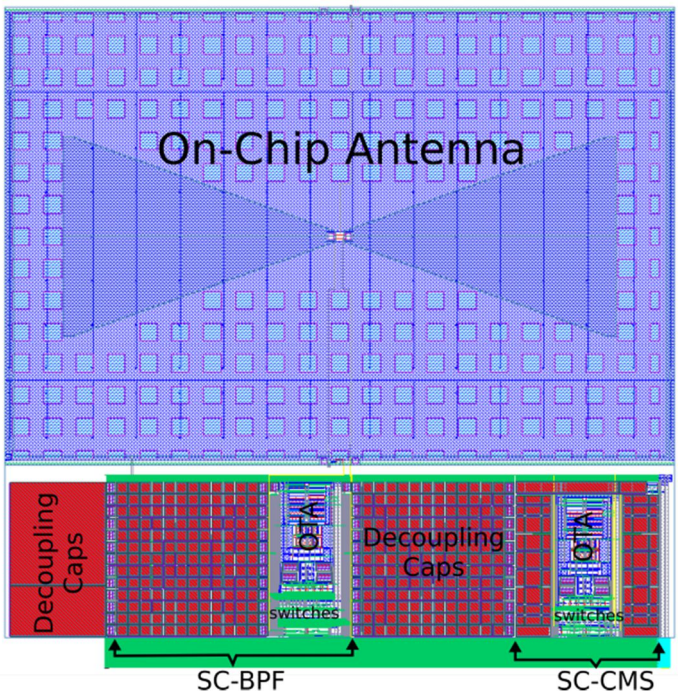

Figure 6-20: Layout of the single pixel including the on-chip antenna

Figure 6-21 shows the layout of chip. The core consists of some test structures for electrical characterization and THz imaging array which occupies a total area of 3.64mm x 2.73mm

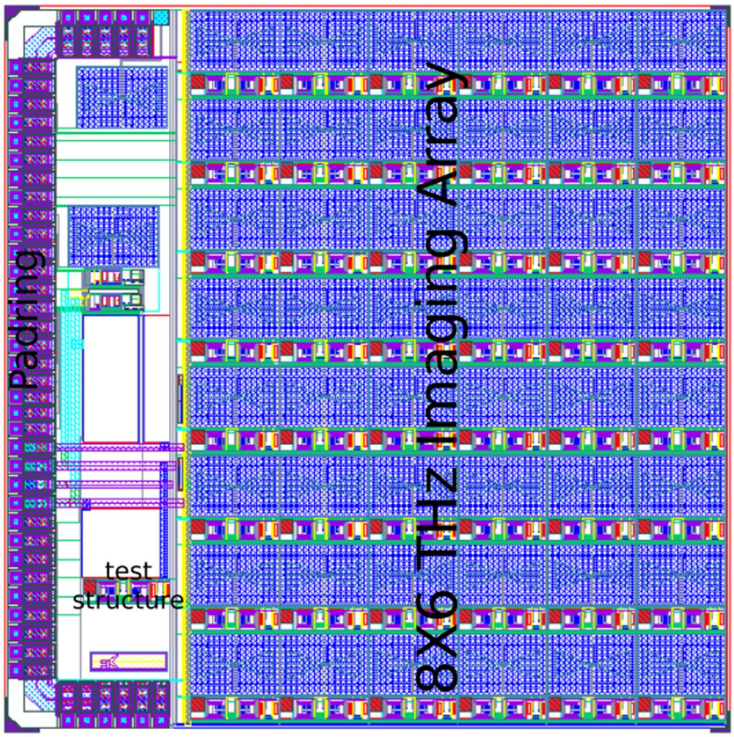

Figure 6-21: Chip: Core and Padring

6.7 CHIP FABRICATION

Figure 6-22 shows the chip micrograph which is fabricated in 0.15µm, 6 metal CMOS process technology which provides **M**etal-**I**nsulator-**M**etal (MIM) and thick metal options. The chip contains a single pixel test structure stimulated externally and an 8 x 6 imaging array of the on-chip antennae and readout channels. The on-chip antenna is implemented using back-end metals and has dimensions of 455µm x 355µm. The readout channel is smaller in dimensions as compared to the antenna: Thus, the rest of its area is filled with decoupling capacitors in order to fill out the vacant space and convert it into a regular structure for array configuration.

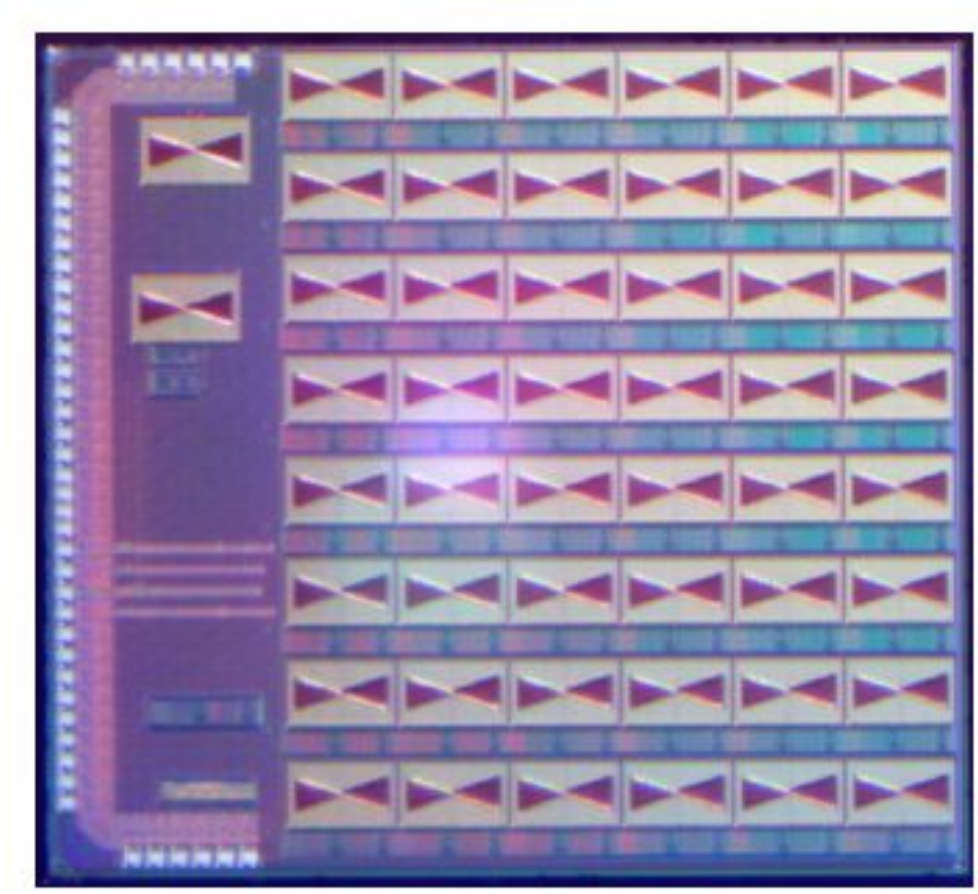

Figure 6-22: Chip micrograph: showing the readout channel test structure and imaging array

6.7.1 Electrical Interface

The overall chip architecture and pinout is described next.

6.7.1.1 Core

The core of the chip has following main parts

- Single pixel (THz readout) connected to external input.
- A 8 x 6 THz imaging array consisting of on-chip antennas & readout interface
- Clock generators
- OTA/OTA Bias generator

6.7.1.2 Pins Description

List and description of the pins are listed in Table 6-7.

Table 6-7: Pins name and description

Name	Dir	Type	Description
outp	O	Analog	Output of 8x6 array
outn	O	Analog	Output of 8x6 array
voutp	O	Analog	Output of single pixel
voutn	O	Analog	Output of single pixel
voutp1	O	Analog	SC-BPF output of single pixel
voutn1	O	Analog	SC-BPF output of single pixel
Vinp	I	Analog	Input of single pixel
Vinn	I	Analog	Input of single pixel
Ibias	I	Analog	Biasing current of OTA
Vref	I	Analog	Reference voltage of SC-BPF
Vref2	I	Analog	Reference voltage of SC-CMS
Vgate	I	Analog	DC voltage of Active FET
VgateD	I	Analog	DC voltage of Dummy FET
GNDD	I/O	Power	Digital & Analog Ground
VDDD	I/O	Power	Digital & Analog Supply
chop_1st	I	Digital	Chopping signal of 1st chopper
chop_2nd	I	Digital	Chopping signal of 2nd chopper
clk_1st	I	Digital	clock signal of 1st stage SC-BPF
clk_2nd	I	Digital	clock signal of 2nd stage SC-CMA
sel1	I	Digital	Select signal for PG SC-BPF
1a	I	Digital	Sample signal of 2nd stage SC-CMS
2a	I	Digital	Charge transfer signal of 2nd stage SC-CMS
2b	I	Digital	Charge subtraction signal of 2nd stage SC-CMS
RST	I	Digital	Reset Signal of 2nd stage SC-CMS
EN_COL_CLK	I	Digital	Clock Signal of Column SR
EN_COL_RST	I	Digital	Reset Signal of Column SR
EN_ROW_CLK	I	Digital	Clock Signal of Row SR
EN_ROW_RST	I	Digital	Reset Signal of Row SR

6.7.1.3 Testbench

The pictorial overview of the testbench for the characterization of single pixel is shown in Figure 6-23, depicting all the signals including input and output pins. The analog voltage and current signals (e.g. Vref, Vref2 etc) are generated from master board while the digital signals are coupled to the chip using LABVIEW automated program. For testing purposes, a test board of Figure 6-24 is designed and mounted on the master board.

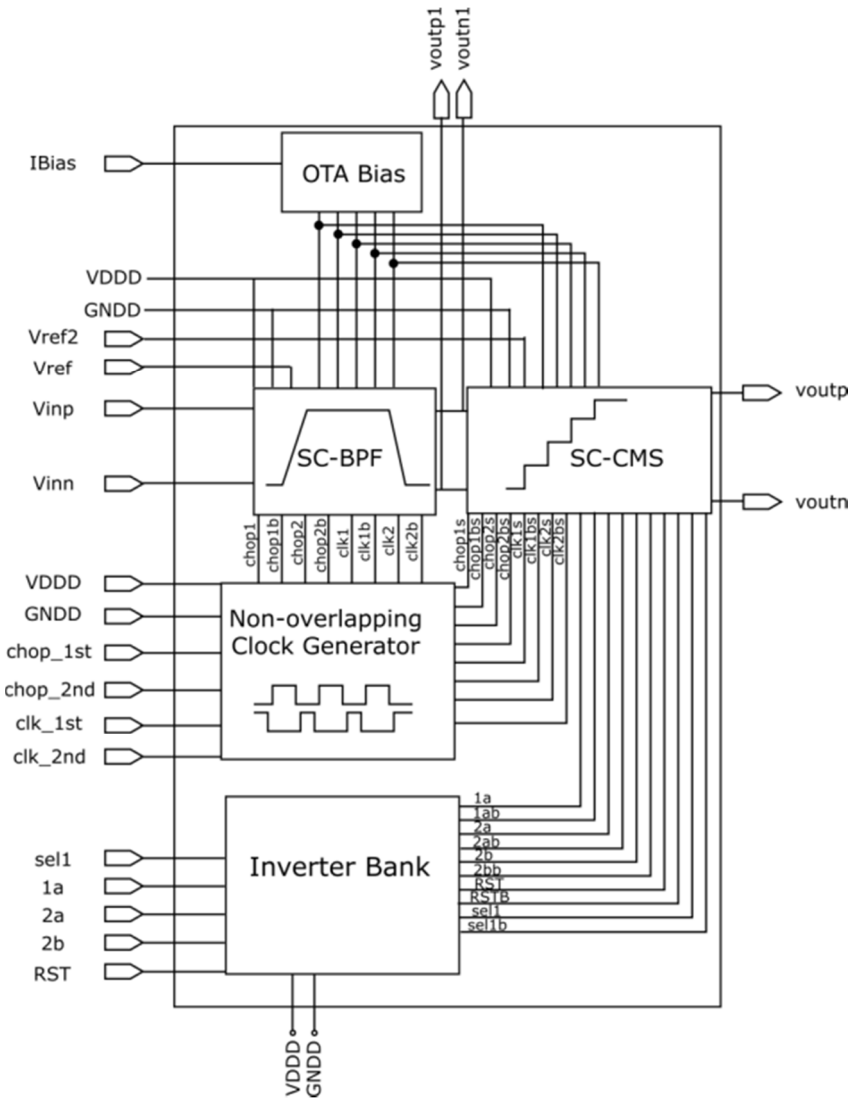

Figure 6-23: Test bench for the measurement and debugging of single pixel and 8 x 6 THz array

6.8 THz CHARACTERIZATION

For the THz characterization, a test setup comprising a polymer Zeonex lens was used in order to collimate and refocus the THz beam on the imaging array. The measurements were focused on a single representative pixel of the imager and followed the methodology as described earlier in Chapter 3 to obtain the main performance parameters. The single channel works fine but due to some bad signal distribution, the array suffers from malfunctioning that prevents the use of CMS which is instead used only as a sample and hold circuit to output the signal.

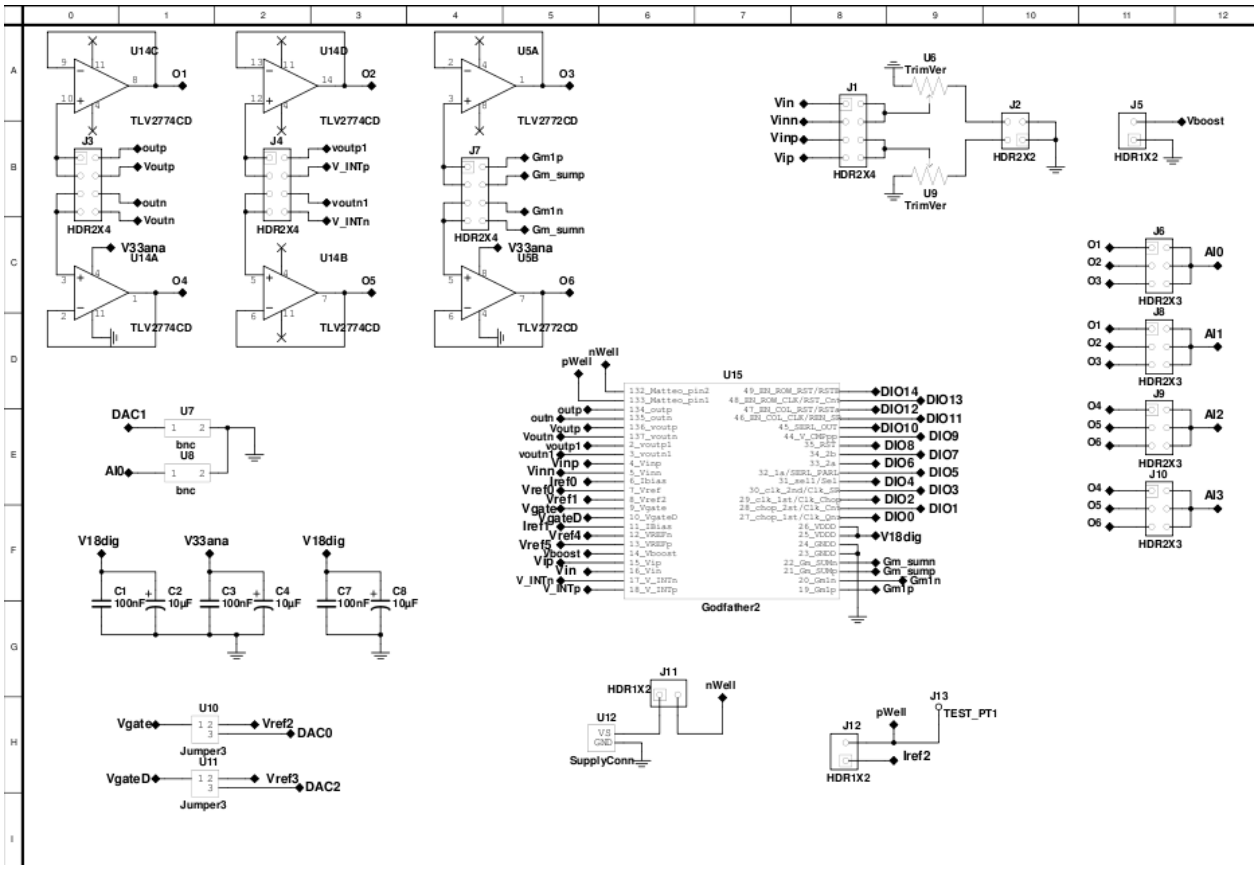

Figure 6-24: Designed daughter board

Figure 6-25 shows the behavior of 5 selected pixels of the sensor and how their output varies for different combinations of bias voltages of the FET detectors V_{Active} and V_{Dummy} (referred to as ΔV). This non-uniformity is found out to be the main challenge for the characterization of the imager, since most of the pixels have different response.

Figure 6-26 shows the pixels non-uniformity. The distribution plots of various pixels response as a function of bias voltage was plotted in order to find the number of pixels in a particular configuration. For several values of V_{Active} and different of ΔV (i.e. V_{Dummy}) a graph was plotted to see how many pixels fall in a particular configuration. As evident from the plots, there are at least 10 pixels sharing similar voltage configuration for every condition.

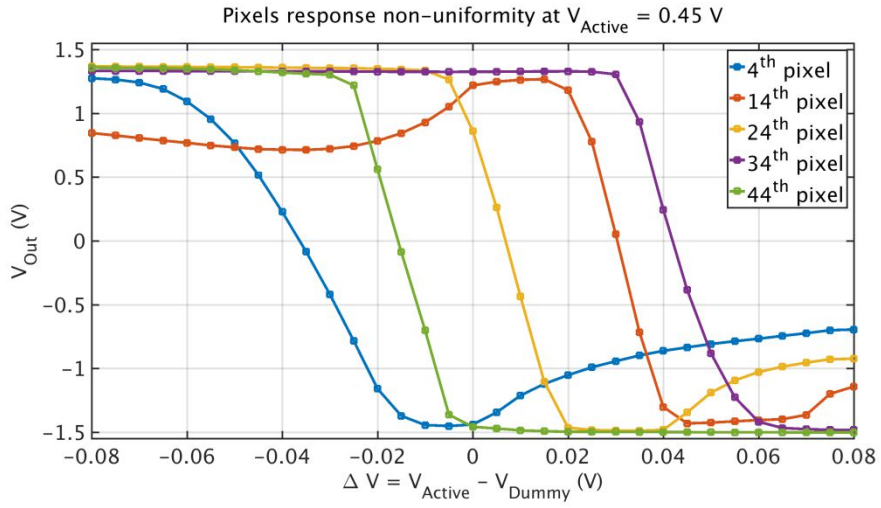

Figure 6-25: Non-uniformity of different pixel response vs. gate bias difference

Figure 6-27 shows the voltage responsivity as a function of FET bias voltage at 325 GHz signal frequency and 0.5 Hz THz source modulation. A single imager frame can be acquired and readout in 3.08 ms, thus allowing the measurement and averaging of 324 frames during the 1s modulation semi-period. Then, the subtraction of the two semi-period readings, with and without THz signal, leads to the THz measurement at 0.5 Hz final rate. A responsivity peak of 37.5 kV/W at 0.47V is

achieved. Since the responsivity of the single antenna-coupled FET detector is measured to be around 150 V/W as published in [98], the total gain of the readout interface is approximately 250 V/V or 48 dB. This result is obtained with the high gain setting, without the functioning of the CMS stage. Infact, the second stage is used only to sample, so theoretically the gain should be 31x5. Figure 6-28 shows the pixel frequency response. Figure 6-29 shows the NEP as a function of FET bias voltage. The values obtained for the NEP are integrated over 0.5 Hz bandwidth, which is the modulation frequency used to chop the signal. The minimum integrated NEP of 3.2 nW was found at 0.4 V FET bias

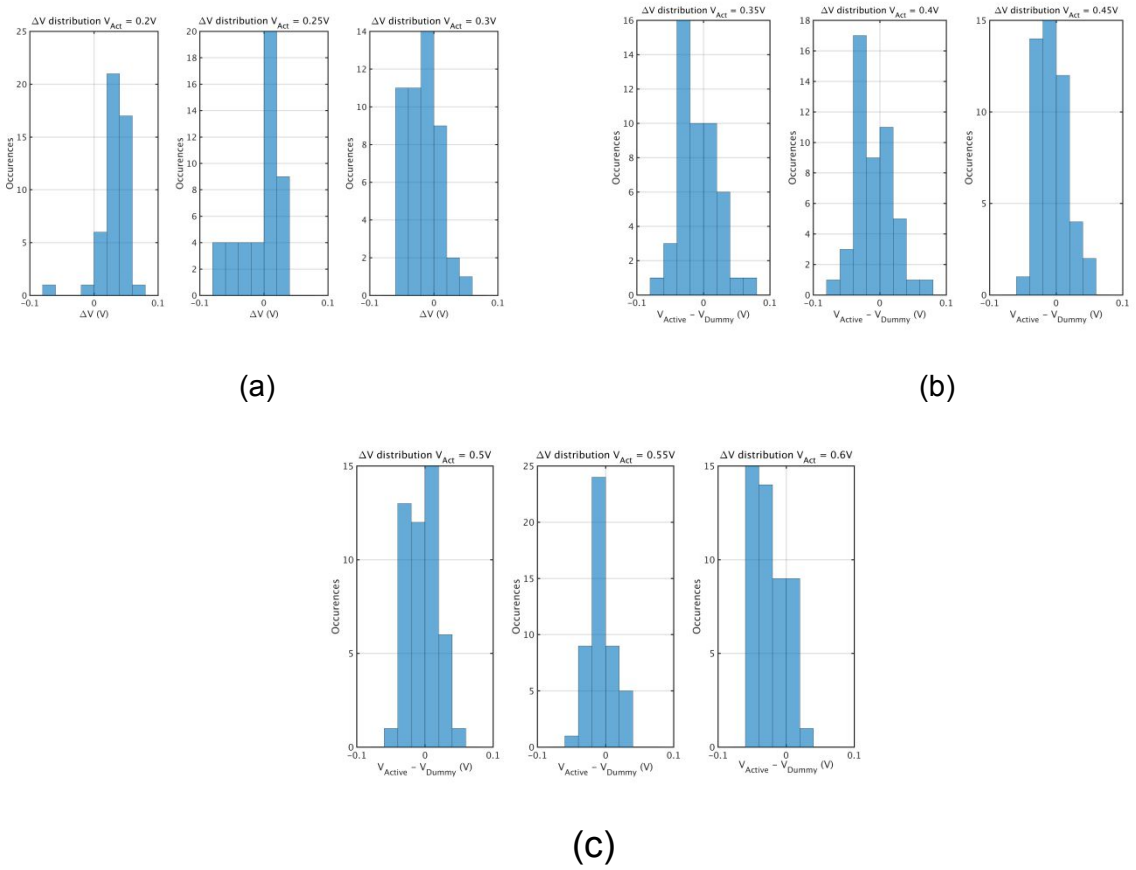

Figure 6-26: Distribution plots of various pixels as a function of bias voltage

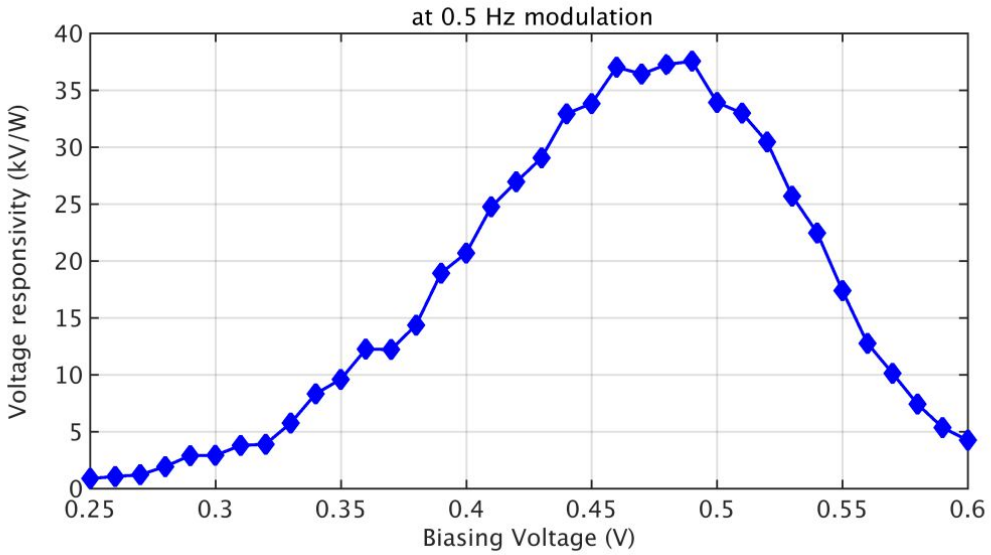

Figure 6-27: Voltage responsivity vs. FET gate bias at 325 GHz signal frequency

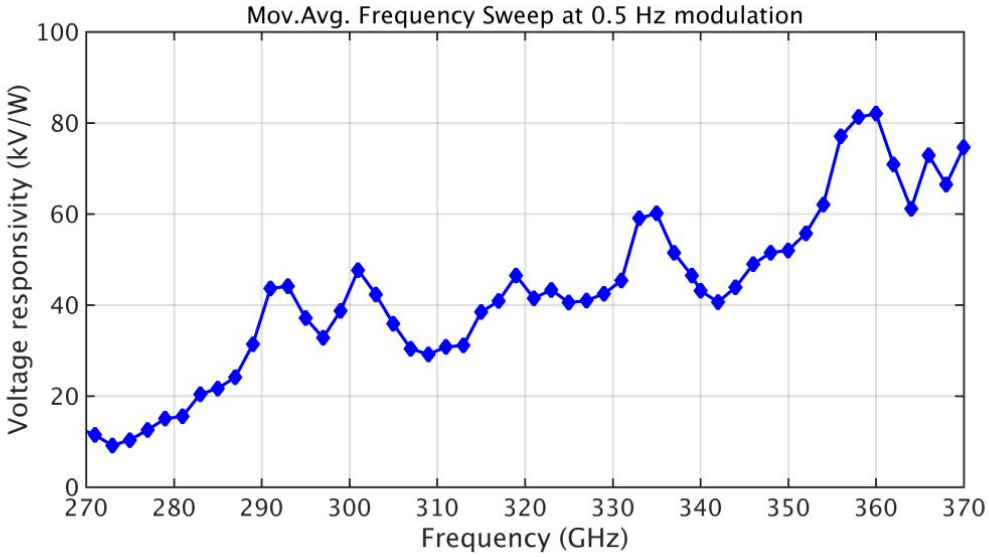

Figure 6-28: Pixel voltage responsivity vs. THz signal frequency at 0.45V bias

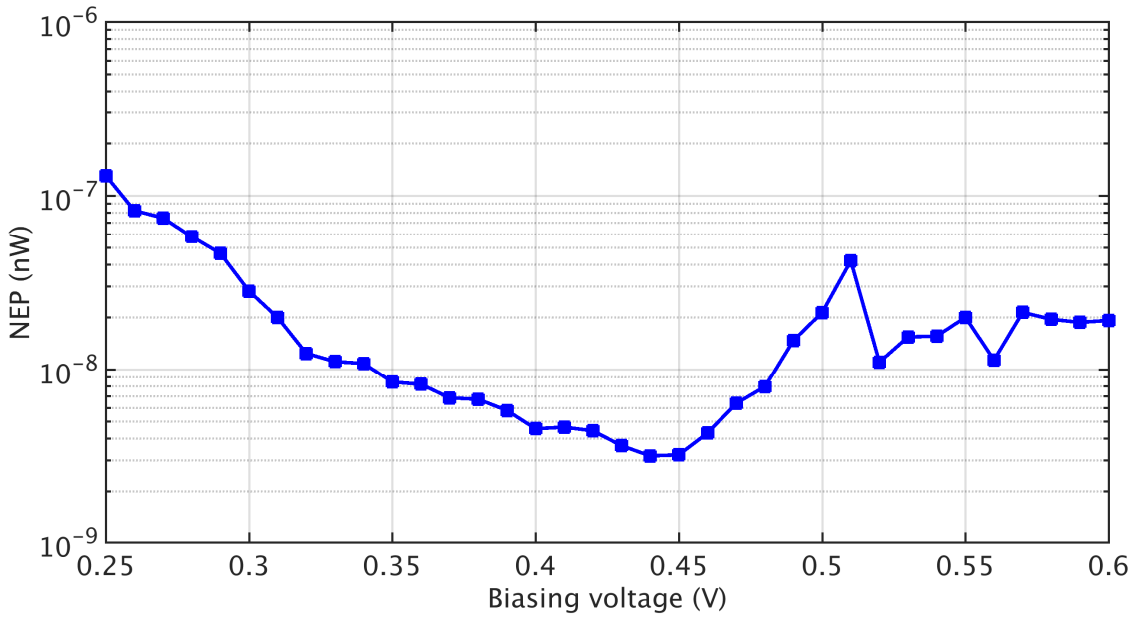

Figure 6-29: Pixel NEP vs. FET gate bias at 325 GHz signal frequency

Finally, by scanning the detector on the plane of focus through an electrically controlled positioning system, multiple frames were acquired and joined together in a post-processing analysis. In this way, an equivalent 24x18 image was acquired in the same experimental condition and processed with a 3x3 median filter. The result is shown in Figure 6-30 demonstrating the THz imaging.

6.9 CHAPTER SUMMARY

This chapter explains the design details and characterization and measurement results of FET based direct THz detector pixel and an 8 x 6 THz imaging array. The pixel was designed with an intention to decrease the occupied area as compared to the one presented in Chapter 5. Thanks to the in-pixel filtering provided by the BPF and a noise removal mechanism implemented using CMS, the pixel is able to achieve a voltage responsivity of 38 kV/W, confirming 250 V/V gain of the readout interface. Moreover, an image of the THz spot was obtained by acquiring multiple frames and joined together in a post-processing analysis.

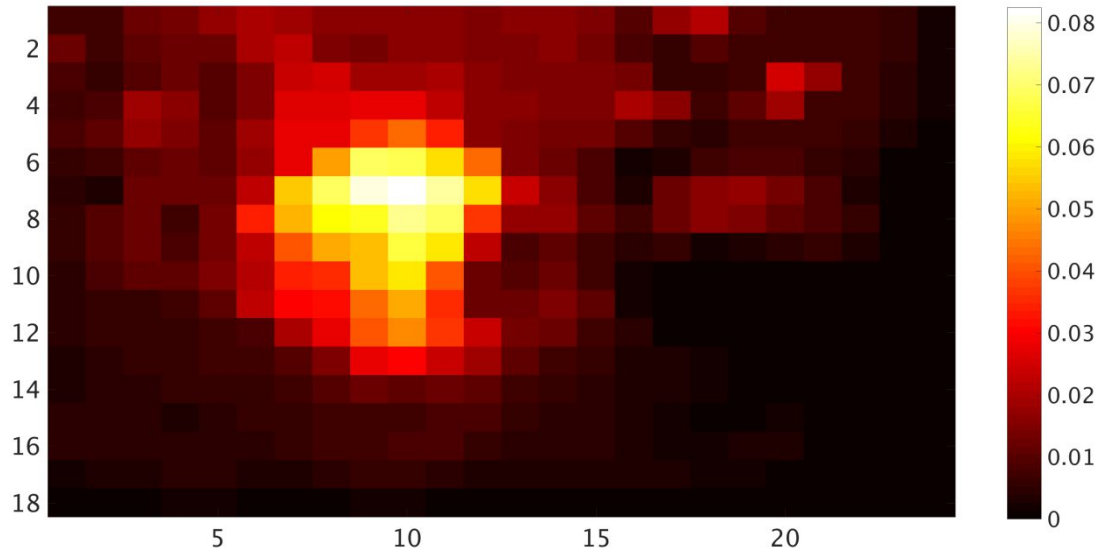

Figure 6-30: Stitching of 3x3 images of the THz spot produced by the source

CHAPTER 7: CONCLUSION AND FUTURE PROSPECTS

This thesis presents the investigation, design, implementation and characterization of room temperature THz systems to be used for imaging applications. These systems are fabricated in low cost Si technologies which can potentially be used to develop THz devices and systems for commercial applications. The FET-based direct THz detectors are readily available in standard processes and provide design freedom for performance optimization. They can be configured differently, based on the way THz radiations are coupled to these detectors, and were in fact characterized and evaluated as a part of this thesis work.

The problems involved in the measurement and characterization of direct THz detector were also addressed. A design methodology involving the use of a reference device for the characterization of direct THz detectors is presented and as an example FET detectors fabricated in 0.18µm technology are characterized. The results obtained as a result of this characterization procedure were found out to be in close agreement with some other methods, thus proving the validity of this approach.

The final objective of the thesis was concerned with designing THz imaging array. This was sub-divided into two parts: First part dealt with the design of an effective readout interface for the signal processing of the detected signal such that the detector NEP is preserved. Moreover due to the operational limitation of the available THz source, there was a requirement that the interface must be able to work with source modulation frequency of less than 1 kHz. High voltage responsivity and low NEP values were also desired. A cascade of switched-capacitor filters with a measured gain value of 70 dB and an input referred noise of less than 2.15μV_{RMS} provided an overall voltage responsivity of 470 kV/W and NEP of 480 pW/sqrt (Hz) at a signal frequency of 370 GHz. The pixel area (500µm x 750µm) was large as compared to some other architectures but the pixel was able to operate with a source modulation frequency range of 0.1Hz-1 kHz. Based on this successful implementation, in the next step an 8x6 THz imaging array was designed after doing some modifications of the pixel interface in order to reduce power and area. THz

characterization results showed a strong non-uniformity among various pixels which proved to be challenging to properly operate the array as different pixels had different responses. Moreover, due to some issues, the 2nd stage of the readout interface could not function properly. Nevertheless, an image of the THz spot was successfully obtained by acquiring multiple frames and doing post-processing afterwards.

With regard to the imaging array described in Chapter 06, there are some issues that need to be addressed in future. First off, the size of the pixel can be further reduced as with current dimensions of 455µm x 455µm, it is on the larger side as compared to the state-of-the-art. Reducing pixel size will also help in the creation of a larger imaging array. Moreover, the noise performance of the readout interface needs to be improved as in the current architecture it is deteriorated due to the non-functional 2nd stage (CMS) which is only used as a sample and hold circuit instead. Essentially, only the 1st stage (SC-BPF) is doing filtering and amplification of the detected signal which is not enough to attain high SNR. The problem might have occurred because of some layout issues or routing of metal wires. Nevertheless, it is indeed satisfying to acquire a real-time image of an object using this architecture which can provide a good foundation stone to further FBK research in this field in order to improve results.

The crux of the thesis is that the THz systems are capable of making inroads in various commercial applications in the near future [111]. However, affordable THz sources with high power still remain the main obstacle in order to realize a monolithic solution but that will eventually be overcome with innovative ideas and smart design techniques.

APPENDIX A: OTA DESIGN USING G_M/I_D METHODOLOGY

This appendix deals with the design of the OTA and its biasing circuitry using g_m/i_d design methodology. First the design methodology is presented and then the DC analysis of the bias circuitry of the folded cascode OTA design is discussed.

A.1 DESIGNING THE AMPLIFIER USING G_M/I_D METHODOLOGY

The traditional square law modelling used to size the long channel devices fails to give reliable results in submicron devices. In such cases the g_m/i_d design approach provides an alternative solution to optimally design circuits. This approach divides the device operative space into three, clearly distinguishable regions based on the **I**nversion **C**oefficient (IC) [102] [112] [99] [103]. IC is a function of drain current (I_D), specific current (I_S), the aspect ratio (W/L) and can be written as:

$$\mathrm{IC} = \frac{I_D}{I_S} \tag{A-1}$$

And the specific current I_S is given by:

$$I_S = 2\eta C_{Ox} {V_T}^2 \mu \left(\frac{W}{L}\right) \tag{A-2}$$

where 'C_{OX}' the gate oxide capacitance, 'V_T' is the thermal voltage and 'μ' is the low field mobility.

Figure A-1 shows the graph between the transconductance efficiency (g_m/i_d) and IC and how the device **R**egions-**O**f-**O**peration (ROC) is divided into 3 different parts based on the value of IC.

- Strong inversion (IC>>1)
- Weak inversion (IC<<1)
- Moderate inversion (1<IC<10)

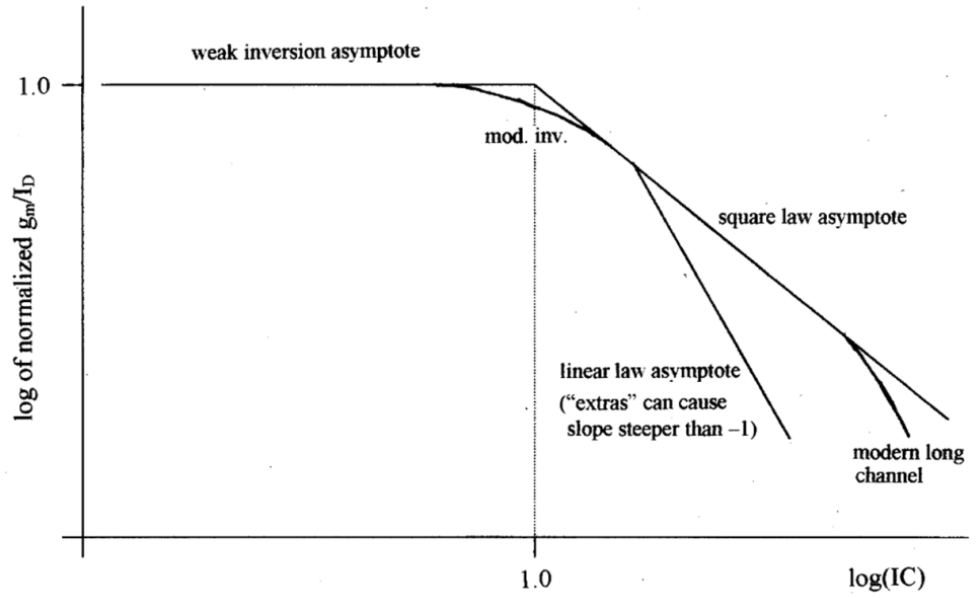

Figure A-1: Transconductance efficiency vs. Inversion coefficient [103]

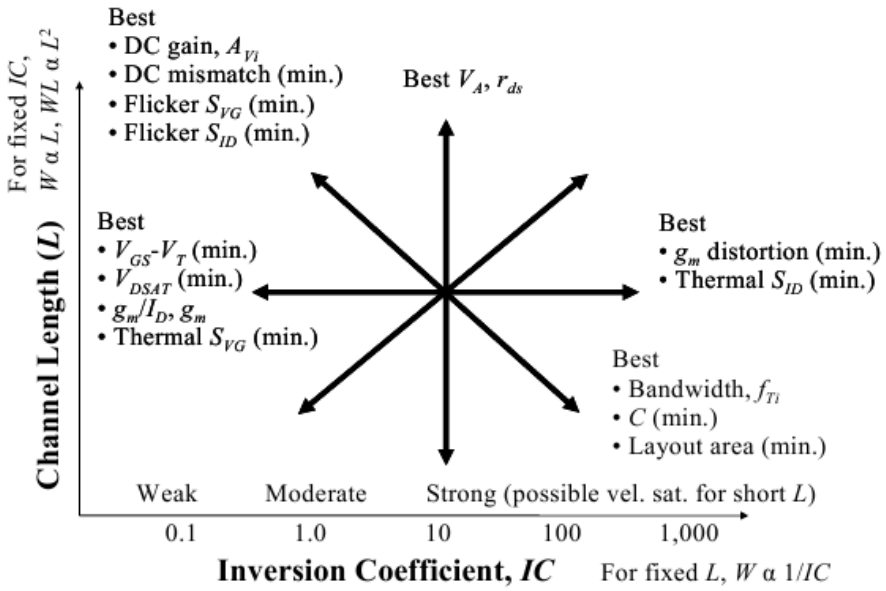

Figure A-2: Operating space of the device with respect to channel length and IC [102]

Figure A-2 shows the operating space of the device with respect to channel length and IC and the merits/demerits of operating the device in every region. To summarize, operating in weak inversion at large L helps in increasing the DC gain and minimizing flicker noise [104] [113] [114]. On the contrary if speed and area are important, the device can be operated in strong inversion with small L. Multiple graphs are generated for the NMOS and PMOS devices characterizing the technology as shown in Figure A-3 and Figure A-4. These include device intrinsic gain, speed and sizing as a function of its transconductance efficiency 'g_m/i_d' and overdrive voltage 'V_{OV}' [115].

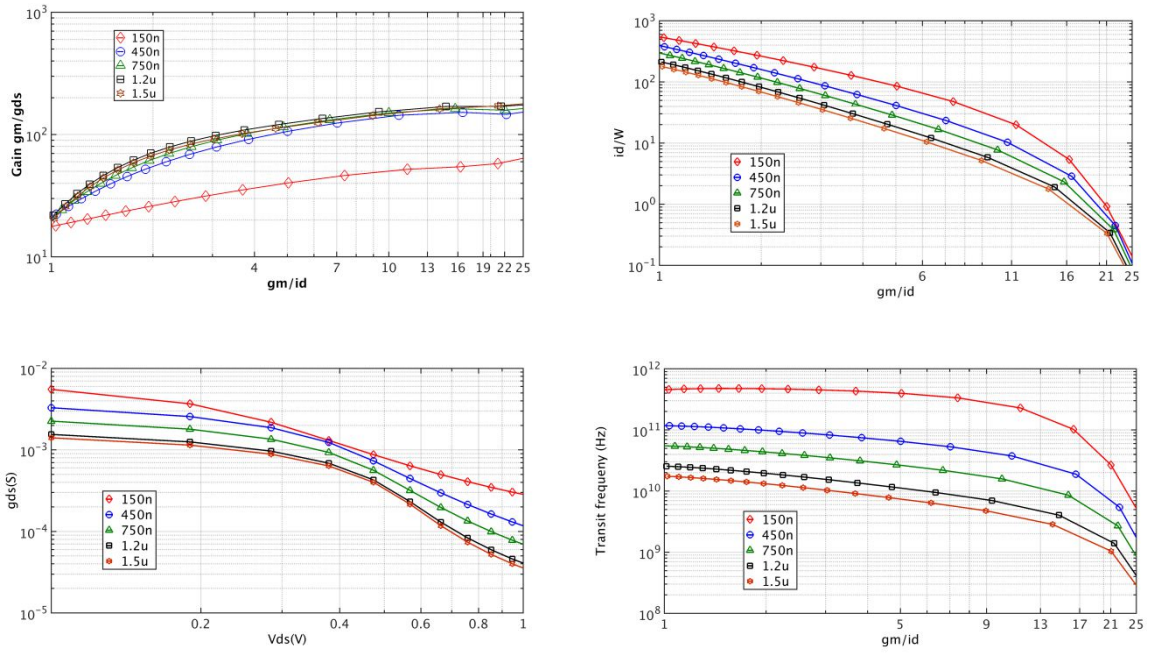

Figure A-3: Simulated parameters of NMOS transistors for g_m/i_d design at different channel length L

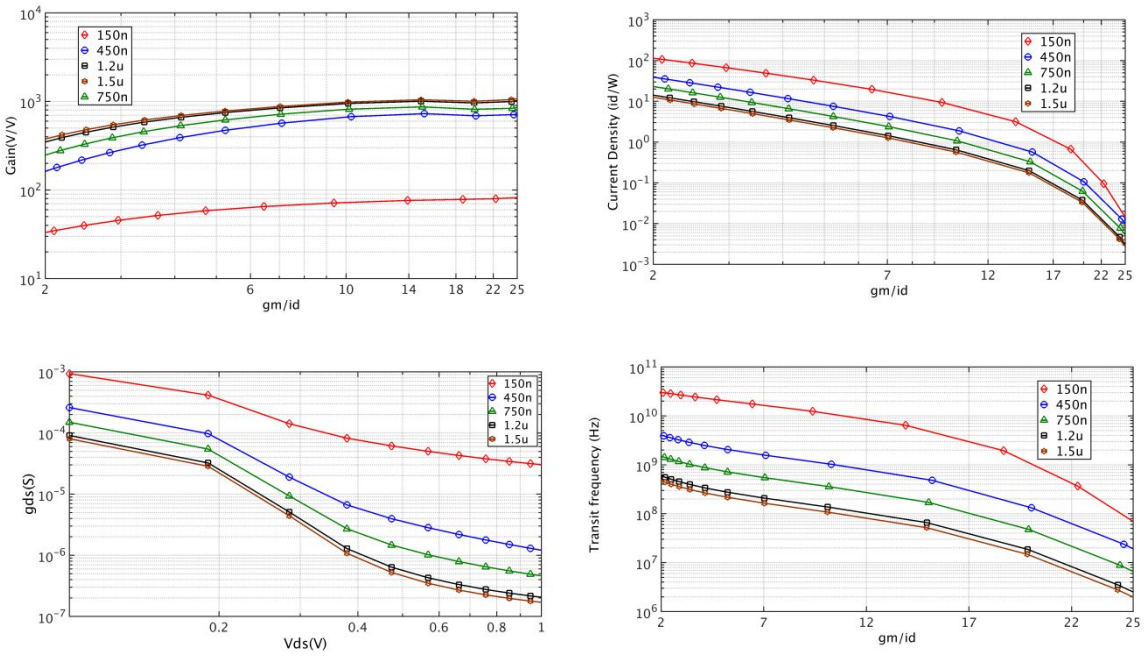

Figure A-4: Simulated parameters of PMOS transistors for g_m/i_d design at different channel length L

A.2 DC ANALYSIS OF THE FOLDED CASCODE OTA

The DC analysis of the folded cascode OTA is performed by applying Kirchhoff Voltage Law (KVL) to determine the required bias voltages of each device. Starting with determining Bias A as shown in Figure A-5:

$$-BiasA + V_{GS,TAIL} = 0$$

$$\left(V_{GS,TAIL} - V_{th,n}\right) + V_{th,n} = BiasA$$

$$BiasA = \left(V_{OV,TAIL}\right) + V_{th,n} \qquad \text{(A-3)}$$

Similarly,

$$-BiasD + V_{GS,M7} + V_{OV,M9} + 50mV = 0$$

$$(V_{GS,M7} - V_{th,n}) + V_{th,n} + V_{OV,M9} + 50mV = BiasD$$

$$BiasD = V_{OV,M7} + V_{th,n} + V_{OV,M9} + 50mV \quad \text{(A-4)}$$

Additional voltage headroom of 50mV is added to calculate BiasD in order to ensure that M7-M8 is properly biased in the saturation region. Applying the same procedure to determine the bias voltages of the PMOS cascode and current source devices, we obtain:

$$-VDDA + |V_{GS,M3}| + BiasB = 0$$

$$BiasB = VDDA - |V_{GS,M3}| + |V_{th,p}| - |V_{th,p}|$$

$$BiasB = VDDA - |V_{OV,M3}| - |V_{th,p}| \quad \text{(A-5)}$$

And

$$BiasC = VDDA - |V_{OV,M3}| - |V_{OV,M5}| - |V_{th,p}| - 50mV \quad \text{(A-6)}$$

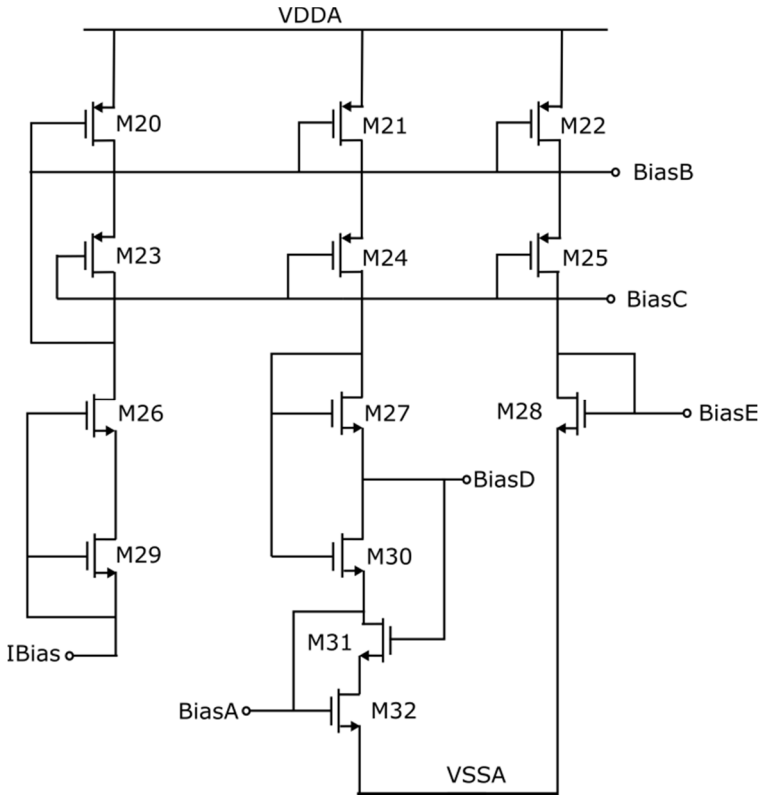

Figure A-5: OTA biasing circuitry

APPENDIX B: FILTER DESIGN

The readout interface for the FET based THz detector consists of a cascade of SC filters. In the following sections, the design details of these filters are discussed.

B.1 HIGH PASS FILTER

Figure 5-8 shows the Continuous Time (CT) HPF with C_1 and C_3 being the sampling and feedback capacitors respectively while R_F represents the feedback resistance. The Signal Transfer Function (STF) of this filter is:

$$H_{HPF}(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{sC_1}{sC_3 + G_F} == \frac{sC_1R_F}{sC_3R_F + 1} \quad \text{(B-1)}$$

Where DC gain is:

$$DC\ Gain = |H_{HPF}(0)| = \frac{C_1}{C_2} \quad \text{(B-2)}$$

And the cut-of frequency is:

$$f_{p,HPF} = \frac{1}{2\pi R_F C_F} \quad \text{(B-3)}$$

The value of sampling capacitor C_1 is determined from the noise analysis of Section 5.3 and is fixed at 5 pF and the voltage gain of 20 V/V is required in the 1st stage. These specifications lead to a feedback capacitor C_3 of 0.25pF as per equation (B-2). Moreover the cut-off frequency of SC-HPF is set to 30 kHz and the sampling frequency is 200 kHz. Thus, the required value of feedback resistor R_F is determined from equation (B-3). R_F can be converted into a SC configuration [99]:

$$R_F = \frac{1}{f_{clk}C_{F2}} \quad \text{(B-4)}$$

Leading to C_2 value of 0.25 pF

B.2 LOW PASS FILTER (LPF) DESIGN

The CT-LPF is shown in Figure B-1 with R_{IN} and R_F as the input and feedback resistances, respectively.

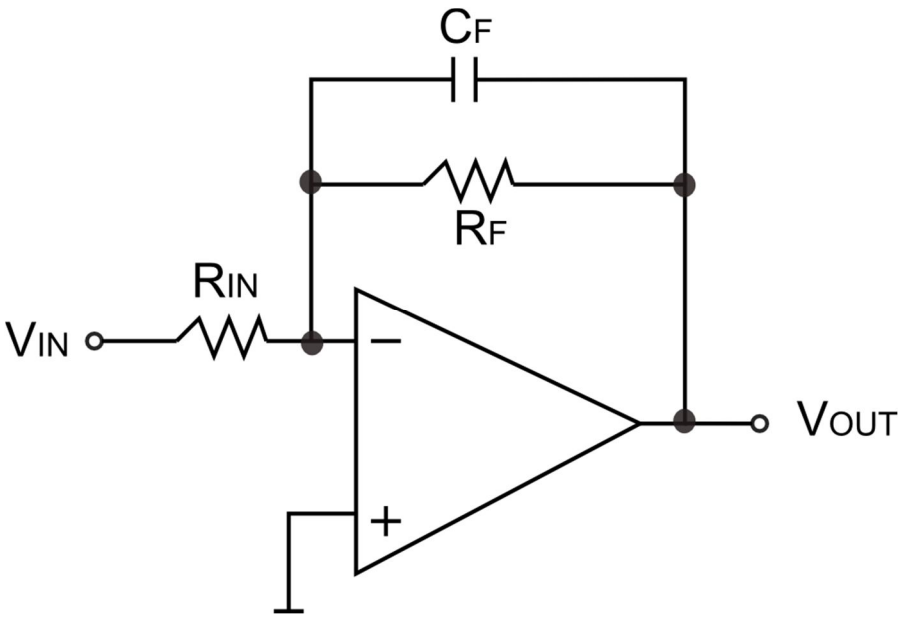

Figure B-1: CT-LPF prototype

DC gain is:

$$DC\ Gain(LPF) = |H_{LPF}(0)| = \frac{R_F}{R_{in}} \qquad \text{(B-5)}$$

And the pole frequency is given by equation (B-3). The LPF is designed to achieve a DC gain of 16 V/V with a cut-off frequency of 70 kHz. Based on these specifications, capacitor values are determined and listed in Table 5-1. By using the same methodology the final stage of the readout interface comprising of the SC-LPF is designed to achieve a DC gain of 12 with a bandwidth of 1 kHz.

APPENDIX C: SYSTEM LEVEL SIMULATIONS

This appendix presents the MATLAB code that was used to carry out simulations in order to see the proper functioning of the readout interface described in Chapter 05 and to extract the system level, design related parameters. The same code can also be used with

C.1 MATLAB CODE

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% General Specifications
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

N=2^16;               % No of FFT points
Asig=15e-6;           % DC signal with amplitude
Aq=1;                 % Amplitude of chopping wave.
Fsig=0.2e3;           % Signal Frequency (Essentially a DC signal)

Fch=50e3;             % Chopping frequency of 5 kHz.
Fs=0.2e6;             % Sampling Frequency
offset=1e-3;          % Assumed offset value.
Vn_rms=5e-6;          % RMS value of the total input reffered noise voltage

Ts=1/Fs;              % Sampling time period.
NBW=1e3*pi*0.5;       % Noise Bandwidth (systemBW*pi/2)
Ut=26e-3;             % Thermal Voltage
qe=1.6e-19;           % Electron charge

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Specifications for 1st stage (SC-HPF)
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

A1=10;                  % Gain of the 1st stage (HPF)
n1=1;                        % Order of the 1st stage (HPF)
f1=30e3;                % Cut off frequency of the 1st stage (HPF)
w1=2*pi*f1;             % Angular Frequency of the 1st stage (HPF)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Specifications for 2nd stage5 (SC-LPF)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

A2=20;                  % Gain of the 2nd stage (LPF)
n2=1;                        % Order of the 2nd stage (LPF)
f2=70e3;                % Cut off frequency of the 2nd stage (LPF)
w2=2*pi*f2;             % Angular Frequency of the 2nd stage (LPF)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Specifications for 3rd stage (SC-LPF)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

A3=5;                        % Gain of the 3rd stage (LPF)
n3=1;                        % Order of the 3rd stage (LPF)
f3=1e3;                 % Cut off frequency of the 3rd stage (LPF)
w3=2*pi*f3;             % Angular frequency of the 3rd stage (LPF)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
index = linspace(0, N-1, N) ;    % Generating Time Sequence
t=Ts*index;
f = Fs/2*linspace(0,1,N/2+1);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating Sine, Square and Modulating Signal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
SineWave = SineWaveGenerator(N, Asig, Fs, Fsig);
SquareWave=SquareWaveGenerator(N,Aq,Fs,Fch);
modulatedoutput=SineWave.*SquareWave;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating White and flicker Noise, offset of a specific noise voltage
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 % noise_psd=Vn_rms^2;
 % x=sqrt(12*Fs/(2*NBW)*noise_psd);
 % wn=-x/2+x*rand(1,N);
wn=randn(1,N)*Vn_rms;                          % Generating Random White Noise Signal
flicker=pinknoise(N);
totalnoise=flicker+wn;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating Modulating Signal & LPF
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Output_one = HighPass(n1, w1, modulatedoutput,t);
gain_Output_one = A1*Output_one;
filtered_noise = Noisefilter(totalnoise,t);
%filtered_noise = 0;
sum_output=filtered_noise + gain_Output_one;
%sum_output=filtered_noise;
%sum_output= gain_Output_one;
Output_two = LowPass(n2, w2,sum_output,t);
gain_Output_two = A2*Output_two;
Demodulatorout = gain_Output_two.*transpose (SquareWave);
```

```
FinalLPout = LowPass(n3, w3,Demodulatorout,t);

gainFinalLPout =A3*FinalLPout;
```

%%%

% Generating time domain waveform and PSD of the Sine Wave

%%%

```
h = spectrum.periodogram('hamming');                    % Creating a periodogram spectrum object

hopts = msspectrumopts(h,SineWave);                     % Plotting the Mean Square power spectrum of the signal 'SineWave'

set(hopts,'Fs',Fs,'SpectrumType','onesided','centerdc',true);

figure(1)

subplot(3,1,1)

msspectrum(h,SineWave,hopts);

title('Mean Square Spectrum of Sine Wave at 500Hz Frequency');

set(gcf, 'Color', [1 1 1])

hpsd = psd(h,SineWave,hopts);                           % Calling the 'psd' on the spectrum object 'h' defined above

subplot(3,1,2)

plot(hpsd);

set(gcf, 'Color', [1 1 1])

subplot(3,1,3)

plot(t,SineWave,'r');

Sine_power=avgpower(hpsd)                               % Calling average power 'avgpower' on the power spectrum density data 'hpsd'
```

%%%

% Generating time domain waveform and PSD of Square Wave Signal

%%%

```
h = spectrum.periodogram('hamming');                    % Creating a periodogram spectrum object

hopts = msspectrumopts(h,SquareWave);                   % Plotting the Mean Square power spectrum of the signal 'SquareWave'
```

```
set(hopts,'Fs',Fs,'SpectrumType','twosided','centerdc',true);
figure (2)
subplot (3,1,1)
msspectrum(h,SquareWave,hopts);
title ('Mean Square Spectrum of Square Wave Signal at 25kHz Chopping Frequency');
%v = axis; axis ([v(1) v(2) 0 7]); % Zoom in Y
set (gcf, 'Color', [1 1 1])
```

% Calculating the power of the 'SineWave' by integrating the area under the

% PSD curve.

```
hpsd = psd(h,SquareWave,hopts);          % calling the 'psd' on the spectrum object 'h' defined above
subplot (3,1,2)
plot (hpsd);
set (gcf, 'Color', [1 1 1])
subplot (3,1,3)
plot (t,SquareWave,'r');
Square_power=avgpower (hpsd)          % Calling average power 'avgpower' on the power spectrum density data 'hpsd'
```

%%%

% Generating time domain waveform and PSD of Modulated Signal

%%%

```
hopts = msspectrumopts(h,modulatedoutput);
set(hopts,'Fs',Fs,'SpectrumType','twosided','centerdc',true);
figure (3)
subplot (3,1,1)
msspectrum(h,modulatedoutput,hopts);
title ('Mean Square Spectrum of Modulated Signal');
set (gcf, 'Color', [1 1 1])
hpsd = psd(h,modulatedoutput,hopts);
```

```
subplot (3,1,2)
plot (hpsd);
set (gcf, 'Color', [1 1 1])
subplot(3,1,3)
plot(t,modulatedoutput,'r');
modulated_power=avgpower(hpsd)
```

%%

% Generating time domain waveform and PSD of Total Noise (offset+flicker+Thermal)

%%

```
hopts = msspectrumopts(h,totalnoise);
set(hopts,'Fs',Fs,'SpectrumType','twosided','centerdc',true);
figure(4)
subplot(3,1,1)
msspectrum(h,totalnoise,hopts);
title('Mean Square Spectrum of Noise (flicker+thermal+offset)');
set(gcf, 'Color', [1 1 1])
hpsd = psd(h,totalnoise,hopts);
subplot(3,1,2)
plot(hpsd);
set(gcf, 'Color', [1 1 1])
subplot(3,1,3)
plot(t,totalnoise,'r');
noise_power=avgpower(hpsd,[0.1 125e3])
```

%%

% Generating time domain waveform and PSD of 1st-stage output signal

%%

```
hopts = msspectrumopts(h,gain_Output_one);
set(hopts,'Fs',Fs,'SpectrumType','twosided','centerdc',true);
```

```
figure(5)
subplot(3,1,1)
msspectrum(h,gain_Output_one,hopts);
title('Mean Square Spectrum of 1st stage Output');
set(gcf, 'Color', [1 1 1])
hpsd = psd(h,gain_Output_one,hopts);
subplot(3,1,2)
plot(hpsd);
set(gcf, 'Color', [1 1 1])
subplot(3,1,3)
plot(t,gain_Output_one,'r');
first_power=avgpower(hpsd)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating time domain waveform and PSD of 2nd-stage output signal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
hopts = msspectrumopts(h,filtered_noise);
set(hopts,'Fs',Fs,'SpectrumType','twosided','centerdc',true);
figure(6)
subplot(3,1,1)
msspectrum(h,filtered_noise,hopts);
title('Mean Square Spectrum of filtered_noise');
set(gcf, 'Color', [1 1 1])
hpsd = psd(h,filtered_noise,hopts);
subplot(3,1,2)
plot(hpsd);
set(gcf, 'Color', [1 1 1])
subplot(3,1,3)
plot(t,filtered_noise,'r');
```

```
filtered_power=avgpower(hpsd)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating time domain waveform and PSD of 3rd-stage output signal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
hopts = msspectrumopts(h,sum_output);
set(hopts,'Fs',Fs,'SpectrumType','twosided','centerdc',true);
figure(7)
subplot(3,1,1)
msspectrum(h,sum_output,hopts);
title('Mean Square Spectrum of filtered noise+1st stage output');
set(gcf, 'Color', [1 1 1])
hpsd = psd(h,sum_output,hopts);
subplot(3,1,2)
plot(hpsd);
set(gcf, 'Color', [1 1 1])
subplot(3,1,3)
plot(t,sum_output,'r');
amplifiedfiltered_power=avgpower(hpsd)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating time domain waveform and PSD of demodulator signal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
hopts = msspectrumopts(h,gain_Output_two);
set(hopts,'Fs',Fs,'SpectrumType','twosided','centerdc',true);
figure(8)
subplot(3,1,1)
msspectrum(h,gain_Output_two,hopts);
title('Mean Square Spectrum of 2nd stage Output');
set(gcf, 'Color', [1 1 1])
```

```
hpsd = psd(h,gain_Output_two,hopts);
subplot(3,1,2)
plot(hpsd);
set(gcf, 'Color', [1 1 1])
subplot(3,1,3)
plot(t,gain_Output_two,'r');
second_stageoutput_power=avgpower(hpsd)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating time domain waveform and PSD of the final output signal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
hopts = msspectrumopts(h,Demodulatorout);
set(hopts,'Fs',Fs,'SpectrumType','twosided','centerdc',true);
figure(9)
subplot(3,1,1)
msspectrum(h,Demodulatorout,hopts);
title('Mean Square Spectrum of Demodulator Output');
set(gcf, 'Color', [1 1 1])
hpsd = psd(h,Demodulatorout,hopts);
subplot(3,1,2)
plot(hpsd);
set(gcf, 'Color', [1 1 1])
subplot(3,1,3)
plot(t,Demodulatorout,'r');
demodulator_power=avgpower(hpsd)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
hopts = msspectrumopts(h,gainFinalLPout);
set(hopts,'Fs',Fs,'SpectrumType','onesided','centerdc',true);
figure(10)
```

```
subplot(3,1,1)
msspectrum(h,gainFinalLPout,hopts);
title('Mean Square Spectrum of Final output');
set(gcf, 'Color', [1 1 1])
hpsd = psd(h,gainFinalLPout,hopts);
subplot(3,1,2)
plot(hpsd);
set(gcf, 'Color', [1 1 1])
subplot(3,1,3)
plot(t,gainFinalLPout,'r');
final_power=avgpower(hpsd,[0 NBW])
```

C.2 SIMULATION

Simulations start with plotting transient waveform and PSD plot of a sinusoidal signal with an amplitude A_{sig} and 200 Hz frequency to the interface as shown in Figure C-1. A square waveform of 50 kHz frequency for modulator/demodulator is also plotted in Figure C-2.

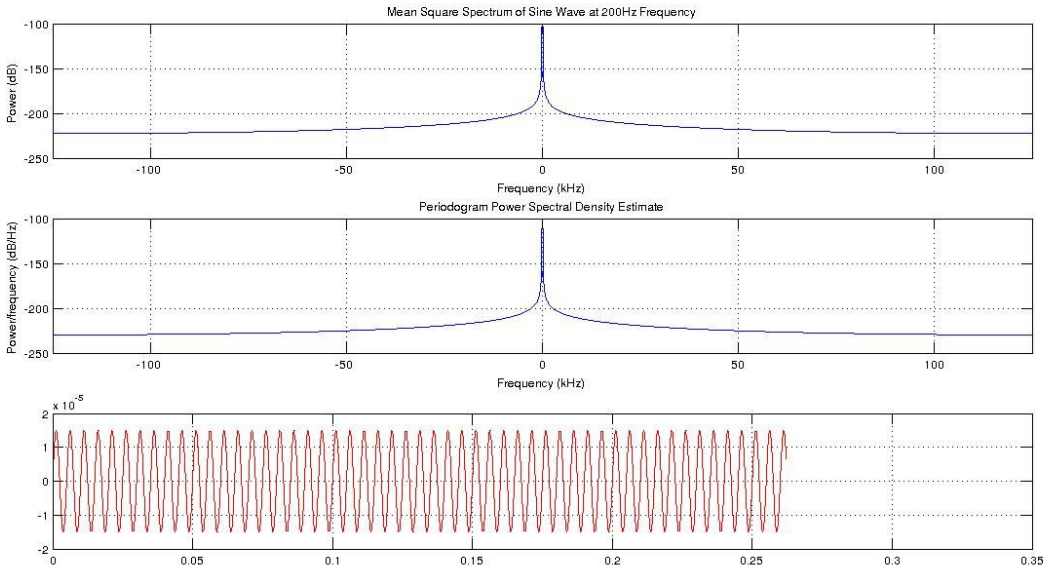

Figure C-1: Simulated plot of input sinusoidal waveform

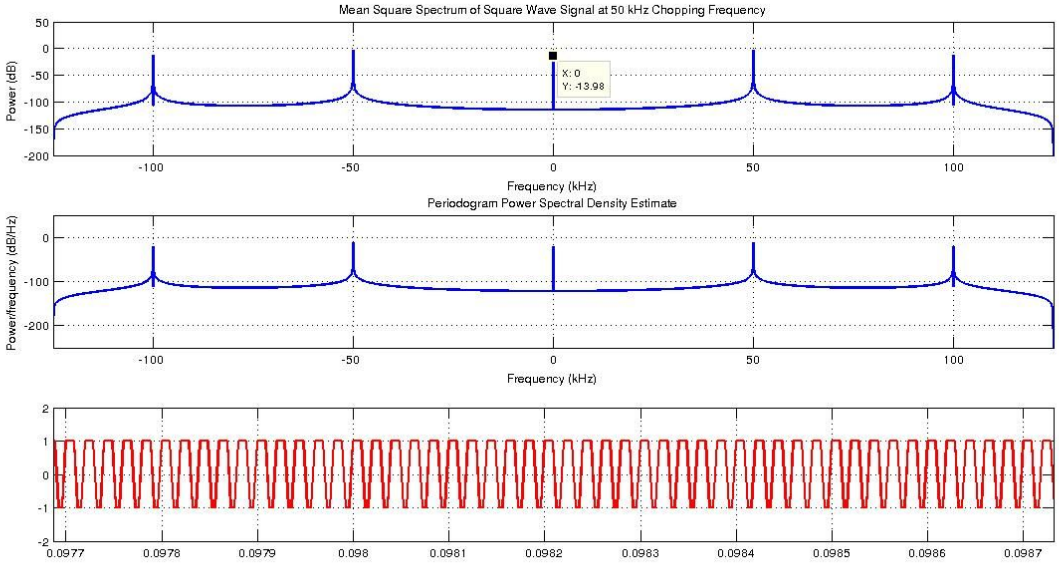

Figure C-2: Simulated plot of square waveform

In Figure C-3, the noise PSD plot at the input of the filter is shown. This noise consists of random white thermal noise and flicker noise dominant at low frequency values.

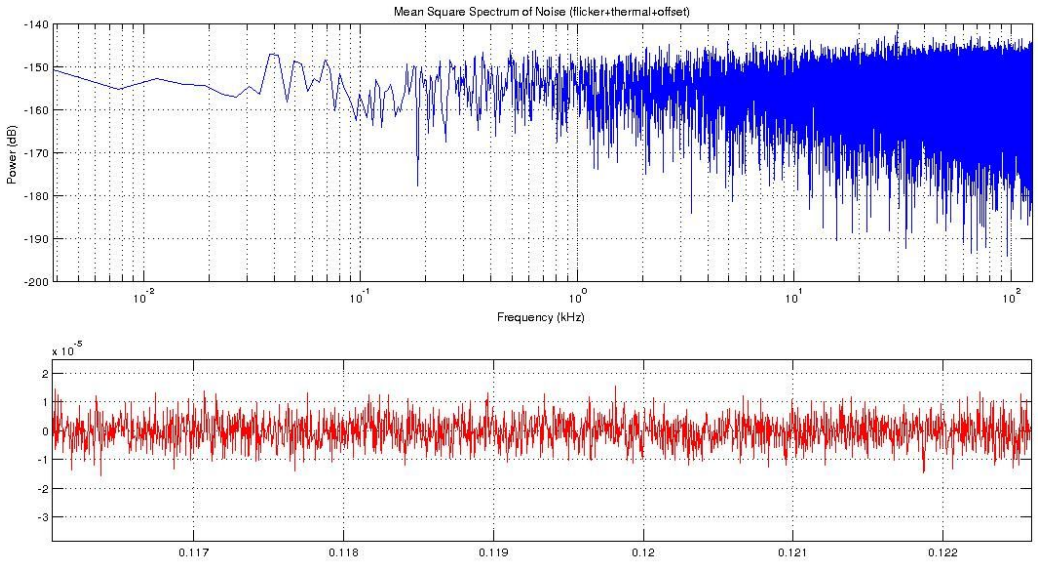

Figure C-3: PSD plot of the generated noise (thermal, flicker and offset)

The input signal passes through the chopper (modulator) and it is transposed to 50 kHz square wave chopping frequency as shown in Figure C-4.

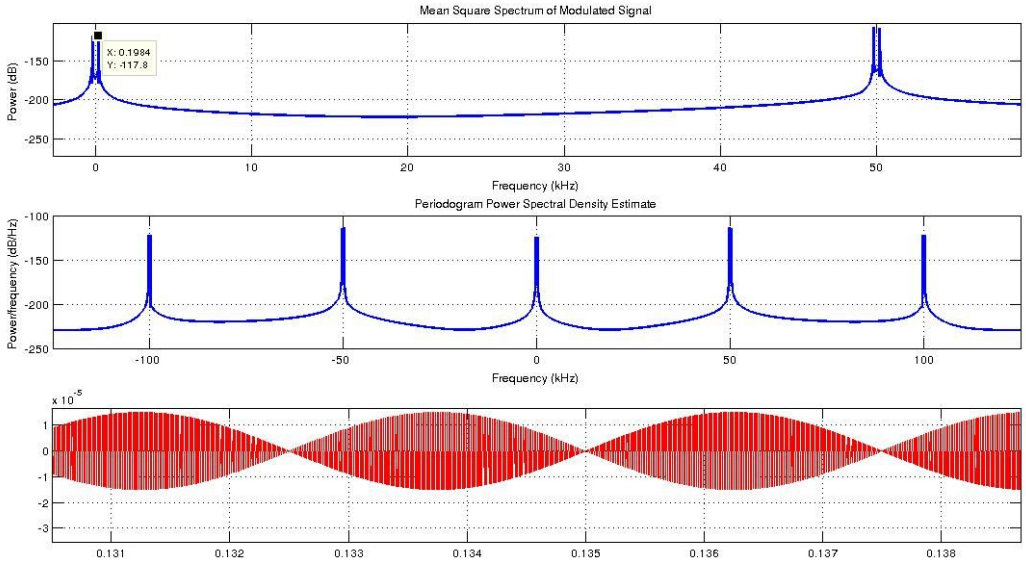

Figure C-4: simulated plot of the modulated signal

Input noise passes through the SC-HPF with 30 kHz cut-off frequency due to which low frequency noise is filtered as shown in Figure C-5.

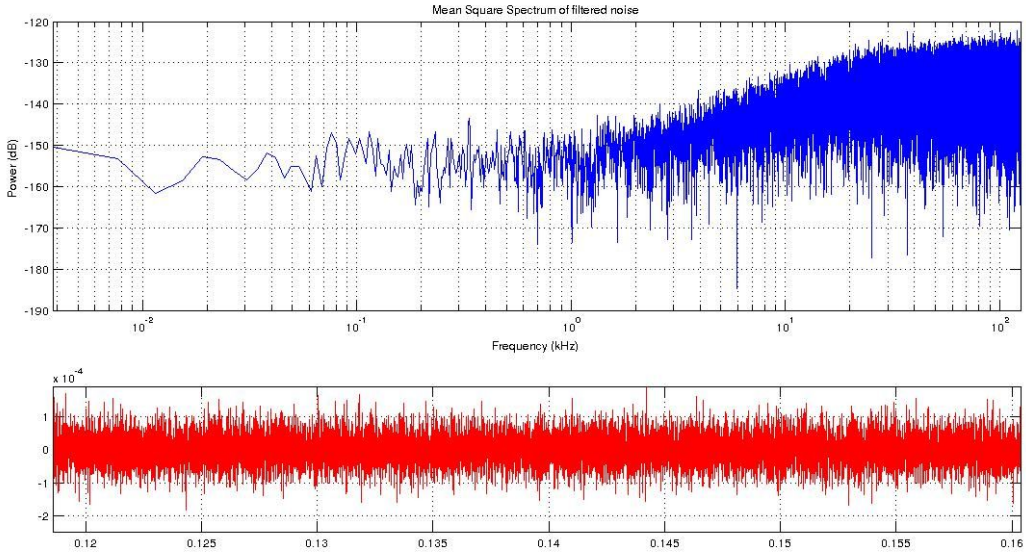

Figure C-5: simulated plot of the filtered noise

The modulated signal and filtered noise then pass through a LPF with 70 kHz cut-off frequency, followed by the demodulator. As a result, the filtered signal is demodulated while noise is transposed to 50 kHz chopping frequency as shown in Figure C-6.

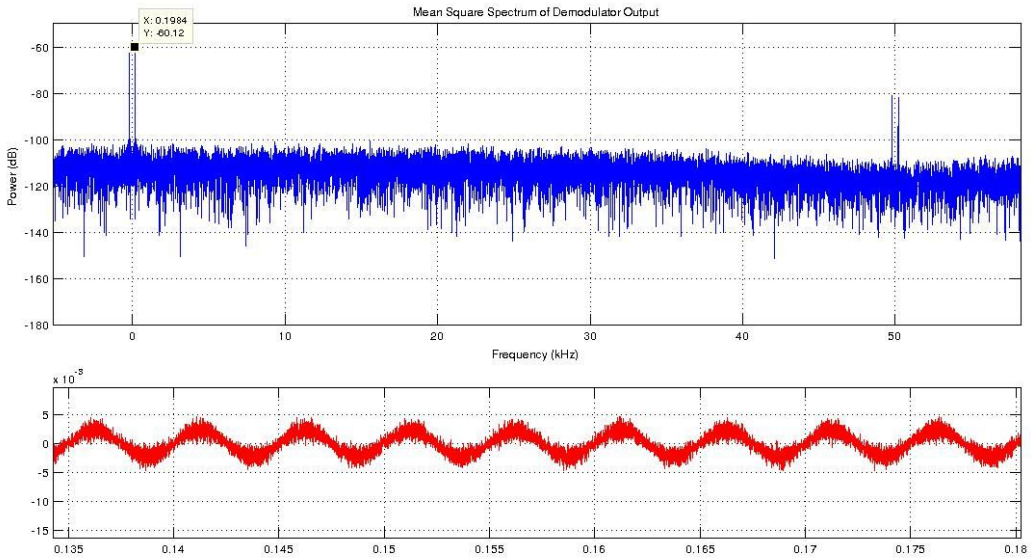

Figure C-6: simulated plot of the filtered signal and noise

Final output of the readout interface is obtained by passing signal and noise through a LPF with only 1 kHz cut-off frequency which decreases the signal bandwidth consequently reducing the integrated in band noise as shown in Figure C-7.

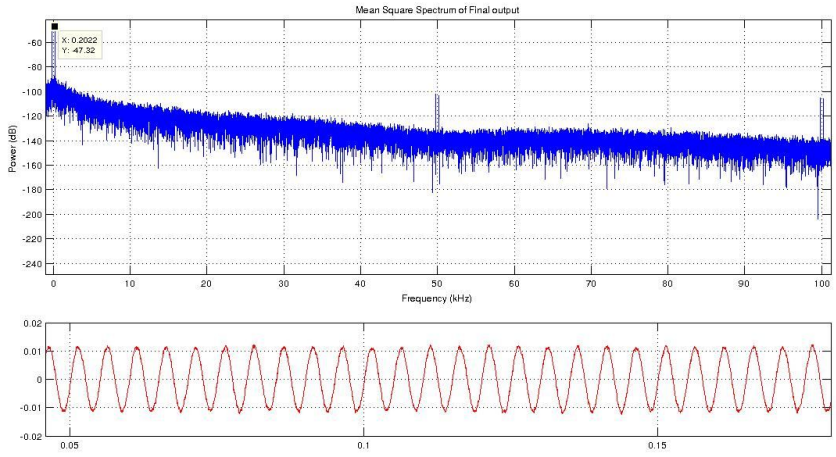

Figure C-7: Final output

REFERENCES

[1] P. H. Siegel, "Terahertz technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 910-928, 2002.

[2] Y.-S. Lee, *Principles of Terahertz Science and Technology*, 1st ed., Springer US, Ed., 2009.

[3] ''Electromagnetic spectrum''. [Online]. Avalaible: http://diarium.usal.es/meziani/?page_id=2

[4] P. H. Siegel, "THz applications for outer and inner space," in *17th International Zurich Symposium on Electromagnetic Compatibility*, Singapore, 2006, pp. 1-4.

[5] M.Shur, "Terahertz technology: Devices and applications," in *Proceedings of 35th European Solid-State Device Research Conference*, 2005, pp. 13-21.

[6] J. Federici, D. Gary, R. Barat, and D. Zimdars, "THz standoff detection and imaging of explosives and weapons," in *International Society for Optics and Photonics*, 2005, pp. 75-84.

[7] M. J. Rosker and H. B. Wallace, "Imaging Through the Atmosphere at Terahertz Frequencies," in *IEEE/MTT-S International Microwave Symposium*, Honolulu, HI, 2007, pp. 773-776.

[8] Hai-Bo Liu, H Zhong, N. Karpowicz, and X. C. Zhang, "Terahertz Spectroscopy and Imaging for Defense and Security Applications," *Proceedings of the IEEE*, vol. 95, no. 8, pp. 1514-1527, Aug 2007.

[9] Daniel M Mittleman, Ramesh Neelamani, Richard G Baraniuk, and Martin C Nuss, "Applications of terahertz imaging," in *Nonlinear Optics' 98: Materials, Fundamentals and Applications Topical Meeting*, 1998, pp. 294-296.

[10] R. Doyle et al., "Stand-off detection of hidden threat objects on personnel at checkpoints and in public areas using active millimetre-wave imaging," *Proceedings of SPIE*, vol. 5619, pp. 90-97, 2004.

[11] M. Kemp, "Millimetre wave and terahertz technology for detection of concealed threats - a review," *Joint 32nd International Conference on Infrared and Millimeter Waves and the 15th International Conference on Terahertz Electronics*, pp. 647-648, 2007.

[12] E. Herault, F. Garet, and J. Coutaz, "Critical study on the identification of concealed

substances by THz spectroscopy," *41st International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, pp. 1-2, 2016.

[13] M. Schirmer et al., "Biomedical applications of a real-time terahertz color scanner," *Biomedical optics express*, vol. 1, no. 2, pp. 354-366, 2010.

[14] E. Pickwell et al., "Terahertz imaging and spectroscopy of skin cancer," in *Conference Digest of the 2004 Joint 29th International Conference on Infrared and Millimeter Waves and 12th International Conference on Terahertz Electronics*, 2004, pp. 821-822.

[15] H. Zhong, A. Redo-Sanchez, and X. Zhang, "Identification and classification of chemicals using terahertz reflective spectroscopic focal-plane imaging system," *Optics Express*, vol. 14, no. 20, pp. 9130-9141, 2006.

[16] Y. Shen, "Terahertz pulsed spectroscopy and imaging for pharmaceutical applications: a review," *International journal of pharmaceutics*, vol. 417, no. 1, pp. 48-60, 2011.

[17] X. Yang et al., "Biomedical Applications of Terahertz Spectroscopy and Imaging," *Trends in biotechnology*, vol. 34, no. 10, pp. 810-824, 2016.

[18] M. Nuss and J. Orenstein, "Terahertz time-domain spectroscopy," , 1998, pp. 7-50.

[19] J. Federici and L. Moeller, "Review of terahertz and subterahertz wireless communications," *Journal of Applied Physics*, vol. 107, no. 11, 2010.

[20] W. Cheng, L. Changxing, D. Xianjin, and X. Shiwei, "Terahertz communication based on high order digital modulation," *2011 International Conference on Infrared, Millimeter, and Terahertz Waves*, pp. 1-2, 2011.

[21] T. Nagatsuma, G. Ducournau, and C. Renaud, "Advances in terahertz communications accelerated by photonics," *Nature Photonics*, vol. 10, no. 6, pp. 371-379, 2016.

[22] C. Kulesa, "Terahertz Spectroscopy for Astronomy: From Comets to Cosmology," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 232-240, 2011.

[23] O. Momeni and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 583-597, March 2011.

[24] R. Han and E. Afshari, "A broadband 480-GHz passive frequency doubler in 65-nm bulk CMOS with 0.23mW output power," in *IEEE Radio Frequency Integrated Circuits Symposium*, Montreal, QC, 2012, pp. 203-206.

[25] J. Rieh, D. Yoon, and J. Yun, "An overview of solid-state electronic sources and detectors for Terahertz imaging," in *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Guilin, 2014, pp. 1-4.

[26] M. Tretyakov, S. Volokhov, G. Golubyatnikov, E. Karyakin, and A. Krupnov, "Compact tunable radiation source at 180--1500 GHz frequency range," *International journal of infrared and millimeter waves*, vol. 20, no. 8, pp. 1443-1451, 1999.

[27] H. Eisele and R. Kamoua, "Submillimeter-wave InP Gunn devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 10, pp. 2371-2378, Oct 2004.

[28] M. Asada and S. Suzuki, "Room-Temperature Oscillation of Resonant Tunneling Diodes close to 2 THz and Their Functions for Various Applications," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 37, no. 12, pp. 1185-1198, 2016.

[29] D. Deacon et al., "First operation of a free-electron laser," *Physical Review Letters*, vol. 38, no. 16, p. 892, 1977.

[30] R. Han and E. Afshari, "A High-Power Broadband Passive Terahertz Frequency Doubler in CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1150-1160, March 2013.

[31] N. Sharma, W. Choi, and K.O. Kenneth, "160–310 GHz frequency doubler in 65-nm CMOS with 3-dBm peak output power for rotational spectroscopy," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, 2016, pp. 186-189.

[32] S. Muralidharan, K. Wu, and M. Hella, "A 165–230GHz SiGe amplifier-doubler chain with 5dBm peak output power," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, 2016, pp. 302-305.

[33] H. Khatibi and E. Afshari, "Towards efficient high power mm-wave and terahertz sources in silicon: One decade of progress," in *IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Phoenix, AZ, USA, 2017, pp. 4-8.

[34] B. Williams, Q. Qin, S. Kumar, Q. Hu, and J. Reno, "High-temperature and high-power

terahertz quantum cascade lasers," in *19th Annual Meeting of the IEEE Lasers and Electro-Optics Society*, Montreal, Que, 2006, pp. 128-129.

[35] B. Williams, "Terahertz quantum-cascade lasers," *Nature photonics*, vol. 1, no. 9, pp. 517-525, 2007.

[36] S. Preu, G. Döhler, S. Malzer, L. Wang, and A. Gossard, "Tunable, continuous-wave Terahertz photomixer sources and applications," *Journal of Applied Physics*, vol. 109, no. 6, p. 061301, 2011.

[37] E. Brown, "THz generation by photomixing in ultrafast photoconductors," *International Journal of High Speed Electronics and Systems*, vol. 13, no. 2, pp. 497-545, 2003.

[38] A.Rogalski and F. Sizov, "Terahertz detectors and focal plane arrays," *Opto-electronics review*, vol. 19, no. 3, pp. 346-404, 2011.

[39] H. W. Hubers, "Terahertz Heterodyne Receivers," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 14, no. 2, pp. 378-391, March-april 2008.

[40] E. Gerecht, D. Gu, L. You, and K. Yngvesson, "A passive heterodyne hot electron bolometer imager operating at 850 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1083-1091, 2008.

[41] B. Karasik, A. Sergeev, and D. Prober, "Nanobolometers for THz Photon Detection," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 97-111, 2011.

[42] M. Golay, "A Pneumatic Infra-Red Detector," *Review of Scientific Instruments*, vol. 18, no. 5, pp. 357-362, 1947.

[43] S. Liu and D. Long, "Pyroelectric detectors and materials," *Proceedings of the IEEE*, vol. 66, no. 1, pp. 14-26, 1978.

[44] A. Holden, "Pyroelectric sensor arrays for detection and thermal imaging," *SPIE Defense, Security, and Sensing*, pp. 87041N--87041N, 2013.

[45] R. Tauk et al., "Plasma wave detection of terahertz radiation by silicon field effects transistors: Responsivity and noise equivalent power," *Applied Physics Letters*, vol. 89, no. 25, p. 253511, 2006.

[46] M. I. Dyakonov and M. S. Shur, "Plasma wave electronics: novel terahertz devices using two dimensional electron fluid," *IEEE Transactions on Electron Devices*, vol. 43, no. 10, pp. 1640-1645, Oct 1996.

[47] P. Chahal, F. Morris, and G. Frazier, "Zero bias resonant tunnel Schottky contact diode for wide-band direct detection," *IEEE electron device letters*, vol. 26, no. 12, pp. 894--896, 2005.

[48] A. Golenkov and F. Sizov, "Performance limits of terahertz zero biased rectifying detectors for direct detection," *Semiconductor Physics, Quantum Electronics \& Optoelectronics*, vol. 19, no. 2, pp. 129-138, 2016.

[49] M. Sakhno, A. Golenkov, and F. Sizov, "Uncooled detector challenges: Millimeter-wave and terahertz long channel field effect transistor and Schottky barrier diode detectors," *Journal of Applied Physics*, vol. 114, no. 16, p. 164503, 2013.

[50] U. Pfeiffer and E. Öjefors, "Terahertz imaging with CMOS/BiCMOS process technologies," in *Proceedings of ESSCIRC*, Seville, 2010, pp. 52-60.

[51] U. Pfeiffer, E. Ojefors, A. Lisauskas, and H. Roskos, "Opportunities for silicon at mmWave and Terahertz frequencies," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Monteray, CA, 2008, pp. 149-156.

[52] A. Lisauskas et al., "Exploration of terahertz imaging with silicon MOSFETs," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 35, no. 1, pp. 63--80, 2014.

[53] H. Iwai and S. Ohmi, "Silicon integrated circuit technology from past to future," *Microelectronics Reliability*, vol. 42, no. 4, pp. 465-491, 2002.

[54] Seok, "Progress and Challenges Towards Terahertz CMOS Integrated Circuits," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1554-1564, Aug 2010.

[55] K. Kim, "From the future Si technology perspective: Challenges and opportunities," in *IEEE International Electron Devices Meeting (IEDM)*, 2010, p. 1.

[56] A. El Gamal, "Trends in CMOS image sensor technology and design," in *International Electron Devices Meeting IEDM'02*, 2002, pp. 805-808.

[57] L. Larson, "Silicon technology tradeoffs for radio-frequency/mixed-signal" systems-on-a-chip," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 683-699, 2003.

[58] A. Abidi, "CMOS microwave and millimeter-wave ICs: The historical background," in *2014 IEEE International Symposium on Radio-Frequency Integration Technology*, 2014, pp. 1-5.

[59] M. Bhuiyan, M. Omar, M. IBNE, K. REAZ, and F. Hashim, "A review on CMOS GM-C band pass filters in RF application," *Journal of Theoretical and Applied Information Technology*, vol. 61, no. 1, pp. 17-23, 2014.

[60] A. Lisauskas, D. Glaab, H. Roskos, E. Oejefors, and U. Pfeiffer, "Terahertz imaging with Si MOSFET focal-plane arrays," in *SPIE OPTO: Integrated Optoelectronic Devices*, 2009, pp. 72150J-72150J.

[61] U. Pfeiffer, E. Ojefors, A. Lisaukas, D. Glaab, and H. Roskos, "A CMOS focal-plane array for heterodyne terahertz imaging," in *IEEE Radio Frequency Integrated Circuits Symposium*, Boston, MA, 2009, pp. 433-436.

[62] E. Öjefors, A. Lisauskas, D. Glaab, H. Roskos, and U. Pfeiffer, "Terahertz imaging detectors in CMOS technology," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 30, no. 12, pp. 1269--1280, 2009.

[63] H. Krekels, B. Schiek, and E. Menzel, "Power detector with GaAs field effect transistors," in *22nd European Microwave Conference*, vol. 1, 1992, pp. 174-179.

[64] H. Sherry et al., "Lens-integrated THz imaging arrays in 65nm CMOS technologies," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2011, pp. 1-4.

[65] E. Ojefors, E. Pfeiffer, A. Lisauskas, and H. Roskos, "A 0.65 THz Focal-Plane Array in a Quarter-Micron CMOS Process Technology," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 1968-1976, July 2009.

[66] Y. Zhang et al., "Schottky diodes in CMOS for terahertz circuits and systems," in *IEEE Radio and Wireless Symposium*, Austin, TX, 2013, pp. 43-45.

[67] F. Schuster et al., "A broadband THz imager in a low-cost CMOS technology," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2011, pp. 42-43.

[68] H. Sherry et al., "A 1kpixel CMOS camera chip for 25fps real-time terahertz imaging applications," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2012, pp. 252-254.

[69] R. Han et al., "280GHz and 860GHz image sensors using Schottky-barrier diodes in 0.13µm digital CMOS," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2012, pp. 254-256.

[70] Y. Yang, M. Mandehgar, and D. Grischkowsky, "Understanding THz pulse propagation in the atmosphere," *IEEE Transactions on Terahertz Science and Technology*, vol. 2, no. 4, pp. 406--415, 2012.

[71] W. L. Stutzman, "Estimating directivity and gain of antennas," *IEEE Antennas and Propagation Magazine*, vol. 40, no. 4, pp. 7-11, Aug 1998.

[72] M. Perenzoni, "Measurement of spatial response of CMOS antenna-coupled FET detector at 325GHz," in *39th International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, Tucson, AZ, 2014, pp. 1-2.

[73] C. Balanis, *Antenna theory: analysis and design*, John Wiley \& Sons, Ed.: 4, 2016.

[74] Z. Jiang and X. Zhang, "Single-shot spatiotemporal terahertz field imaging," in *Optics Letters*, 1998, pp. 1114-1116.

[75] T. Chu, "An approximate generalization of the Friis transmission formula," *Proceedings of the IEEE*, vol. 53, no. 3, pp. 296-297, 1965.

[76] R. Bowman, "Field strength above 1 GHz: Measurement procedures for standard antennas," *Proceedings of the IEEE*, vol. 55, no. 6, pp. 981-990, 1967.

[77] J. Lee and S. Nam, "Effective area of a receiving antenna in a lossy medium," *IEEE Transactions on Antennas and Propagation*, vol. 57, no. 6, pp. 1843-1845, 2009.

[78] Chen-To Tai and C. Pereira, "An approximate formula for calculating the directivity of an antenna," *IEEE Transactions on Antennas and Propagation*, vol. 24, no. 2, pp. 235-236, Mar 1976.

[79] J. López-Alonso, B. Monacelli, J. Alda, and G. Boreman, "Uncertainty analysis in the measurement of the spatial responsivity of infrared antennas," *Applied optics*, vol. 44, no. 21, pp. 4557-4568, 2005.

[80] J. Alda, C. Fumeaux, I Codreanu, J. Schaefer, and G. Boreman, "Deconvolution method for two-dimensional spatial-response mapping of lithographic infrared antennas," *Applied*

Optics, vol. 39, no. 19, pp. 3993-4000, 1999.

[81] Y. Li, L. Li, A. Hellicar, and Y. Guo, "Super-resolution reconstruction of terahertz images," in *SPIE Defense and Security Symposium*, 2008, pp. 69490J--69490J.

[82] R. George, "Power Transformer Noise Its Characteristics and Reduction," *Transactions of the American Institute of Electrical Engineers*, vol. 50, no. 1, pp. 347--352, 1931.

[83] M. Ali, M. Perenzoni, and D. Stoppa, "A Methodology to Measure Input Power and Effective Area for Characterization of Direct THz Detectors," *IEEE Transactions on Instrumentation and Measurement*, vol. 65, no. 5, pp. 1225-1231, May 2016.

[84] UC Berkeley Department of Electrical Engineering and Computer Sciences. SPICE. [Online]. https://bwrcs.eecs.berkeley.edu/Classes/IcBook/SPICE/

[85] MATLAB. [Online]. https://de.mathworks.com/academia/student_version.html

[86] D. Glaab et al., "Terahertz heterodyne detection with silicon field-effect transistors," *Applied physics letters*, vol. 96, no. 4, p. 042106, 2010.

[87] D. But et al., "Nonlinear photoresponse of field effect transistors terahertz detectors at high irradiation intensities," *Journal of Applied Physics*, vol. 115, no. 16, p. 164514, 2014.

[88] T. Otsuji and M. Shur, "Terahertz plasmonics: Good results and great expectations," *IEEE Microwave Magazine*, vol. 15, no. 7, pp. 43-50, 2014.

[89] A. Lisauskas et al., "Terahertz detection and coherent imaging from 0.2 to 4.3 THz with silicon CMOS field-effect transistors," in *2012 IEEE/MTT-S International Microwave Symposium Digest*, 2012, pp. 1-3.

[90] B. Sheu, D. Scharfetter, P. Ko , and M. Jeng , "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 558-566.

[91] D. Perenzoni, M. Perenzoni, L. Gonzo, A. Capobianco, and F. Sacchetto, "Analysis and design of a CMOS-based terahertz sensor and readout," in *SPIE Photonics Europe*, 2010, p. 772618.

[92] R. Al Hadi et al., "A broadband 0.6 to 1 THz CMOS imaging detector with an integrated lens," in *IEEE MTT-S International Microwave Symposium Digest (MTT)*, 2011, pp. 1-4.

[93] R. Al Hadi et al., "A 1 k-Pixel Video Camera for 0.7–1.1 Terahertz Imaging Applications in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2999-3012, Dec 2012.

[94] A. Boukhayma, A. Dupret, J. Rostaing, and C. Enz, "A Low-Noise CMOS THz Imager Based on Source Modulation and an In-Pixel High-Q Passive Switched-Capacitor N-Path Filter," *Sensors (Basel)*, vol. 16, no. 3, p. 325, 2016.

[95] A. Boukhayma et al., "A 533pW NEP 31×31 pixel THz image sensor based on in-pixel demodulation," in *40th European Solid State Circuits Conference (ESSCIRC)*, Venice Lido, 2014, pp. 303-306.

[96] D. Kim, S. Park, and R. Han, "Design and Demonstration of 820-GHz Array Using Diode-Connected NMOS Transistors in 130-nm CMOS for Active Imaging," *IEEE Transactions on Terahertz Science and Technology*, vol. 6, no. 2, pp. 306-317, March 2016.

[97] S. Domingues et al., "Analysis of CMOS 0.13µm test structures for 0.6 to 1.5 THz imaging," in *38th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, Mainz, 2013, pp. 1-2.

[98] R. L. Geiger and E. Sánchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," *IEEE Circuits and Devices Magazine*, vol. 1, no. 2, pp. 20-32, March 1985.

[99] W. Sansen, *Analog design essentials*, Springer, Ed. Newyork, 2007.

[100] J. Chisum, E. Grossman, and Z. Popović, "A general approach to low noise readout of terahertz imaging arrays," *Review of Scientific Instruments*, vol. 82, no. 6, p. 065106, 2011.

[101] K.Laker, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, Ed., 1994.

[102] D. M. Binkley, "Tradeoffs and Optimization in Analog CMOS Design," in *14th International Conference on Mixed Design of Integrated Circuits and Systems*, Ciechocinek, 2007, pp. 47-60.

[103] F. Silveira, D. Flandre, and P. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314-1319, Sep 1996.

[104] J. Ou, "Gm/ID based noise analysis for CMOS analog circuits," in *IEEE 54th International*

Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, 2011, pp. 1-4.

[105] M. Ali, M. Perenzoni, and D. Stoppa, "A high-gain, low-noise switched capacitor readout for FET-based THz detectors," in *42nd European Solid-State Circuits Conference*, Lausanne, 2016, pp. 401-404.

[106] R. Gregorian and G. Temes, "Analog MOS integrated circuits for signal processing," *Wiley-Interscience, New York*, p. 614, 1986.

[107] Iowa State University. MonteCarlo Simulations using ADE XL. [Online]. https://wikis.ece.iastate.edu/vlsi/index.php/MonteCarlo_Simulations_using_ADE_XL

[108] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584-1614, 1996.

[109] S. Suh, S. Itoh, S. Aoyama, and S. Kawahito, "Column-parallel correlated multiple sampling circuits for CMOS image sensors and their noise reduction effects," *Sensors*, vol. 10, no. 10, pp. 9139-9154, 2010.

[110] M. Perenzoni and D. Stoppa, "Responsivity and NEP optimization of FET-based terahertz detectors," in *41st International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, 2016, pp. 1-2.

[111] F. Friederich et al., "THz Active Imaging Systems With Real-Time Capabilities," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 183-200, Sept 2011.

[112] M. Bucher, G. Diles, and N. Makris, "Analog performance of advanced CMOS in weak, moderate, and strong inversion," in *Proceedings of the 17th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES*, Warsaw, 2010, pp. 54-57.

[113] B. Murmann, "Thermal Noise in Track-and-Hold Circuits: Analysis and Simulation Techniques," *IEEE Solid-State Circuits Magazine*, vol. 4, no. 2, pp. 46-54, 2012.

[114] R. Schreier, J. Silva, J. Steensgaard, and G. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 11, pp. 2358-2368, Nov 2005.

[115] A. Mangla, C. Enz, and J. Sallese , "Figure-of-merit for optimizing the current-efficiency of

low-power RF circuits," in *Proceedings of the 18th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES*, Gliwice, 2011, pp. 85-89.

[116] K. Statnikov et al., "Methods for determining the exposure to THz radiation utilizing CMOS-based detectors," in *38th International Conference on Infrared, Millimeter, and Terahertz Waves*, Mainz, 2013, pp. 1-2.

[117] M. Ali, M. Perenzoni, and D. Stoppa, "A measurement setup for THz detectors characterization validated on FET-based CMOS test structures," in *IEEE International Instrumentation and Measurement Technology Conference (I2MTC) Proceedings*, Pisa, 2015, pp. 320-324.

[118] M. Andersson and J. Stake, "An accurate empirical model based on Volterra series for FET power detectors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 5, pp. 1431-1441, 2016.

[119] S. Domingues et al., "Analysis of CMOS 0.13 μm test structures for 0.6 to 1.5 THz imaging," in *38th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz), 2013*, 2013, pp. 1-2.

[120] M. Bucher, C. Lallement , C. Enz , F. Théodoloz , and F. Krummenacher , "The EPFL-EKV MOSFET model equations for simulation," *EPFL Lausanne Switzerland, Technical Report*, 1998.