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To cite this article: A. Loi *et al* 2024 *JINST* **19** C02069

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PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *November 3, 2023*
ACCEPTED: *January 8, 2024*
PUBLISHED: *February 27, 2024*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS
GEREMEAS, SARDINIA, ITALY
1–6 OCTOBER 2023

A prototype 4D-tracking demonstrator based on the TimeSPOT developments

A. Loi,[a,*] M. Addison,[b] L. Anderlini,[c] D. Brundu,[a] M. Boscardin,[d] S. Cadeddu,[a] A. Cardini,[a] G.M. Cossu,[a] G.-F. Dalla Betta,[e] L. Frontini,[f] M. Garau,[a] A. Lai,[a] L. La Delfa,[a] A. Lampis,[a] V. Liberali,[f] G. Passaleva,[c] L. Piccolo,[a] S. Ronchin,[d] A. Stabile[f] and M. Veltri[c]

[a] *INFN, sezione Cagliari,*
Str. Per Sestu, km 0.700, Monserrato (CA), Italy
[b] *University of Manchester,*
Oxford Road, Manchester, M13 9PL, U.K.
[c] *INFN, sezione Firenze,*
via Sansone 1, 50019 Sesto Fiorentino (FI), Italy
[d] *Fondazione Bruno Kessler,*
Via Sommarive, 18, 38123 Povo (TN), Italy
[e] *Universita degli Studi di Trento and INFN,*
Via Sommarive, 9, 38123 Povo (TN), Italy
[f] *Universita degli Studi di Milano and INFN,*
Via Celoria, 16, 20133 Milano (MI), Italy

E-mail: angelo.loi@ca.infn.it

ABSTRACT: We present first results obtained with a prototype 4D-tracking demonstrator, using sensors and electronics developed within the TimeSPOT project, and tested on a positive charged pion beam at CERN SPS. The setup consists of five small tracking layers in a row, having area of about 3 mm^2 each, three of which equipped with 3D-trench silicon sensors and two with 3D-column diamond sensors. The five layers are then read-out by a KC705 Xilinx board on a PC. We describe the demonstrator structure and operation and illustrate preliminary results on its tracking capabilities.

KEYWORDS: Front-end electronics for detector readout; Particle tracking detectors; Particle tracking detectors (Solid-state detectors); Timing detectors

*Corresponding author.

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https://doi.org/10.1088/1748-0221/19/02/C02069

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1 Introduction

In preparation for forthcoming experiments at the High Luminosity Large Hadron Collider (HL-LHC) and beyond, it is mandatory to develop experimental solutions capable to cope with higher luminosity levels (up to a factor seven). This increased luminosity poses challenges across various aspects of detector technologies, including managing higher data rates and increased radiation exposure. For specific particle tracking detectors, such as a potential VErtex LOcator detector for the LHCb Upgrade II) [1], meeting specific performance criteria is crucial, requiring them to be radiation-tolerant up to 10^{17} 1 MeV (n_{eq}/cm^2). Also spatial resolution around 10 µm and the inclusion of time-tagging capabilities with a resolution equal to or better than 50 ps are key aspects for the needed track reconstruction performance. A critical focus lies on optimising sensor components and integrated circuits. The former involves improving the timing characteristics of radiation-resistant, high spatial resolution 3D silicon sensors, while the latter entails using smaller-scale 28-nm CMOS technology within the detectors to mitigate radiation-induced damage and reduce power consumption.

This paper offers a short summary and account of the work conducted over the past four years. In the first section, we describe the timing-optimised 3D silicon sensor, highlighting its parallel trench design and presenting the results from the first beam tests. In the second section, we introduce the Timespot-1 Application-Specific Integrated Circuit (ASIC), discussing its architecture and inherent performance. We then proceed to describe the Timespot-1 sensor-ASIC hybrid in both configurations, involving both the diamond and silicon sensor matrices. Finally, we conclude the summary by providing the results of the most recent beam test, where we tested a complete tracking demonstrator comprising five stations.

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2 Timing optimised 3D silicon sensors

The requirement for a sensor capable of withstanding radiation damage exceeding 10^{16} 1 MeV n_{eq}/cm^2, all while achieving an intrinsic time resolution below 50 ps, led to the design of the TimeSPOT 3D silicon sensor with a parallel trench electrode geometry [2]. The device features a pitch of 55 µm and is constructed on a 150 µm thick, high-resistive silicon wafer serving as the active bulk material, which is wafer-bonded to a second high-conductive silicon wafer primarily for mechanical support during the fabrication process. The single pixel channel is characterised by a 3 parallel trench geometry, the two outer electrodes are p++ doped and provide the bias voltage for the electric field and are shared among more pixels. The middle trench, discontinuous, is used as readout electrode and is n++ doped (figure 1). Two production batches were completed in 2019 and 2021 at FBK in Trento, each

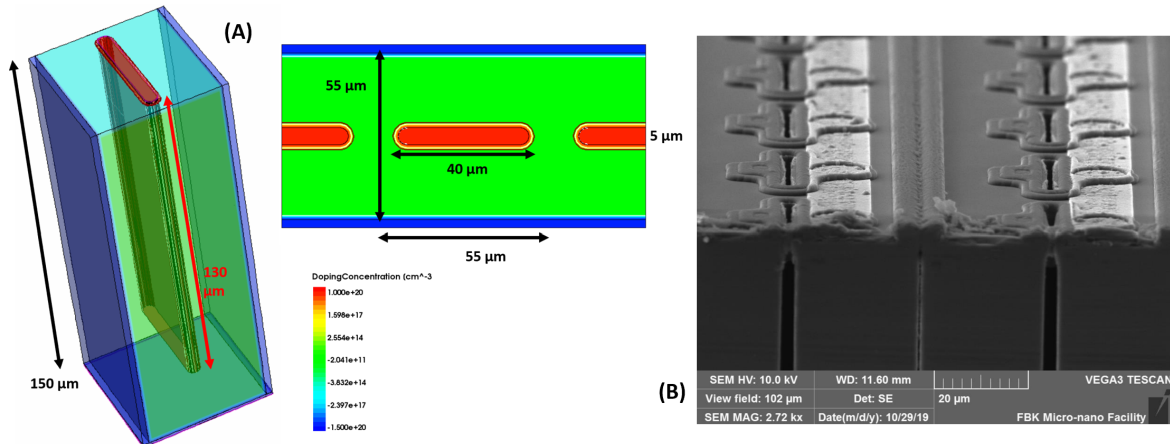

Figure 1. (A) TCAD rendering of the TimeSPOT 3D trench electrode sensor. (B) Cross section of silicon strip sensor based on the TimeSPOT sensor produced by FBK.

incorporating distinct test structures and pixel matrices. Furthermore the second batch presented a more improved fabrication process to increase production yield. Over the past four years, a sequence of three beam tests were undertaken to assess the pixel geometry in terms of intrinsic time resolution and performance after exposure to radiation comparable to future LHCb conditions. For this purpose, a dedicated readout board, based on a discrete component analog readout was designed and produced by INFN Cagliari. During the latest beam test in 2022, an intrinsic time resolution of 10.9 ps was measured for the un-irradiated sensor [3]. Same resolution was confirmed for irradiated sensors with a total radiation damage of $2.5 \cdot 10^{16}$ 1 MeV n_{eq}/cm^2, demonstrating that the technology is capable of matching with the requirements for a future VELO phase 2 tracker [1, 4].

3 Timespot-1 ASIC

Another key aspect of the TimeSPOT project revolved around the exploration and development of new integrated circuit solutions for readout and time measurement using 28 nm integrated circuit CMOS technology. These efforts resulted in the design of the Timespot-1 ASIC [5], serving as a technological demonstrator for an integrated circuit capable of accommodating small pixel matrices measuring 32×32 pixels, with a pitch of 55 um, achieved through bump-bonding connections, with the main purpose of hosting the dedicated TimeSPOT 3D parallel trench pixel matrix.

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The 1024 channel pixel matrix is organised in two main blocks of 16×32, 512 pixel each. Each pixel block is divided into two quadrants of 256 pixels with a dedicated read-out tree (ROT). Each ROT adds a timestamp to each detected event and channels the data towards one of two dedicated serialisers which output the data in double data rate LVDS at 640 MHz. The maximum sustainable data rate is 1.28 Gbit/s per LVDS channel for an overall data output of 10.24 Gbit/s. Each single pixel channel occupies an area of 55×50 μm^2, which allows to free enough surface to use it for routing and power supply. The analog front-end (AFE) occupies circa 30 percent of the entire pixel area and it is based on a two-stage amplifier, with a charge sensitive amplifier (CSA) and a leading edge discriminator. The remaining area is dedicated to the digital electronics, in particular the time to digital converter (TDC), which is based on a Vernier Architecture and run by two identical Digital Controlled Oscillators (DCOs) working with a programmable tapped delay line [5].

The Timespot-1 ASIC was previously tested without bonded sensor in order to study the intrinsic performances of its TDCs and AFEs. For this purpose and for the successive beam test, the Tspot-1 board was developed, which allows the user to fully access, test and monitor the entire ASIC input and output using an I^{2}C interface, logic analyser and FPGA with dedicated firmware. From the initial test campaign, we found that the collective average time uncertainty for all 1024 TDCs in a single Timespot-1 is 22.6 ps. For the AFEs the resolution depends on the injected charge, which can be injected in the AFE by a dedicated internal pulse generator, capable to generate up to 10 fC of charge. By using this approach it was determined that the AFE's introduces an average uncertainty of 43 ps [5].

3.1 ASIC hybridisation

The Timespot-1 ASIC was connected with two different types of pixel sensors. One is based on a 32×37 pixel matrix of the 3D silicon sensor with trench geometry, the other one is a columnar electrode based 3D diamond sensor [6], developed and fabricated at INFN Firenze. Hybridisation process was performed by the Fraunhofer Institute for Reliability and Micro-integration (IZM). Pixel matrix on both sensors had to be increased by 5 rows in order to cope with the mechanical requirements requested by IZM for their bump-bonding process. For this purpose, the Timespot-1 ASIC presents extra 5 bump pad rows on the surface to guarantee the mechanical application of the indium bumps (figure 2).

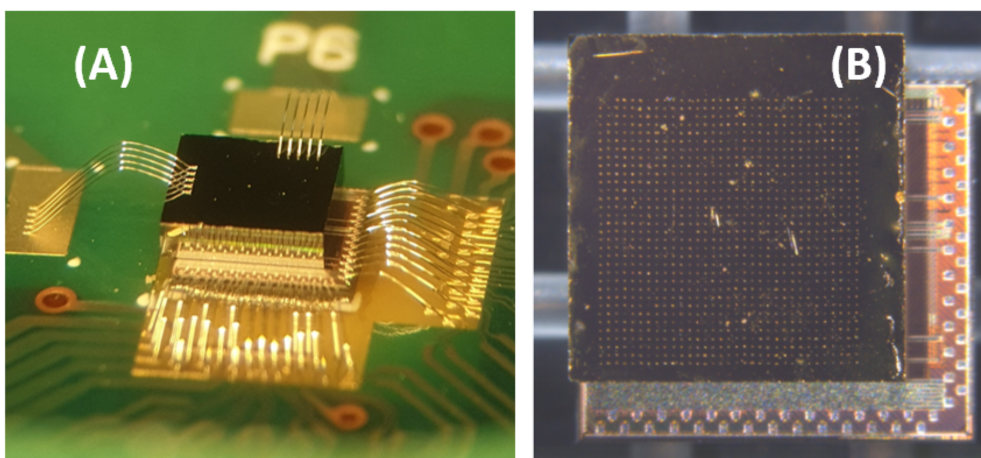

Figure 2. (A) Lateral picture of Timespot-1 with 3D silicon sensor matrix (top black cuboid) (B) Timespot-1 hybrid with 3D diamond sensor on top. Reproduced from [6]. CC BY 4.0.

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4 Test-beam

Timespot-1 underwent intense beam testing in the period of April to May 2023. Five Timespot-1 boards were specifically fabricated for this test, with three boards accommodating the 3D silicon sensor matrix and two boards accommodating the 3D diamond sensor matrix.

4.1 Setup

To minimise alignment uncertainty, the complete setup was installed on a compact optical table measuring 1×0.5 m^2, which included a dedicated rail, on which every single station was installed. The fine alignment of the entire rail, with respect to the beam was achieved by using two strip sensor boards installed at both ends of the rail. These two boards were mounted on the rail and featured a piezoelectric mechanisms for fine movement. The output of the boards was connected to an oscilloscope used to count the number of events passing through the sensor. This allowed to measure the beam shape and determine the position of the beam with respect of the rail, which then was corrected by applying the correct counter roto-translation.

The complete tracking and alignment system, along with the analog supply relay for the Timespot-1 boards, is enclosed within a sizeable metal box in order to minimise external electromagnetic interference.

Externally, a silicon-lab clock generation board (model 5341-D) is mounted and provides the reference clock of 640 MHz towards all Timespot-1 boards and the FPGA (model KC705), which is too mounted externally with the mezzanine and works as data acquisition hardware (DAQ). The mezzanine is an active PCB board that acts as interface between the high density, LVDS formatted, data output of the Timespot1 ASICS and the FMC ports of the FPGA. All Timespot-1 boards are controlled with a dedicated USB-I^{2}C interface connected to a windows computer running a customised software (figure 3).

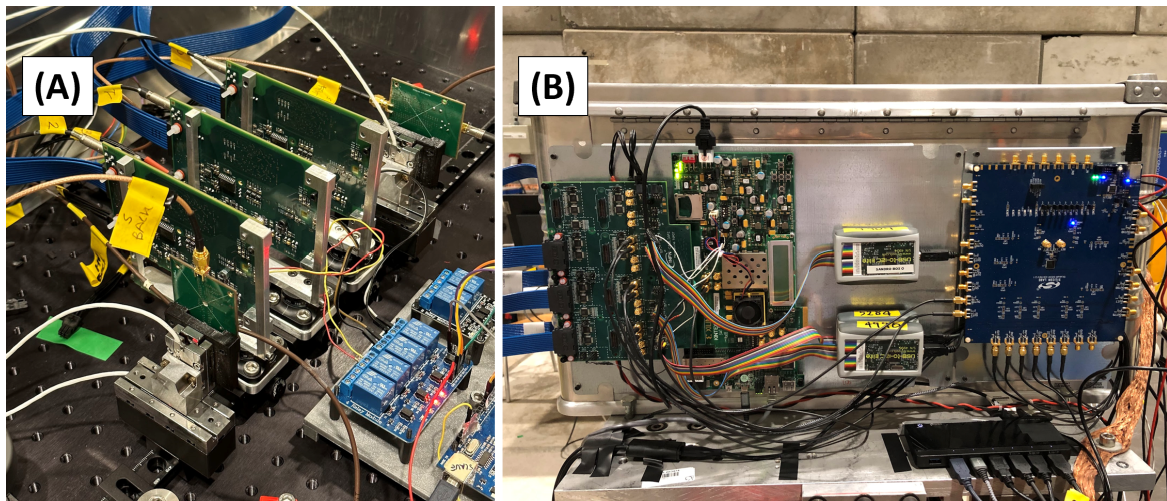

Figure 3. (A) Setup used during alignment. Both strip sensor boards are visible. (B) External setup of the tracker, with FPGA, mezzanine, I^{2}C interface boards and clock source.

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4.2 DAQ and monitoring system

A FPGA board, model Xilinx KC705 evaluation, with dedicated firmware works as DAQ and monitoring system.

The firmware has been designed to operate the FPGA together with the TimeSPOT mezzanine, allowing it to acquire data from a maximum of 8 Timespot-1 boards. Each board provides 8 LVDS_25 data links which send data to the mezzanine in double data rate at 1280 Gb/s per link.

Each data link is processed by the firmware independently of the others and presents the same architecture, synchronous to a 160 MHz service clock. The serial data enters the FPGA and, after passing through an initial Tap Delay Line (TDL), is de-serialised into an 40 bit bus, containing the information of the Time-of-Arrival (ToA), Time-over-Threshold (ToT), channel address and ASIC timestamp. The data word is then completed by the FPGA firmware by adding additional 24 bits, containing an internally generated timestamp, the ASIC address and data link address. The data is then stored in a temporary First In First Out (FIFO) memory block which is continuously read every 64 160 MHz clock cycles by a continuously operating multiplexer. This sends the data for the final memory block with maximum capacity of 131072 events. The entire control and monitoring of the FPGA parameters, as well as data saving on a dedicated computer, is achieved by using intellectual property (IP) of the CERN IPBUS firmware [7].

5 Results

The Timespot-1 hybrid modules underwent pre-beam test validation to ensure proper functionality. It was during these test campaign that a leakage current issue was identified in all three silicon hybrids when the sensor was under bias, at the level of μA over the full pixel matrix. This effect, whose real causes are still under investigation, prevented the correct biasing of the sensors, which receive an effective limited biasing around 1 V. The diamond hybrids were not affected by such a problem.

At the moment, a possible explanation about such unwanted electrical behaviour is that the 5 extra pixel rows, requested for additional mechanical stability of the sensor on the ASIC, caused an electrical perturbation due to their floating state. The sensor would charge up during biasing, transferring the bias potential directly on top of the ASIC, where only a very thin layer of passivisation insulates the sensor from the metal layer of the ASIC. This hypothesis is also coherent with what was observed with the diamond hybrid, which did not show the same behaviour, due to the fact that diamond behaves more like an insulator instead of a semiconductor. Therefore, the tracker was operated with the silicon hybrids at 1 V bias and the diamond hybrids at 100 V bias. Despite this technical issue, it was possible to observe tracks through the entire tracker (figure 4), due to the fact that the 3D silicon sensor geometry is already partially depleted at build-in potential. Preliminary analysis showed a time resolution of around 200 ps which is still being analysed, using the Trans Current Technique (TCT) setup in Cagliari.

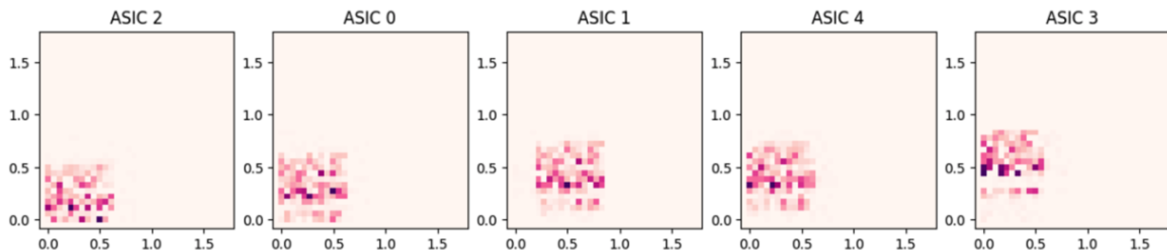

Figure 4. Hit map of all 5 tracking stations related to only coincidences.

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6 Conclusions

With the Timespot-1 ASIC a long journey in the development of novel technologies for future tracking detectors is concluded. Further advancements and research are merged within the INFN IGNITE initiative, which will focus in particular on the aspects of an ASIC for future 4D tracking detectors with large area coverage. Analysis and further tests on the Timespot-1 beam test are still ongoing, with a more in depth focus on the single tracking station using the available TCT setup. In addition to the inferior results obtained with the technological demonstrator when compared to the results achieved with the standalone ASIC and sensor, the experience and data gathered are deemed highly significant and strategically valuable for future developments.

Acknowledgments

The authors wish to thank the staff of North Hall Area at CERN for their help in the beam-line setup and operations.

Funding. This work was supported by the First Scientific Commission (CSN1) of the Italian National Institute for Nuclear Physics (INFN), within the IGNITE Project.

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