Hindawi
International Journal of RF and Microwave Computer-Aided Engineering
Volume 2023, Article ID 3786691, 13 pages
https://doi.org/10.1155/2023/3786691

Research Article

Performance Analysis of a Reconfigurable Mixer Using Particle Swarm Optimization

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Received 1 December 2022; Revised 3 August 2023; Accepted 22 August 2023; Published 20 October 2023

Academic Editor: Giovanni Crupi

In this article, a novel 1.8-5 GHz downconversion mixer is presented. The mixer is designed and simulated using SiGe 8HP 130 nm CMOS process technology. The proposed mixer is implemented by incorporating a double-balanced configuration, active inductor, and current mirror techniques. For performance optimization of the proposed mixer, different algorithms such as the genetic algorithm (GA), inclined plane system optimization (IPO) algorithm, and particle swarm optimization (PSO) algorithm have been used. Compared to existing works, this design shows an enhanced conversion gain (CG), a third-order input intercept point (IIP3), and return loss (S_{11}) at the expense of the noise figure (NF). Additionally, the design consumes low power and covers a small chip area compared to other state-of-the-art devices. PSO shows the most promising results when compared to other optimization algorithms' results. According to the measurement results after PSO optimization, the mixer attains a maximum CG of 25 dB, an IIP3 of 4 dBm, and a NF of 5.2 dB at 5 GHz, while consuming only 15 mW of DC power. The mixer operates at 1.2 V and covers 0.8 mm^2 die area.

1. Introduction

With recent advances in the wireless industry, it is desirable to develop sophisticated receivers with reconfigurable components, which can be used to support a variety of wireless standards, significantly reducing development time and cost. Software-defined radios (SDRs) have proven to be a promising candidate that offers considerable flexibility by enabling various band operations within a single circuitry [1]. Mixers are one of the most critical components of SDRs.

Generally, mixers can be classified as passive mixers and active mixers [2]. Based on the design specifications, any of these mixer topologies can be used. For example, passive mixers maintain high linearity and good noise figure (NF) performance at the expense of port isolation. Likewise, the port isolation problem can be overcome by active mixers. Moreover, these mixers can provide high conversion gain (CG) and low NF at the expense of linearity. Gilbert mixers are one of the common types of active mixers that are widely used in RF circuits [3–5]. These mixers are adopted in SDR receivers due to their broadband operation and wideband coverage [6]. However, because of the parasitic capacitance at different nodes, these mixers are not suitable for high-frequency applications. To address this issue, folded structures can be utilized due to less number of transistor requirements; however, they consume high power. Different techniques can be used to enhance the performance of a mixer, of which current bleeding appears promising.

Several mixers were reported in the literature based on the current bleeding approach that integrated inductive degeneration [7], forward body, inductive gate bias, inductive resonance [8], and gm/ID [8] techniques to improve the overall performance of the proposed mixers. However, the proposed mixers were not able to maintain high linearity. Therefore, based on literature studies, various promising techniques have been identified that are capable of improving linearity performance, such as resistive degeneration [9] and derivative superposition [10]. In [11], an improved derivative superposition technique is used to enhance the linearity performance of the mixer. Current bleeding and current reuse techniques are also used to enhance CG and NF performance. The proposed mixer not

only consumed less power but also small chip area. Another mixer based on source degeneration and current bleeding with a resistive load approach is proposed in [12]. The proposed mixer consumed less power and attained reasonable CG and high IIP3 at the expense of NF. To further enhance the NF and CG performance, another mixer based on the conventional Gilbert mixer is proposed [13]. The proposed mixer employed a differential active inductor (DAI) circuit, a cross-coupled current injection technique, and cross-coupled current bleeding techniques to improve flicker noise and CG performance. Active inductor circuitry resonates with parasitic components, thus lowering the leakage current that contains harmonic components and generating flicker noise [14]. Finally, a high IIP3 and low NF mixer based on active load, cross-connected design topology, and current bleeding technique are proposed [15]. The proposed mixer is well suited for wireless local area network applications. However, the above proposed designs involve many tradeoffs among CG, NF, IIP3, and power consumption, resulting in a more complicated design [16–19]. Moreover, sizing circuits to meet specific performance specifications is an intricate and time-consuming process. Nowadays, researchers are primarily concerned with space limitations and economic factors. Designers perform several functional experiments using computer simulations and design software in order to meet these requirements. Manual adjustment of the tunable parameters is a time-consuming task. Therefore, researchers have attempted to employ optimization algorithms to optimize the circuit parameters [20, 21]. Genetic algorithm (GA) [22], inclined plane system optimization (IPO) algorithm [20], and particle swarm optimization (PSO) are some of the commonly used algorithms to solve the multiobjective problems where CG, NF, and IIP3 are the objectives or parameters to be optimized [23, 24]. The implementation of these algorithms has been described in several studies by researchers, but no work has been identified that shows the implementation of these algorithms on mixers. Thus, to the best of our knowledge, our work is the first to demonstrate such implementation on a mixer.

In this work, a novel double-balanced mixer was proposed with the objective of achieving high CG and good IIP3 and an active inductor technique was found to be the most efficient method to achieve these objectives. Based on this, an active inductor circuit is employed instead of passive inductors within the circuit. In addition, a triple transistor current mirror circuit is used instead of a conventional current mirror circuit to control the overall current within the circuit. Moreover, due to the limitations of the Gilbert mixer, the proposed design uses mixing stages based on single transistors, resulting in a small chip area. GA, IPO, and PSO have been used to optimize mixer performance using an equation-based approach using MATLAB. The proposed mixer is designed and simulated in SiGe 8HP 130 nm CMOS process technology to validate that the optimization-based design is satisfying the desired specifications. The remainder of the paper is organized as follows. Section 2 discusses the proposed mixer design, and Section 3 presents the analysis of the design. Section 4 describes optimization algorithms, and the results of the proposed design are discussed in Section 5, and finally, Section 6 concludes the paper.

2. Proposed Mixer

Figure 1 shows the design of the proposed balanced mixer. The mixer consists of a mixing stage, improved current mirror stage, and active inductor stage, respectively.

2.1. Current Mirror. Circuits that mirror current are constructed using two main transistors, which reflect current that flows through one transistor and flows through the other. Depending on the circuit requirements, the copied current can be constant or variable [25]. The proposed mixer's current mirror stage consists of transistors (T_0, T_1, T_6, T_7, and T_8) responsible for controlling the current within the circuitry. Similarly, to maintain symmetry within the circuit, another current mirror circuit consists of transistors (T_9-T_{13}). All transistors operate in the saturation region. Transistors T_7 and T_{10} are responsible for mirroring the current within the transistors T_8 and T_9. This current will be mirrored to the transistors T_0 and T_{12} which are responsible for providing the current to the transistors T_1 or T_{11}. Transistors T_1 or T_{11} also receive current from the transistors T_6 or T_{13} so that sufficient current is maintained within the mixing stage transistors T_3 and T_4, respectively.

2.2. Mixing Stage. The mixing stage consists of n-type field effect transistors (NFETs) (T_3, T_4). According to the design, RF+/RF- and LO+/LO- inputs are imparted through the gate and source terminals. Likewise, IF+/IF- outputs are obtained at the drain terminals.

Due to their tightly controlled physical sizes, resistors are difficult to fabricate, which makes transistors an optimal choice at the load instead of resistors. Further, high CG requires large drain resistors, resulting in a lower DC biasing voltage required at the output port. As a result, transistor operating conditions may be affected. Thus, using transistors (T_2 and T_5) at the load, the current increases within the mixing stage to such an extent that T_3 and T_4 operate in the saturation region and result in minimal flicker noise. Consequently, this improves the transconductance and hence the overall CG.

2.3. Differential Active Inductor. There are a variety of passive electronic components available in complementary metal-oxide semiconductor- (CMOS) based process technologies, including bond wires, spirals, multilevel spirals, and solenoids [26]. The choice of inductors varies with the application.

Spiral-layout inductors are commonly used in signal processing and data communication applications. They have degraded performance because their spiral layout structure requires large silicon areas, causing a low-quality factor and low self-resonance frequency. Therefore, active inductors are typically employed in circuits. Various active devices are used to develop these inductors, including metal-oxide-semiconductor field effect transistors (MOSFETs), operational amplifiers (Op-Amps), operational transconductance amplifiers (OTAs), and resistors [27]. Inductors are usually

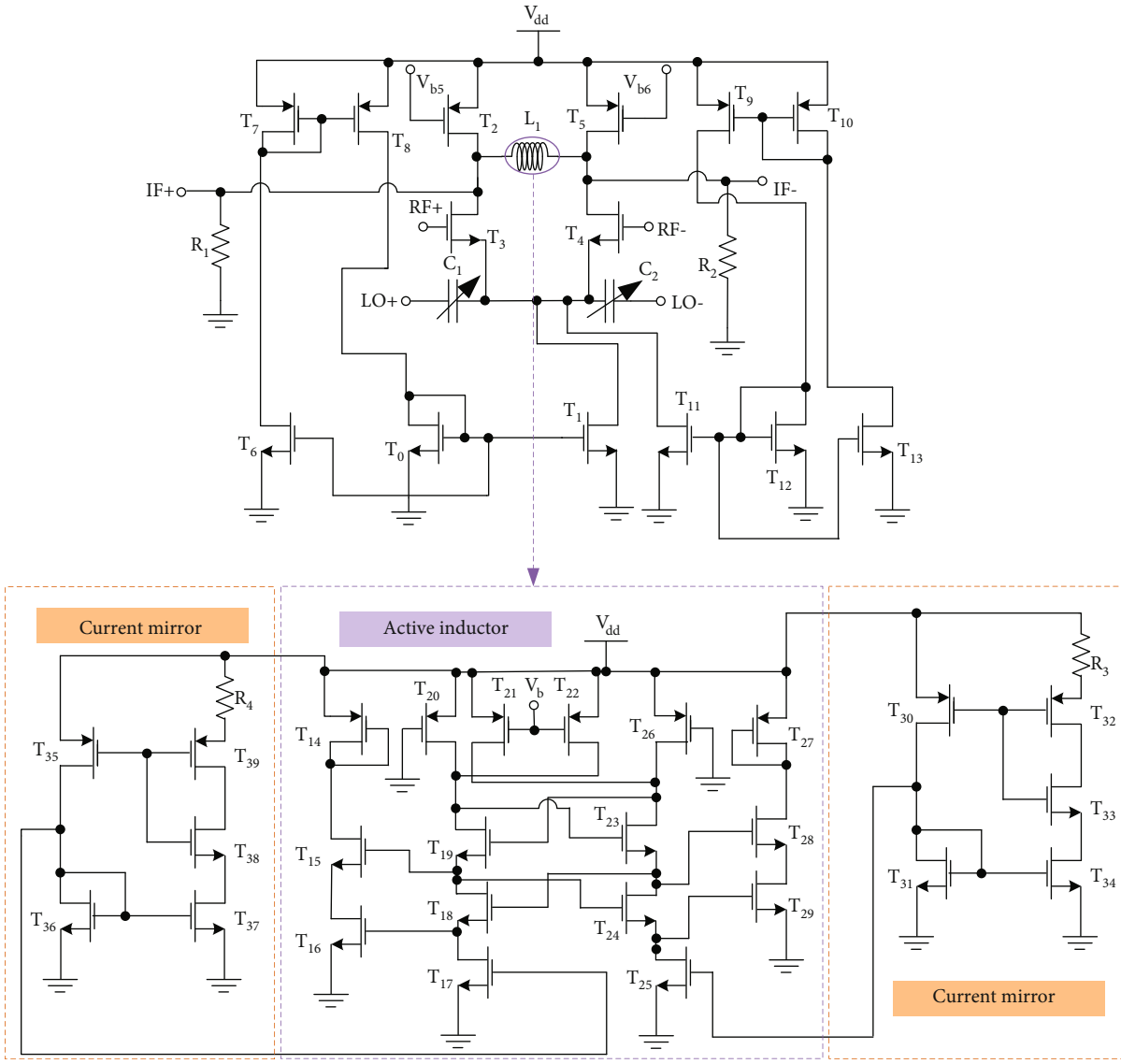

FIGURE 1: Schematic of the proposed mixer.

used in conjunction with resistors as feedback elements, which ultimately improve the overall performance of active inductors. Alternatively, inductors can be used in a gyrator C topology, which contains two transconductors arranged in a feedback configuration. As long as DC bias conditions and signal swing restrictions are met, an actively biased network (a combination of active devices) behaves as an inductor within a specific frequency band [28]. These inductors have high tunability and quality factors, making them suitable for low amplifiers and mixers as differential RF front-ends.

High linearity is also desired in SDR mixers while maintaining reasonable CG at the expense of NF, which can be achieved by using an active inductor across the IF stage of the design. The active inductor circuit topology is useful within the mixer circuitry to tune out parasitic capacitors and thus reduce flicker noise [13]. Various active inductor topologies are discussed in [29, 30]. We propose a mixer that uses a differential active inductor with current mirror circuitry. Cascode reduces output conductance and boosts gain at high frequencies using this technique. Dual gain stages were incorporated within this stage to maximize the cascode effect. The transistors (T_{20}-T_{22}, T_{26}) operate in saturation region. Moreover, transistors (T_{21}-T_{22}) are biased in the triode region that behave as voltage-controlled resistors. The bias voltages of these transistors are varied to show the tunability behavior of the inductor. The cross-coupled transistors are balanced with the other transistors, i.e., (T_{19} and T_{23}) and (T_{18} and T_{24}), respectively. Transistors T_{14} and T_{27} are diode loads. Moreover, transistors (T_{15}-T_{16}) and (T_{28}-T_{29}) deliver current to the next stages.

A current mirror circuit controls the current in the active inductor by mirroring the current from current mirror stages from the left- and right-hand sides of the active inductor to transistors (T_{17} and T_{25}), respectively. RL equivalent circuit is used to simplify the active inductor circuitry as

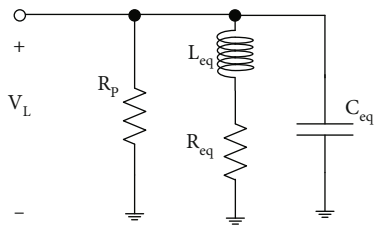

FIGURE 2: Equivalent circuit of an active inductor.

shown in Figure 2 [31]. The expressions for the RL circuit are defined as follows:

$$\begin{aligned} C_{eq} &= C_{gs18}, \\ R_p &= \frac{1-\omega^2\left(C_{gs19}C_{gs15}/g_{m19}g_{m15}\right)}{g_{m18}}, \\ L_{eq} &= \frac{C_{gs23}}{g_{m17}g_{m18}g_{m23}}\left(1-\frac{\omega^2 C_{gs19}C_{gs15}}{g_{m19}g_{m15}}\right), \\ R_{eq} &\approx -\frac{\omega^2 C_{gs23}C_{gs15}}{g_{m15}g_{m18}g_{m23}g_{m17}}, \end{aligned} \tag{1}$$

where g_{m15}, g_{m17}, g_{m18}, and g_{m23} are transconductance of transistors T_{15}, T_{17}, T_{18}, and T_{23}. R_{eq} is very small due to the second-order effect. To obtain the resonant frequency (ω_{RES}), R_{eq} is neglected, which is given by

$$\begin{aligned} \omega_{RES} &= \sqrt{\frac{g_{m18}g_{m23}}{C_{gs18}C_{gs23}\left(1-\omega^2\left(C_{gs19}C_{gs15}/g_{m19}g_{m15}\right)\right)}} \\ &= \sqrt{\frac{\omega_{t18}\omega_{t23}}{\left(1-\omega^2/\omega_{t19}\omega_{t15}\right)}}, \end{aligned} \tag{2}$$

where $\omega = g_m/C_g$ for transistors at resonant frequency. Thus, ω_{t15}, ω_{t18}, ω_{t19}, and ω_{t23} correspond to transistors T_{15}, T_{18}, T_{19}, and T_{23}.

To determine the broadband characteristics of the active inductors, it is necessary to calculate the quality factor (Q factor), which can be approximated by the following expression:

$$\begin{aligned} Q \approx & \left(\frac{\omega^2 C_{gs18}}{g_{m18}}\left(\frac{C_{gs23}}{g_{m23}}\right) - \omega^2\left(\frac{C_{gs23}}{g_{m23}}\right)\frac{C_{gs15}}{g_{m15}} + \omega^2\frac{C_{gs19}}{g_{m19}}\frac{C_{gs15}}{g_{m15}} - 1\right) \\ & \times \left(\omega\left(\frac{C_{gs23}}{g_{m23}}\right) - \omega\frac{C_{gs15}}{g_{m15}}\right)^{-1} \\ = & \frac{\left(\omega^2/\omega_{t23}\omega_{t18}\right) - \left(\omega^2/\omega_{t23}\omega_{t15}\right) + \left(\omega^2/\omega_{t15}\omega_{t19}\right) - 1}{\left(\omega/\omega_{t23}\right) - \left(\omega/\omega_{t15}\right)}. \end{aligned} \tag{3}$$

3. Performance Analysis

3.1. Conversion Gain. Figure 3 shows the complete small signal model for the proposed mixer circuit for CG analysis.

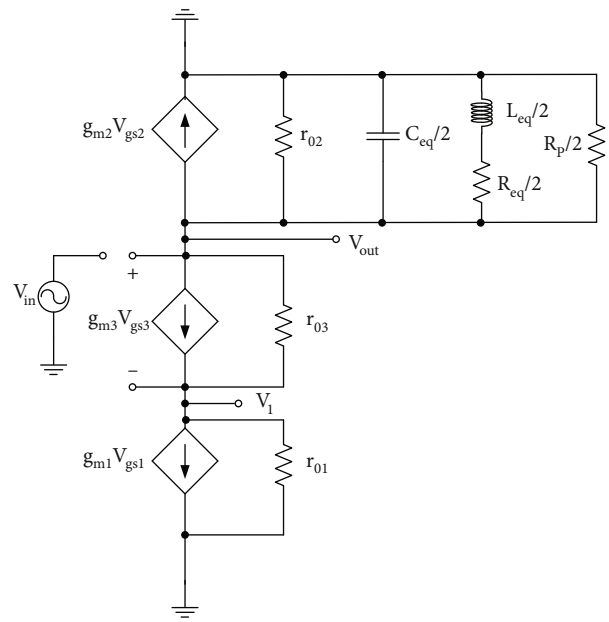

FIGURE 3: Complete small signal model for half circuit.

The load and current mirror sections are simply represented as resistors (r_{02}, r_{01}). Furthermore, the active inductor is defined using an equivalent RL circuit as shown Figure 2. Thus, the complete circuit behaves like a common source amplifier with a source-degeneration resistor. Based on the circuit shown in Figure 3, the controlled current source determines the current through R_S. Voltage, V_1 can be expressed as

$$V_1 = \frac{g_{m3}R_S V_{in}}{\left(1+g_{m3}R_S\right)}, \tag{4}$$

Gain, A_1 can be expressed as

$$A_1 = \frac{V_1}{V_{in}} = \frac{g_{m3}R_S}{1+g_{m3}R_S}. \tag{5}$$

Once V_1 is obtained, the output voltage, V_{out} can be expressed as

$$V_{out} = -R_D\left(g_{m3}V_{gs3}\right) = -g_{m3}R_D(V_{in}-V_1), \tag{6}$$

where $R_D = r_{02}\|-jX_{Ceq}/2\|((R_{eq}/2)+jX_{Leq}/2)\|(R_P/2)$.

Substituting V_1 from (5) to (6), we get

$$V_{out} = -\frac{g_{m3}R_D}{1+g_{m3}R_S}V_{in}, \tag{7}$$

where $R_s = r_{01}$.

$$A_0 = \frac{V_{out}}{V_{in}} = -\frac{g_{m3}R_D}{1+g_{m3}R_S}. \tag{8}$$

To determine the impact of parasitic capacitors, C_{gd3} and C_{gs3}, Miller's theorem can be used, which relates the

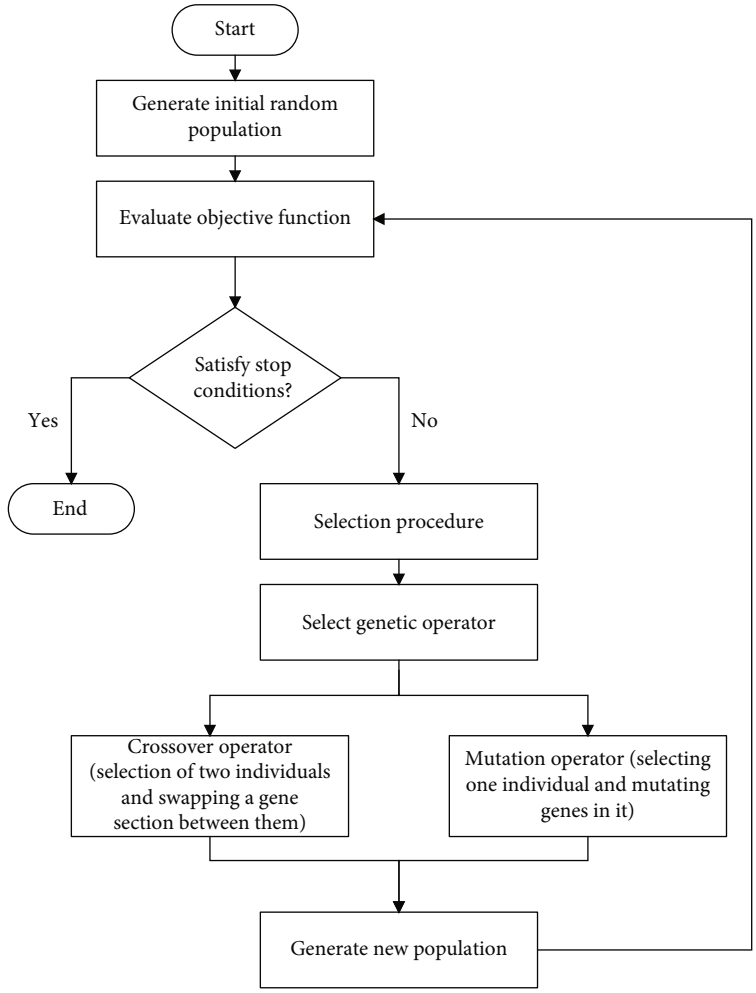

Figure 4: Genetic algorithm flow chart.

equivalent capacitance to the gain between the nodes to which the capacitor is connected. Assume that C_{in}, C_1, and C_0 are present at the gate, source, and drain terminals of the transistor T_3. Thus, these capacitances can be expressed by Miller's theorem as

$$\begin{aligned} C_{in} &= C_{gs3}(1 - A_1) + C_{gd3}(1 - A_0), \\ C_0 &= C_{gd3}\left(1 - \frac{1}{A_0}\right), \\ C_1 &= C_{gs3}\left(1 - \frac{1}{A_1}\right). \end{aligned} \tag{9}$$

3.2. Noise Figure. To determine noise performance, the low-frequency noise of all proposed circuitry components is modeled using noise voltage sources [32, 33]. The first step is to determine the gain from each noise source to the output node, i.e., V_{n0}.

The gain from V_{n2} and V_{n5} is expressed as

$$\left|\frac{V_{n0}}{V_{n2}}\right| = \left|\frac{V_{n0}}{V_{n5}}\right| = g_{m2}R_0, \tag{10}$$

where R_0 denotes the output impedance at node 0. Furthermore, the gain from V_{n3} and V_{n4} is defined as

$$\left|\frac{V_{n0}}{V_{n3}}\right| = \left|\frac{V_{n0}}{V_{n4}}\right| = g_{m3}R_0. \tag{11}$$

Using the gain factors obtained in (10) and (11), the output noise value can be expressed as

$$V_{n0}^2(f) = 2(g_{m2}R_0)^2 V_{n2}^2(f) + 2(g_{m3}R_0)^2 V_{n3}^2(f). \tag{12}$$

The obtained output noise $V_{n0}^2(f)$ can be related back to input noise $V_{neq}^2(f)$ by dividing it by the obtained gain as mentioned in (8). Thus, it is expressed as

$$V_{neq}^2(f) = \frac{2(g_{m2}R_0)^2(4kT\gamma/g_{m2}) + 2(g_{m3}R_0)^2(4kT\gamma/g_{m3})}{(-g_{m13}R_D/(1 + g_{m13}R_S))^2}, \tag{13}$$

where $V_{n2}^2(f) = 4kT\gamma/g_{m2}$ and $V_{n3}^2(f) = 4kT\gamma/g_{m3}$ refer to the power spectral density of transistors T_2 and T_3.

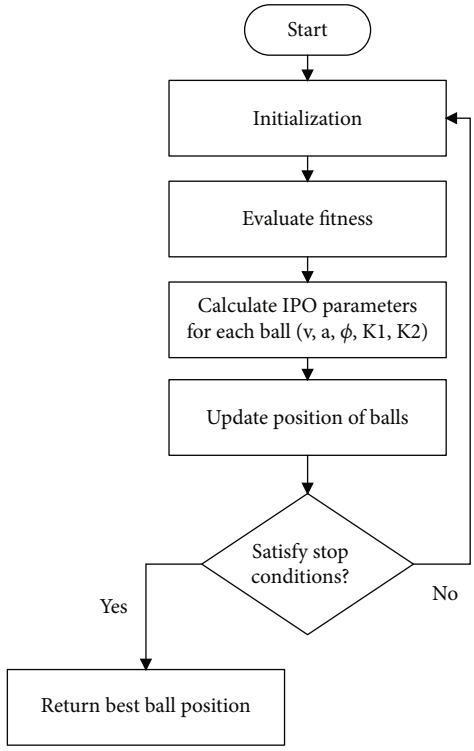

FIGURE 5: Inclined plane system optimization flow chart.

3.3. Linearity. It is essential to determine the nonlinear behavior of the mixer circuit. Based on the literature study, we found that resonant circuits are capable of enhancing linearity performance. As per conventional Gilbert mixers, harmonic generation is possible, especially due to the RF stage, because the LO stage behaves like a switch and the load stage contains passive components. Thus, the LO and load stages do not produce distortions [34]. Within the transconductance stage, the main sources of harmonics are transconductance (g_m), output conductance (g_{ds}), and gate-source capacitance (C_{gs}), where g_m is the most predominant one. Thus, the equivalent drain current of the transconductance stage is represented as a function of g_m and v_{gs}

$$i_{ds} = g_m\left(v_g - v_s\right) + g_m{}'\left(v_g - v_s\right)^2 + g_m{}''\left(v_g - v_s\right)^3 + \cdots, \tag{14}$$

where the coefficients g_m, $g_m{}'$, and $g_m{}''$ represent the transconductance, 2nd order, and 3rd order nonlinearity of transistor transconductance, respectively. Additionally, v_g and v_s refer to the gate and source voltages of the transistor. In addition, switching-stage transistors are responsible for providing parasitic components, which results in linearity degradation. Based on the above discussion, it has been found that the harmonics of the mixer depend on all transistors present within the design and parasitic component effects.

In the proposed design, a single transistor works as a mixer; therefore, the parasitic effect and g_m are equally important for the main mixer transistors, i.e., T_3 and T_4. Furthermore, the load stage also contains transistors instead of passive components, and parasitics obtained using T_3 and T_4 are balanced using the active inductor circuit.

Additionally, the circuit also includes current mirror circuits with resistive loads where the parasitic effect can be considered. Thus, the drain current i_3 through the main transistor T_3 will be dependent on load and active inductor stage transistors as well. Additionally, the harmonics will be dependent on all the transistors T_0-T_{39} within the proposed circuit.

$$i_3 = i_{L/2} + i_{I/2}, \tag{15}$$

where $i_{L/2}$ and $i_{I/2}$ refer to current flowing through load and active inductor stages, respectively.

Based on the small signal model shown in Figure 3, the total current flow through the half-mixer circuit is expressed in equation (15). Furthermore, the parasitic capacitance at node V_1 is denoted by C_P which is balanced by the active inductor circuitry. According to equation (15), the transconductance G_m of the half-mixer is expressed as

$$G_m = g_{m3} + g_{mL/2} + g_{mI/2}, \tag{16}$$

where g_{m3}, $g_{mL/2}$, and $g_{mI/2}$ refer to the transconductance of the mixing stage, load stage, and active inductor stage transistors, respectively.

3.4. Power Consumption. In general, power consumption is expressed as DC current (I_{dc}) times supply voltage.

$$P_{dc} = I_{dc} \times V_{dd}, \tag{17}$$

where I_{dc} and V_{dd} refer to DC current and supply voltage, respectively.

The proposed mixer must be able to provide high CG and good IIP3 at the expense of NF throughout the entire band of operation. Therefore, to maintain good performance, design optimization, good wideband matching, and other desired parameters must be taken into account.

4. Optimization Algorithms

Today's commercial CAD tools can only solve simulation tasks, not automatic schematic generation. With these tools, it is impossible to control circuit configurations and all design performances accurately.

The design process is time-consuming and challenging; it requires a highly skilled individual to execute it. As a result, optimizing algorithms become essential for solving such problems [35]. In the literature, different algorithms are described, such as genetic algorithm (GA), particle swarm optimization (PSO), and inclined plane system optimization (IPO) algorithms, that have been successful when implemented on analog circuits including operational amplifiers, low noise amplifiers (LNAs), and filters. However, we believe that our work is the first one to demonstrate the implementation of these algorithms on mixer circuits.

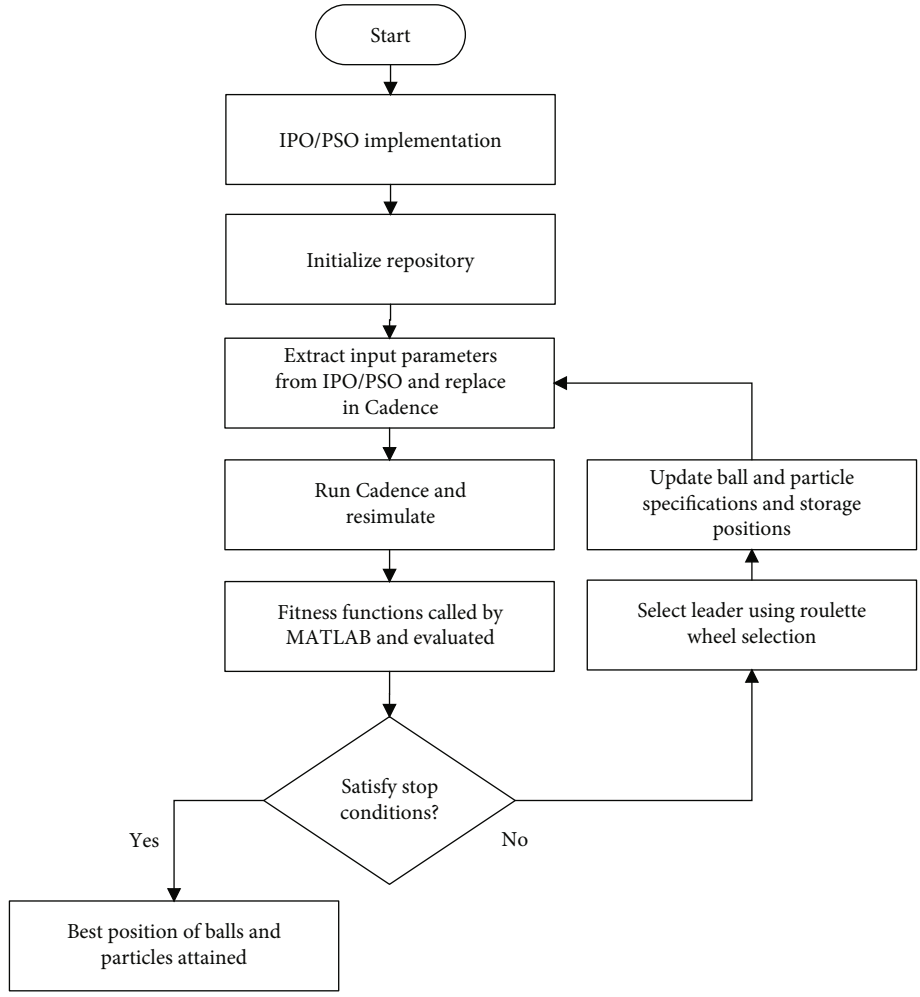

FIGURE 6: Inclined plane system optimization/particle swarm optimization flow chart.

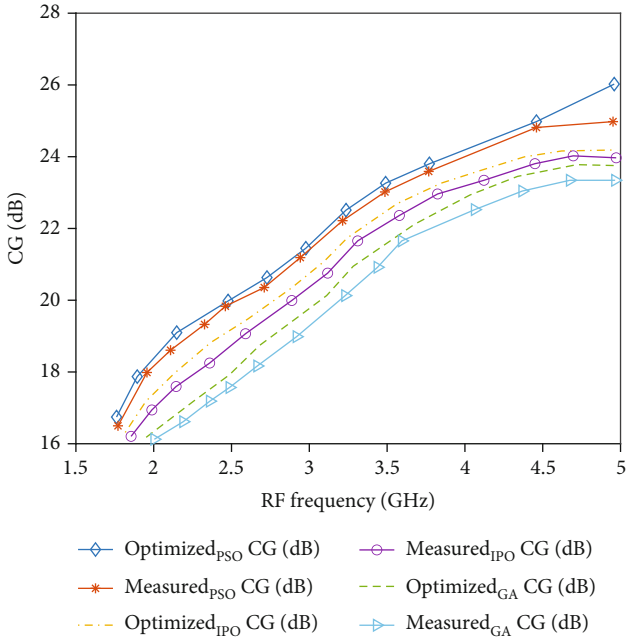

FIGURE 7: Simulated and measured conversion gain.

This section discusses all of these algorithms and the process of implementing them on the mixer circuits. Despite the differences in the implementation process, all these algorithms are aimed at improving the mixer's performance. Therefore, the algorithms are implemented one by one to see how well the proposed mixer performs under different optimizations and, additionally, how optimized results are better than unoptimized results.

The whole process is briefly explained as follows: (a) develop a high-performance reconfigurable mixer, (b) simulate using SiGe 8HP 130 nm CMOS process technology (with no optimization), and (c) implement optimization algorithms under different conditions and requirements as per algorithms and the proposed mixer. Thus, if desired conditions are met and requirements are fulfilled, then the process is completed. Otherwise, it is iterated until desired results are obtained: (d) comparison and identification of the best optimization algorithm based on the obtained results and (e) comparison of optimized and unoptimized results.

The following is a step-by-step explanation of each algorithm's implementation.

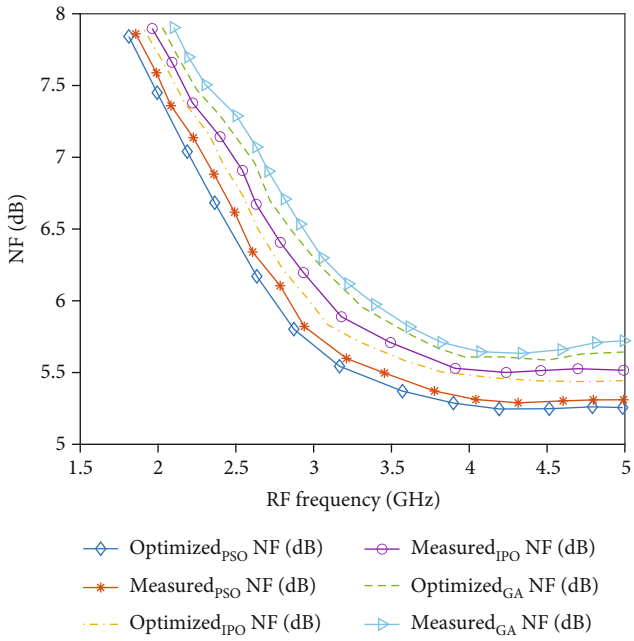

FIGURE 8: Simulated and measured noise figure.

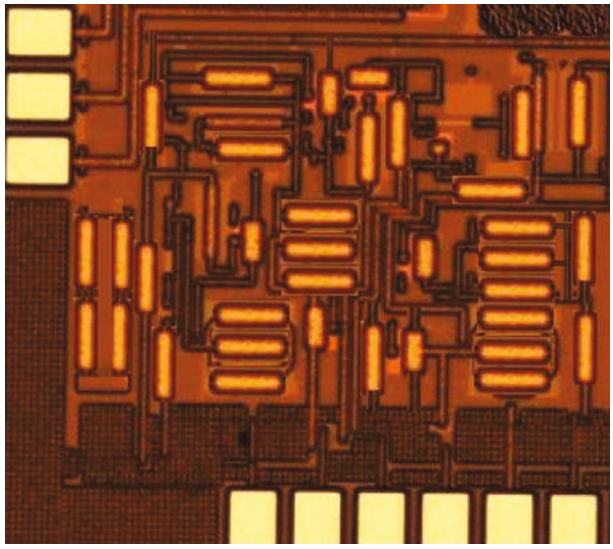

FIGURE 9: Layout of the proposed mixer.

4.1. Genetic Algorithm. In the genetic algorithm (GA), optimum parameters for a problem are obtained by following the natural evolution process. Additionally, GA works well with complex and nonlinear systems [22].

4.1.1. GA Implementation on Proposed Mixer. In this work, GA is used as a search algorithm for the optimization of various performance parameters such as CG, Pdiss, IIP3, S_{21}, S_{11}, and NF, respectively. Thus, minimization and maximization of these parameters are dependent on the values of various variables such as W/L of transistors, I_d, $C_1 - C_2$, $R_1 - R_4$, V_b, and L_1 of the proposed mixer. The implementation of this algorithm is done in MATLAB to obtain the

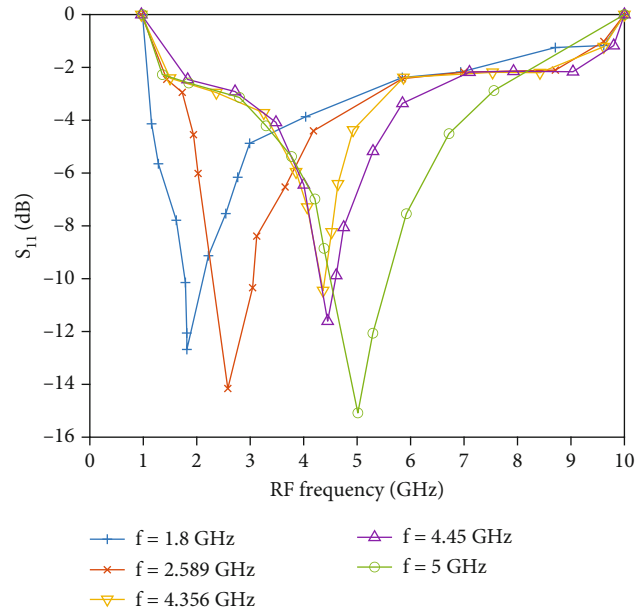

FIGURE 10: S_{11}-particle swarm optimization.

optimized values of the desired variables and subsequently satisfy the performance and specifications for the proposed design. Figure 4 depicts the flow chart which highlights the GA procedure utilized to achieve the required performance.

To start the process, the chromosome is designed to contain the variables specified above, followed by random population creation of this chromosome. Each part of this chromosome is referred to as a gene (the real value of each variable). The real value is then converted into binary code of varied and proper length.

When parameter values of the design differ in scale, adjusting the length of binary codes depends on the desired precision and range of each variable [22]. The desired values and range are as follows: (a) (C_1-C_4) pF = 0.1-6, (b) (R_1-R_4) ohms = 50-250, (c)$(W/L)_0 - (W/L)_{39} = (1 - 100)/0.13$, (d) V_b = 0.1-0.7 V, and (e)I_d = 1-20 mA; GA operators are given by (a) crossover rate ($P_c = 0.5$), (b) mutation rate ($P_M = 0.025$), and (c) number of generations = 100.

Following this, the fitness or objective function of each chromosome is obtained. As the fitness function is evaluated for more than one objective function, it is expressed as

$$F = \sum_{i=1}^{m} W_{ti} \times f_i, \tag{18}$$

where i is the object and f_i is the required value of an object. Likewise, m refers to the number of objects and W_{ti} denotes the weight coefficients of i object. Thus, the fitness function for the proposed mixer is expressed as

$$F = \frac{W_{t1} \times S_{21} + W_{t2} \times IIP3 + W_{t3} \times f}{W_{t4} \times \mathrm{NF} + W_{t5} \times \mathrm{Pdiss} + W_{t6} \times S_{11}}, \tag{19}$$

where W_{t1}-W_{t6} refer to weights corresponding to performance parameters, i.e., S_{21}, IIP3, frequency (f), NF, Pdiss,

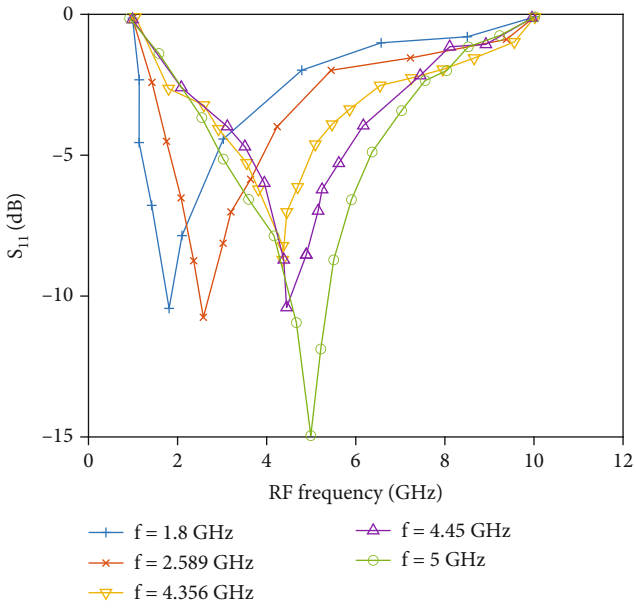

Figure 11: S_{11}-genetic algorithm.

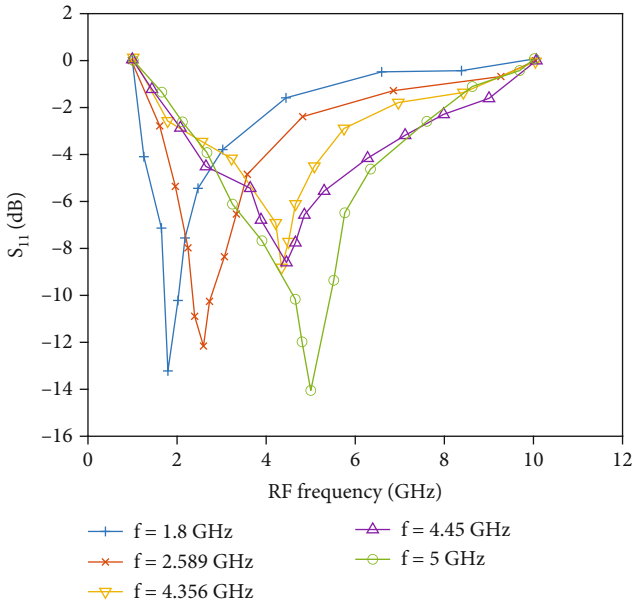

Figure 12: S_{11}-inclined plane system optimization.

and S_{11}, respectively. Weights are selected between 50 μm and 650 μm in accordance with work presented in the literature that employs a genetic algorithm to enhance overall performance. In addition, these values are most suitable for achieving the circuit's performance objectives [22]. All expressions defined in Section 3 are used for overall estimation. Once all conditions of the objective function are satisfied, the optimum results are obtained. The required information of parameters and their specified range is available in chromosomes being realized by genes that correspond to the desired variables for the proposed design. The obtained results are compared with the simulation results

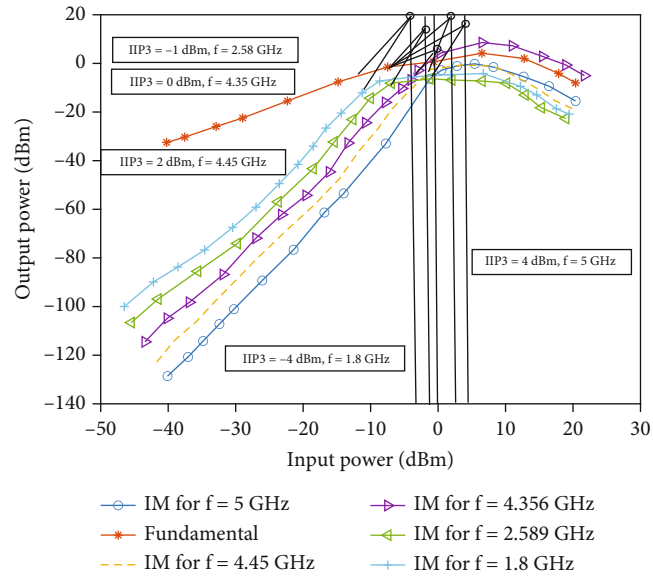

Figure 13: Measured IIP3-particle swarm optimization.

obtained before applying this algorithm. The optimized results are later compared with the results obtained from other algorithms as well.

4.2. Inclined Plane System Optimization. The inclined plane system technique is characterized by spherical objects such as balls that interact on a nonrigid, sloping surface to reach the bottom point. In this algorithm, height values are assigned to reference points for each ball based on a fitness function where potential energy is calculated at various elevations by estimating these height values. When these balls fall, their energy is converted to kinetic energy, accelerating them downward. In this way, balls begin to lose their potential energy and reach their minimum point.

In the search space, each ball is described by three coordinates: its position, its height, and its angle with other balls. The ith position of each ball is defined as

$$x_i = \left(x_i^1 . \cdots x_i^d . \cdots x_i^n\right), \quad i = 1, 2, . \cdots N, \tag{20}$$

where x_i^d refers to ith ball position within d-dimension in the n-dimensional space.

$$x_j^{\min} \le x_j \le x_j^{\max}, \quad j \le 1 \le n. \tag{21}$$

Position of ith ball is defined below:

$$\phi_{ij}^d = \left[\tan^{-1}\left(\frac{f_{j(t)} - f_{i(t)}}{x_i^d(t) - x_j^d(t)}\right)\right], \tag{22}$$

where $f_i(t)$ refers to the height of the ith ball.

Additionally, the acceleration of the ball due to inclined planes can be expressed as

$$a = g \times \sin(\phi). \tag{23}$$

Table 1: Comparison table.

Ref.	[36]	[13]	[37]	[38]	[39]	[40]	[41]	[42]	[43]	This work (S/S1/M1)	This work (S2/M2)	This work (S3/M3)
Freq. (GHz)	2.4	2.4	2.4	1-10	0.865-0.867	2.4	4-30	0.4	1-5	1.8-5	1.8-5	1.8-5
V_{dd} (V)	1.8	1.8	1.8	1.8	0.9	1.5	1.5	1.8	1.8/1.2	1.2	1.2	1.2
Pdiss (mW)	19.8	10.5	3.8	12.15	1.94	3.82	12	5.15	20	16/15	15.8	15.5
CG (dB)	12	23.7	18.3	4.5-3	26.62	14.64	-2.9-3.1	10.2	32	15-25/16.7-26/16.5-25	16.2-23.8/16.1-23.5	16.1-23/16-22.5
NF (dB)	15	11.2	12.4	20.1	6.48	7.23	Nil	6.7	3.4	6.2-8/5.3-7.8/5.2-7.79	5.4-7.7/5.35-7.78	5.6-7.9/5.65-7.8
IIP3 (dBm)	-5.5	-6	-0.9	2.7-3.8	Nil	-15.89	Nil	8.2	-12	-7–1/-5–3/-4– 4	-6–3/-5–2	-6.2–3.5/-5–2
Area (mm^2)	0.9	Nil	0.002	Nil	0.002	Nil	0.056	0.01	0.35	0.9/0.8	0.88	0.86

S: simulation results of the proposed mixer without optimization; S1: simulation results of the proposed mixer with PSO; M1: measurement results of the proposed mixer with PSO; S2: simulation results of the proposed mixer with IPO; M2: measurement results of the proposed mixer with IPO; S3: simulation results of the proposed mixer with GA; M3: measurement results of the proposed mixer with GA.

Likewise, acceleration within d-dimensional and time, t is expressed as

$$a_i^d(t) = \sum_{j=1}^{N} U\left(f_j(t) - f_i(t)\right) \times \sin\left(\phi_{ij}^d(t)\right). \tag{24}$$

Position update for the ball is possible using equation (22) as below:

$$\begin{aligned} x_i^d(t+1) = {} & k_1(t) \times \text{rand}_1 \times a_i^d(t) \times \Delta t^2 \\ & + k_2(t) \times \text{rand}_2 \times a_i^d(t) \times \Delta t^2 + x_i^d(t), \end{aligned} \tag{25}$$

where rand_1 and rand_2 refer to random constants obtained with a range of [0,1] and $k_1(t)$ and $k_2(t)$ refer to the control functions which are expressed as

$$k_1(t) = \frac{c_1}{1 + e^{((t - \text{shift}t_1) \times \text{scale}_1)}}, \tag{26}$$

where shift_1, scale_1, and c_1 are all constants.

$$k_2(t) = \frac{c_2}{1 + e^{((t - \text{shift}_2) \times \text{scale}_2)}}, \tag{27}$$

where shift_2, scale_2, and c_2 are all constants.

Finally, the speed of each ball is expressed as

$$v_i^d(t) = \frac{x_{\text{best}}^d(t) - x_i^d(t)}{\Delta t}, \tag{28}$$

where x_{best} corresponds to the ball with the lowest height.

Figure 5 depicts the flow chart which highlights the IPO procedure utilized to achieve the required performance. The following are the steps that are followed to perform this optimization: (a) The population is created randomly based on the predetermined range. (b) Population fitness (height) is determined. (c) Best balls are recorded in the external storage (record positions). (d) Every ball's position is updated; that is, all nondominant balls are placed in storage. Thus, if storage reaches a certain limit, supercubes can be created where balls can be stored according to their coordinates. (e) The supercubes with the highest number of balls are identified, and unnecessary points are randomly deleted to reduce storage capacity [20].

4.3. IPO Implementation on Proposed Mixer. For the proposed mixer, initial simulations are done in Cadence software and the results are obtained. Later, IPO is implemented to optimize the proposed mixer.

The cost function is provided below:

$$\text{CF} = \frac{\text{IIP3} \times |S_{21}| \times f}{(\text{NF} - 1) \times \text{Pdiss} \times |S_{11}|}. \tag{29}$$

Figure 6 depicts the flow chart which depicts the IPO implementation procedure, and the steps are enlisted as follows: (a) IPO implementation; (b) setting maximum iterations (Max-It) to 100 and number of balls (n_{ball}) to 30 for IPO, which is considered as an initial population; (c) the input parameters were extracted from the IPO and substituted in Cadence for subsequent simulations; and (d) all fitness functions are called by MATLAB. Once the best members have been identified, they are stored in an external list. The process continues till conditions are met. This optimization has improved the mixer's performance over that obtained using prior algorithms.

4.4. Particle Swarm Optimization. The technique is based on the behaviors of several insects and animals that cooperate in a swarm, including bees, ants, fish, and birds [24]. The vectors $\vec{v}$ and $\vec{s}$ represent the positions and velocity of the agents, respectively. By iterating the velocity (30) and position update equations (31) reported below, the modified position of the agent is realized.

$$v_i^{k+1} = W v_i^k + c_1 \, \text{rand}_1\left(\text{pbest}_i - s_i^k\right) + c_2 \, \text{rand}_2\left(\text{gbest}_i - s_i^k\right), \tag{30}$$

where v_i^k refers to the i^{th}-agent velocity at k^{th}-iteration, W is the weighting function, c_1 and c_2 are the acceleration coefficients, rand is a random number generator between 0 and 1, s_i^k is the current position of the i^{th}-agent at k^{th} iteration,

pbest_i is the pbest of agent i, and gbest is the global best of the group. Likewise, the position of each agent is expressed as

$$s_i^{k+1} = s_i^k + v_i^{k+1}. \tag{31}$$

The objective function is also optimized in this process, where all agents know their best value (pbest), their x and y positions, and the best value for a group (gbest) among the pbest values.

4.5. PSO Implementation on the Proposed Mixer: Specifications and Objectives. The proposed mixer has been designed based on PSO with an objective function as maximization of the figure of merit (FOM) of the proposed mixer. Thus, the cost function is expressed as

$$\text{CF} = \frac{\text{IIP3} \times |S_{21}| \times f}{(\text{NF-1}) \times \text{Pdiss} \times |S_{11}|}, \tag{32}$$

where IIP3, S_{21}, BW, NF, S_{11}, and Pdiss are linearity in dBm, gain in dB, BW in GHz, noise figure in dB, return loss in dB, and power dissipation in mW, respectively. It is, therefore, necessary to increase CG and IIP3 and reduce NF and power dissipation in order to maximize the objective function. An equation-based approach has been used to optimize the proposed mixer, and all the obtained expressions have been specified in Section 3.

The PSO has been implemented using MATLAB, and all the design specifications for the mixer design are as follows: (a) supply voltage = 1.2 V, (b) CG ≥ 10 dB, (c) NF ≤ 5 dB, and (d) IIP3 > 1 dBm. Similarly, the PSO specifications are given by (a) swarm size = 30, (b) iterations = 100, (c) $c_1, c_2 = 1$, and (d) $w = 0.4$. The design variables for the proposed mixer are defined as (a) (C_1-C_4) pF = 0.1-6, (b) (R_1-R_4) ohms = 50-250, (c) $(W/L)_0 - (W/L)_{39} = (1 - 100)/0.13$, and (d) V_b = 0.1-0.7 V.

The design reconfiguration is based on the variation in the bias voltage V_b corresponding to the transistors T_{21}-T_{22}. Thus, maximum power is transferred when the active inductor is fully matched with the parasitic capacitances at the IF end of the main transistors T_3-T_4. The aspect ratio (W/L) is achieved upon obtaining the g_m, V_{gs}, and V_{ds} values using basic transistor equations where mobility, gate oxide capacitance, and threshold voltage are based on 8HP CMOS process technology. Furthermore, the linearity of the mixer is highly dependent on the operating conditions of the main transistors T_3 and T_4, respectively. To attain the optimal values of CG, NF, and IIP3, the equations are represented in equations (8), (13), and (15), respectively [44].

Figure 6 depicts the flow chart which depicts the PSO implementation procedure, and the steps are enlisted as follows: (a) PSO implementation, (b) extract input parameters from PSO and replace them in Cadence, (c) run Cadence and resimulate, and (d) all fitness functions are called by MATLAB. Once the best members have been identified, they are stored in an external list. The process continues till conditions are met. This optimization has improved the mixer's performance over that obtained using prior algorithms. The optimization and measurement results are discussed in the next section.

5. Results and Discussions

The proposed mixer has been designed and fabricated using SiGe 8HP 130 nm CMOS process technology. For simulation purposes, the supply voltage is set to 1.2 V. Upon simulating the design in Cadence software, it has been found that the maximum CG reached by the design is 26 dB and IIP3 is 4 dBm. Similarly, the minimum NF at the maximum frequency is 5.3 dB. Simulation results demonstrate the validity of the mathematical models for CG, NF, and IIP3. Figure 7 depicts the comparison of CG performance upon implementation of GA, IPO, and PSO algorithms. From the plots, it has been found that the proposed mixer attained a maximum CG (after PSO) of 26 dB upon simulation, which lowered to 25 dB upon measurement. Likewise, for IPO and GA, the maximum CG are 23.5 dB and 22.5 dB, respectively. Based on the observation, it has been found that the proposed mixer attains the best results when optimized with PSO. Figure 8 depicts the comparison of NF performance upon implementation of GA, IPO, and PSO algorithms. The mixer exhibits a measured NF of 7.8 dB at 1.8 GHz and drops to 5.3 dB at 5 GHz. The simulated NF (after PSO), on the other hand, ranges from 5.3 to 7.8 dB as shown in Figure 8. Similarly, for IPO and GA, NF is within the range of (5.4-7.7)dB and (5.6-7.9)dB, respectively. Based on the observation, it has been found that the proposed mixer attains the best results when optimized with PSO in terms of NF. Variation can be observed in the simulated and measured results, due to inaccuracy of the transistors, parasitic capacitance effect, and use of external baluns. The proposed design is also fabricated and tested. The chip die microphotograph is shown in Figure 9 which covers an area of 0.8 mm^2. For chip evaluation purposes, external baluns were used with an input-matching network present at the RF and LO ports, respectively. Additionally, an output buffer of 0 dB gain was also used. On wafer, S_{11} measurements were made while fixing the LO frequency of 2 GHz for proposed mixer's performance measurement purposes. Thus, with the variation in the RF frequency from 1.8-5 GHz, the measured return loss (S_{11}) PSO was plotted as shown in Figure 10. Upon observation, it has been found that the simulated and measured S_{11} are better than 10 dB within the entire band of operation. Likewise, results for S_{11} after IPO and GA optimization are shown in Figures 11 and 12. Additionally, the mixer operates at 1.2 V while consuming a low power of 15 mW while maintaining an IIP3 of 4 dBm (after PSO), as shown in Figure 13. Table 1 depicts the performance comparison summary of the proposed mixer (with and without optimization) with the other works reported in the literature which employed active inductor technique within their proposed circuit. Upon comparison, it has been noticed that the proposed mixer attains good CG and reasonable IIP3 while covering a small area but at the expense of NF.

6. Conclusion

This paper proposes a novel reconfigurable downconversion mixer. The use of an active inductor at the load end of the main mixing transistors is the mechanism used to maintain a high gain while improving the linearity. PSO, IPO, and GA have been used to optimize the proposed mixer. Upon optimization and comparison, the best results have been obtained when optimized using PSO. The measurement results after PSO implementation showed a conversion gain of 25 dB, as well as an IIP3 of 4 dBm at the expense of NF of 5.2 dB.

Data Availability

The article contains all the data

Disclosure

A part of this study has been presented in PhD thesis (https://openrepository.aut.ac.nz/server/api/core/bitstreams/5a18 331a-475f-87a2-40f1c43f6fb9/content).

Conflicts of Interest

The authors declare no conflict of interest.

Acknowledgments

The authors would like to thank Auckland University of Technology for providing them with opportunities to conduct research and contributions to this study. Open access publishing was facilitated by Auckland University of Technology, as part of the Wiley-Auckland University of Technology agreement via the Council of Australian University Librarians.

References

[1] P. Cruz, N. Carvalho, and K. Remley, "Designing and testing software-defined radios," *IEEE Microwave Magazine*, vol. 11, no. 4, pp. 83–94, 2010.

[2] H. Zhang, S. Tang, M. Cai, and Y. Jiang, "Optimal design of CMOS mixer: a research review," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 32, no. 12, p. 19, 2022.

[3] B. Asad, *Low-Noise 24 GHz 0.15μm GaAs pHEMT Gilbert Cell Mixer for Intelligent Transportation System Radar Receiver, [M.S. Thesis]*, Ottawa-Carleton Institute for Electrical and Computer Engineering, Electrical and Computer Engineering, Ottawa, ON, Canada, 2014.

[4] E. Altuner, I. Ozoguz, and M. Yelten, "High-linearity Gilbert-cell mixer design for cryogenic applications," *Analog Integrated Circuits and Signal Processing*, vol. 113, no. 2, pp. 249–256, 2022.

[5] T. Li, F. Huang, Y. Wang, and X. Hu, "A high linearity reconfigurable down-conversion mixer for dual-band applications," in *2010 International Symposium on Signals, Systems and Electronics*, pp. 1–4, Nanjing, China, 2010.

[6] A. Othman, R. Barrak, and M. Mabrouk, "A tunable RF filter for multistandard GSM/UMTS/WiFi/LTE receiver," in *Proceedings of 2014 Mediterranean Microwave Symposium (MMS2014)*, pp. 1–5, Marrakech, Morocco, 2014.

[7] M. I. Ahmed, M. S. Sultan, and S. Azeemuddin, "A novel CMOS current bleeding mixer based on inductive degeneration," in *2013 International Conference on Signal Processing and Communication (ICSC)*, pp. 82–85, Noida, India, 2013.

[8] J. Chung and A. A. Iliadis, "Modeling a high linearity, low noise Gilbert cell mixer using three optimization techniques," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 790–793, Springfield, MA, USA, 2020.

[9] H. Zhang and E. Sánchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: a tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 22–36, 2011.

[10] J. Yoon, H. Kim, C. Park et al., "A new RF CMOS Gilbert mixer with improved noise figure and linearity," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 3, pp. 626–631, 2008.

[11] M. H. Kashani, M. Asghari, M. Yavari, and S. Mirabbasi, "A +7.6 dBm IIP3 2.4-GHz double-balanced mixer with 10.5 dB NF in 65-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 10, pp. 3214–3218, 2021.

[12] M. A. Raheem and M. M. S. Hussain, "A low voltage NMOS current bleeding down conversion mixer with source degeneration in 0.18μm CMOS technology," in *2021 Devices for Integrated Circuit (DevIC)*, pp. 637–642, Kalyani, India, 2021.

[13] H. Kia and A. A'ain, "A high gain and low flicker noise CMOS mixer with low flicker noise corner frequency using tunable differential active inductor," *Wireless Personal Communications*, vol. 79, no. 1, pp. 599–610, 2014.

[14] F. Soleymani, P. Amiri, and M. H. Maghami, "A 0.3–5 GHz, low-power, area-efficient, high dynamic range variable gain low-noise amplifier based on tunable active floating inductor technique," *International Journal of Circuit Theory and Applications*, vol. 49, no. 10, pp. 3230–3247, 2021.

[15] S. Zandian, H. Khosravi, A. Bijari, and N. Kandalaft, "Design of A 2-3 GHz down-conversion active mixer with improved linearity," in *2020 10th Annual Computing and Communication Workshop and Conference (CCWC)*, pp. 0463–0468, Las Vegas, NV, USA, 2020.

[16] D. Na and T. W. Kim, "A 1.2 V, 0.87–3.7 GHz wide-band low-noise mixer using a current mirror for multiband application," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 2, pp. 91–93, 2012.

[17] J. Manjula, "Performance analysis of 1.8 GHz to 5 GHz HEMT multiband mixer," *International Journal of Applied Engineering Research*, vol. 11, pp. 6312–6317, 2016.

[18] C. S. Lin, P. S. Wu, H. Chang, and H. Wang, "A 9–50-GHz Gilbert-cell down-conversion mixer in 0.13-/spl mu/m CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 5, pp. 293–295, 2006.

[19] J. Y. Lee, J. Y. Park, and T. Y. Yun, "Flicker noise improved CMOS mixer using feedback current bleeding," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 8, pp. 730–732, 2017.

[20] A. Bijari, S. Zandian, and M. Ebrahimipour, "Optimum design of a new ultra-wideband LNA using heuristic multiobjective optimization," *Journal of Computational Electronics*, vol. 19, no. 3, pp. 1295–1312, 2020.

[21] B. Liu, F. Fan, H. Zhang, and C. Zeng, "A wideband down conversion mixer with dual cross-coupled loops for software defined radio," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 990–993, Lisbon, Portugal, 2015.

[22] A. T. Younis and E. A. Abdo, "Low noise amplifier (LNA) performance optimization using genetic algorithms (GAS)," *Journal of Engineering Science and Technology*, vol. 15, no. 5, pp. 3122–3131, 2020.

[23] R. Kumar, F. A. Talukdar, A. Rajan, A. Devi, and R. Raja, "Parameter optimization of 5.5 GHz low noise amplifier using multi-objective firefly algorithm," *Microsystem Technologies*, vol. 26, no. 10, pp. 3289–3297, 2020.

[24] M. Kumar and V. K. Deolia, "Performance analysis of low power LNA using particle swarm optimization for wide band application," *AEU-International Journal of Electronics and Communications*, vol. 111, article 152897, pp. 1–9, 2019.

[25] S. Shukla, "Qualitative analysis of high gain small- signal amplifier with MOSFET current mirror," *International Journal of Applied Engineering Research*, vol. 14, no. 1, pp. 55–61, 2019.

[26] H. Xiao and R. Schaumann, "A 5.4-GHz high-Q tunable active-inductor bandpass filter in standard digital CMOS technology," *Analog Integrated Circuits and Signal Processing*, vol. 51, no. 1, pp. 1–9, 2007.

[27] M. Bhuiyan, J. Chew, M. B. I. Reaz, and N. Kamal, "Design of an active inductor based LNA in Silterra 130 nm CMOS process technology," *Informacije Midem-Ljubljana*, vol. 45, pp. 188–194, 2015.

[28] F. Yuan, *CMOS active inductors and transformers: principle, implementation, and applications*, Springer, 2008.

[29] H. Kia and A. A'Ain, "A single-to-differential LNA using differential active inductor for GPS applications," *Frequenz*, vol. 67, no. 1-2, pp. 27–34, 2013.

[30] H. B. Kia, A. K. A'ain, I. Grout, and I. Kamisian, "A reconfigurable low-noise amplifier using a tunable active inductor for multistandard receivers," *Circuits, Systems, and Signal Processing*, vol. 32, no. 3, pp. 979–992, 2013.

[31] D. P. Patel, *CMOS active inductor and its applications*, Intech Open, 2019.

[32] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, Wiley, United States of America, 2012.

[33] B. Razavi, *RF Microelectronics*, Pearson Education, United States, 2012.

[34] B. Gilbert, "The MICROMIXER: a highly linear variant of the Gilbert mixer using a bisymmetric class-AB input stage," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 9, pp. 1412–1423, 1997.

[35] L. I. Babak, A. A. Kokolov, A. A. Kalentyev, and D. V. Garays, "A new genetic-algorithm-based technique for low noise amplifier synthesis," in *2012 7th European Microwave Integrated Circuit Conference*, pp. 381–384, Amsterdam, Netherlands, 2012.

[36] M. A. Abdelghany, R. K. Pokharel, H. Kanaya, and K. Yoshida, "Flicker noise reduction in RF CMOS mixer using differential active inductor," *Microwave and Optical Technology Letters*, vol. 53, no. 11, pp. 2553–2556, 2011.

[37] A. K. Hota and K. Sethi, "Pseudo-differential active inductor-based modified Gilbert cell mixer," *Iranian Journal of Science and Technology, Transactions of Electrical Engineering*, vol. 46, no. 1, pp. 245–256, 2022.

[38] D. Bhatt, "Design of wideband active mixer by using an active inductor," in *2019 IEEE Asia-Pacific Microwave Conference (APMC)*, pp. 1173–1175, Singapore, 2019.

[39] D. Shukla, S. K. Gupta, V. Bhadauria, and R. Tripathi, "An inverter amplifier with resistive feedback current mirror Gilbert mixer," *International Journal of Electronics*, vol. 110, no. 2, pp. 221–244, 2023.

[40] S. H. Pang, Y. Kim, and T. Y. Yun, "High-gain, low-power, and low-noise CMOS mixer using current-reused bleeding amplification," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 5, pp. 418–421, 2022.

[41] J. Kim, "A wideband and low-power distributed cascode mixer using inductive feedback," *Sensors*, vol. 22, no. 22, p. 9022, 2022.

[42] E. Yesil, O. Ferhanoglu, and M. Yelten, "An ISM-band direct down-conversion double-balanced mixer for biomedical applications," *Analog Integrated Circuits and Signal Processing*, vol. 113, no. 2, pp. 231–239, 2022.

[43] B. Guo, H. Wang, H. Wang, L. Li, W. Zhou, and K. Jalali, "A 1–5 GHz 22 mW receiver frontend with active-feedback baseband and voltage-commutating mixers in 65 nm CMOS," *IET Circuits, Devices & Systems*, vol. 16, no. 7, pp. 543–552, 2022.

[44] S. Mehta, *Reconfigurable Mixer Design for Software-Defined Radios, [Ph.D. Thesis]*, Auckland University of Technology, Auckland, New Zealand, 2022.