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RESEARCH ARTICLE

Achieving Reduced Sizing for Shunt Active Power Filters: A Design Leveraging Load Impedance Analysis and Conservative Power Theory

JOÃO HENRIQUE DE OLIVEIRA[1], (Member, IEEE), JOSEPH KIRAN BANDA[2], (Member, IEEE), AND ELISABETTA TEDESCHI[1,3], (Senior Member, IEEE)

[1]Department of Electric Energy, Norwegian University of Science and Technology (NTNU), 7034 Trondheim, Norway
[2]SINTEF Energy Research, 7465 Trondheim, Norway
[3]Department of Industrial Engineering, University of Trento, 38122 Trento, Italy

Corresponding author: João Henrique de Oliveira (joao.h.de.oliveira@ntnu.no)

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ABSTRACT The growing integration of power electronics in industrial systems has led to the widespread adoption of variable frequency drives, most of which are powered by 6-pulse diode bridge rectifiers combined with large DC-link capacitors. While this configuration ensures a stable voltage supply for IGBT-based motor drives, it also behaves as a non-linear voltage-source load that injects substantial harmonic distortion into the grid. Conventional mitigation strategies often involve shunt active power filters (SAPFs), but when improperly dimensioned, these filters can end up requiring power ratings nearly as large as the load itself—rendering them impractical for many applications. This paper introduces a streamlined design approach aimed at minimizing the size and rating of SAPFs and associated passive elements for typical rectifier-capacitor-fed induction motor systems. A key part of this approach is the use of one-cycle power components, based on Conservative Power Theory (CPT), both in the filter design and its control. The effectiveness of the proposed strategy is demonstrated through comprehensive PLECS simulations and real-time hardware-in-the-loop experiments. The results demonstrate the effectiveness of the proposed approach. By selecting a load impedance value of 4.5%, which is lower than the 6% commonly recommended in the literature, good performance is achieved in terms of low harmonic distortion and reduced current ripple in the grid current.

INDEX TERMS Compensation strategy, conservative power theory (CPT), FACTS, harmonics, power quality, shunt active power filter (SAPF).

I. INTRODUCTION

Electric motors are widely used in industry to move loads, which are often rotating loads. Traditionally, mostly dc motors were used, which were fed through either diode bridges or thyristor-controlled rectifiers. However, with the advancement of the semiconductor industry and the improved robustness, efficiency, and reliability of ac drives, IGBT-based ac drives are progressively replacing dc drives. These new drives are typically connected to the grid through low-cost 6-pulse uncontrolled diode bridge rectifiers with a bulky capacitor on the dc link to create a constant voltage. This constant voltage is connected to IGBT-based voltage source converters which drive the motors using either voltage/frequency control or field-oriented control (FOC) techniques. These loads inject undesired harmonics into the upstream grid, and in some cases this can result in significant penalties from utilities, hence they have to be compensated. In particular, diode bridge rectifiers of this type are voltage source type of loads, whereas rectifiers

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that feed large inductances are known as current source types. To compensate for harmonics from any of the two types, passive filters are the simplest and least expensive solution. However, their drawbacks such as: bulky size, resonance issues due to network parameters' changes and de-tuning with aging are now establishing active power filters as strong competitors, as the cost of semiconductors is decreasing and the computation power of micro-controllers increasing. To minimize the size of the compensation system, it is recommended to connect the active filter in shunt for the current source type-loads and in series for the voltage source types [1]. However, series connection of active filters requires transformers, which is sometimes avoided. Ready-to-use converters directly connected in shunt at the rectifier terminals are preferred. Many publications in the literature have considered a shunt active power filter (SAPF) to compensate harmonics originated from a voltage source type non-linear load, resulting in the connection of a SAPF whose size is close to that of the rectifier itself. Reference [2] provides an overview of active filter topologies, control strategies, and design considerations. In [3], the rating and sizing of shunt and series active power filters are analyzed, highlighting their suitability for compensating harmonic current and voltage sources. Reference [4] addresses conducted electromagnetic interference by proposing a soft-switching-based active power filter design. Finally, [5] reviews hybrid filter configurations, their control approaches, and application trends, emphasizing their role in practical power quality enhancement. Also, the bulky capacitor on the dc link of the standard active filter offers very limited impedance to SAPF injected currents, and hence over-currents through the rectifier may emerge, which flow into the load and are sensed back again by the SAPF itself to be compensated [6]. To avoid this, typically a load impedance around 6% is included between the SAPF and rectifier terminals, which can occupy large space and increase the overall capital cost [7]. The first contribution of this paper is a detailed analysis and the consequent derivation of a methodology to reduce the sizing of SAPF and load impedance with the maximum possible attenuation of harmonics at the source side.

Recent years have witnessed significant advancements in SAPF control strategies. Model Predictive Control (MPC) has emerged as a promising technique due to its fast dynamic response and ability to handle system nonlinearities. In [8], an MPC strategy with Lyapunov-based stability guarantee is proposed. Similarly, [9] presents an adaptive neural network topology using ADALINE networks for fundamental signal extraction. Proportional-resonant (PR) controllers have also received considerable attention. The authors of [10] propose a genetic algorithm-optimized PR controller. Reference [11] introduces a dispersing quasi-proportional resonance (QPR) controller with leading phase compensation that integrates harmonic detection and control into a single current closed-loop, eliminating complex harmonic detection algorithms. Reference [12] addresses stability challenges of LCL-filtered resistive-active power filters through passivity-based controller design, proposing an innovative calculation method for compensation angles of resonant controllers. The impact of semiconductor technology selection on SAPF performance has also been investigated. The authors of [13] present analytical models for evaluating losses in SAPFs, demonstrating that SiC-based solutions achieve significantly lower losses (48.2 W vs 207 W at 16 kHz) and enable higher switching frequencies. Alternative control approaches have been explored as well. Reference [14] analyzes reduced-order generalized integrator (ROGI) based SAPF under both current-fed and voltage-fed nonlinear loading conditions. The authors of [15] present a practical implementation using harmonic component separation method with low-pass filter on an Field-Programmable Gate Array (FPGA) platform. Reference [16] proposes a dual fundamental component extraction algorithm using self-tuning filters for a three-level Neutral Point Clamped (NPC) inverter-based SAPF, demonstrating effective operation under nonideal grid voltage conditions without requiring phase-locked loop elements.

For the control of SAPF, many power theories both in the time and frequency domains have been used to generate current references [2]. Conservative Power Theory (CPT) is one of the time domain power theories that have been widely discussed and applied to shunt active power filters in the last two decades. Reference [17] presents the CPT as a suitable framework for power quality analysis in smart microgrids operating under non-ideal conditions. Reference [18] applies CPT-based current decomposition to cascaded multilevel converters for selective harmonic compensation. Reference [19] investigates CPT as a control algorithm for shunt active power filters with experimental validation. Reference [20] addresses active power filtering using CPT under distorted voltage conditions. Reference [21] compares CPT with PQ-theory (also know as: Instantaneous Power Theory [22]), which calculates instantaneous powers in the $\alpha\beta$ domain to generate compensation currents, and the DQ (Synchronous Reference Frame Method), which uses a synchronous reference frame to control current components in steady state, for shunt active compensation in terms of performance and dynamic behavior. The penetration of the CPT theory into domestic and industrial power quality compensators has increased in the last years [23], due to the following reasons: 1) The implementation of CPT does not need a phase-locked loop (PLL) with source voltage. This helps to avoid low pass filters or advanced PLL techniques to eliminate the harmonics in the voltage caused by the non-linear load that needs to be compensated by the active filters. Although low-pass filters are widely used to filter out harmonics in the source voltage measurement, they can introduce delays in the reference current generation to the SAPF. 2) CPT decomposes the source current into orthogonal components and it is effective in identifying and selecting the components that need to be compensated with the SAPF. In this paper we use the generated reference currents by the CPT not only to control the SAPF, but also to design the

power circuit components. This manuscript is an extended and enhanced version of the conference paper [24]. While both works share the same fundamental transfer-function formulation, the present journal article expands the theoretical analysis by introducing an inverse inductance estimation method based on numerical interpolation, a closed-loop sensitivity study, and the identification of a saturation effect that provides a rigorous justification for the selected inductance range. In addition, the work advances from a purely simulation-based evaluation to a comprehensive experimental validation using controller hardware-in-the-loop (CHIL) tests with an external Digital Signal Processor (DSP), operating as the controller hardware, implementing the complete shunt active power filter control in real time. This includes CPT-based signal processing, hysteresis current control, DC-link voltage regulation, and real-time PWM generation. Finally, the extended analysis yields more accurate and experimentally grounded performance metrics, thereby transforming the original conceptual study into a validated engineering design methodology. The structure of this paper is as follows: Section II describes the studied system; Section III shows how to use the transfer function approach to size the required inductance between the SAPF and the rectifier; Section IV introduces the CPT; Section V presents the use of one-cycle CPT-decomposed current components for the design of the SAPF; Section VI presents the simulation results; Section VII discusses the experimental results; and Section VIII concludes the paper.

II. SYSTEM DESCRIPTION

The test case under analysis is a low voltage (LV) drive with a 6-pulse diode rectifier in the front end as shown in Fig. 1. It is connected to the medium voltage grid through a star-delta transformer T_1 whose primary and secondary voltages are rated as 3 kV and 690 V, respectively [25]. The short circuit MVA of the grid before the transformer is SCMVA = 200 MVA. To reduce the harmonic currents that the drive injects into the grid, typically an ac choke is placed either in front of the diode rectifier or in the dc link. For the given system, an ac choke whose inductance is 2.5% is placed between the diode bridge rectifier and the transformer T_1, marked as L_{ac} in Fig. 1.

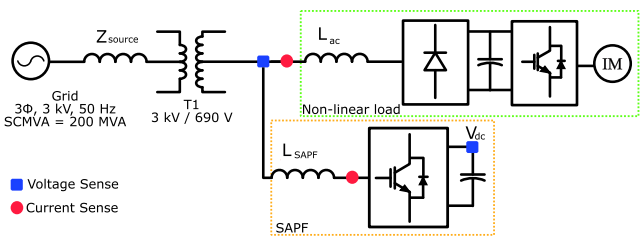

FIGURE 1. System configuration: 500 kW induction motor drive with a diode rectifier as the front end.

The motor drive load is connected to the dc link through an IGBT-based voltage source converter, which operates under closed-loop field-oriented control, causing it to behave like a constant power load, so that variations in the source voltage do not reflect into the drive. All the grid, transformer and rectifier parameters, as well as related base values, are tabulated in Table 1.

According to the *IEEE Std 519-2014*, harmonic distortion levels must be controlled to ensure power quality and equipment protection. The Total Harmonic Distortion (THD) is a measure of signal distortion that indicates how much the harmonics in a signal deviate from the original. For voltage distortion at the Point of Common Coupling (PCC), the standard sets a maximum THD of 5% for systems with voltages below 69 kV. Regarding current distortion, IEEE 519 defines limits based on the ratio between the load current and the short-circuit current at the PCC. For example, when the ratio I_L/I_{SC} is less than 20, the maximum allowable THD for current is 5%, increasing up to 20% for weaker systems where this ratio exceeds 1000. These limits are intended to minimize the impact of nonlinear loads and ensure compatibility between utility and customer systems [26].

The impact of a choke on the harmonic distortion is first studied to verify if it is possible to address the problem without any additional passive or active filtering component. From Table 2, it can be seen that even if 3 chokes are placed in series (total inductance of 7.5%), the THD in current and voltage has only reduced to 22.9% and 6.1%, respectively. This highlights the need for filtering options other than series chokes to reduce the harmonic distortion resulting from this voltage source type of non-linear load to an acceptable level.

III. SHUNT ACTIVE POWER FILTER FOR VOLTAGE SOURCE TYPE NON-LINEAR LOAD

This section uses the transfer function approach presented in [7] to size the required inductance between the SAPF and the rectifier, considering the drive working at full load. The detailed and simplified schematics of the considered system are shown in Fig. 2. It can be seen that the SAPF is denoted as a current source I_{sapf}, whereas the voltage source type non-linear load is shown as a harmonic voltage source V_{load}. In Fig. 2 the total source impedance, including the medium-voltage grid and the transformer referred to the base voltage of 690 V, is denoted as Z_{source_tot}, while the impedance between the SAPF connection point and the rectifier terminals is represented as Z_{load}, which is predominantly inductive and can be approximated as $Z_{load} \approx j2\pi f_{base} L_{ac}$.

From Fig. 2, it can be written:

$$V_{source} - (I_{source} \cdot Z_{source\_tot}) = V_{load} + I_{load} \cdot Z_{load}, \quad (1)$$

$$I_{source} + I_{sapf} = I_{load}, \quad (2)$$

$$I_{source} = \frac{V_{source} - V_{load}}{Z_{source\_tot} + \frac{Z_{load}}{1-k}}, \quad (3)$$

where V_{source} is the voltage source, I_{source} is the current source, I_{load} is the load current, and k is the transfer function

TABLE 1. 500 kW AC motor drive system parameters.

Parameter	Value
Grid Parameters	3 kV, 50 Hz, Short Circuit MVA = 200 MVA
Transformer T_1	YD1, 3 kV / 690 V, X_{T1} = 6%
Motor Drive Load	500 kW
DC Bus Capacitance C_{dc}	7.9 mF
Choke Inductance L_{ac}	75 µH (2.5% or 0.025 pu)
Base Power P_{base}	500 kW
Base Voltage V_{base}	690 V
Base Frequency f_{base}	50 Hz
Base Impedance Z_{base}	0.95 Ω

TABLE 2. Harmonic distortion indices with L_{ac}.

Choke inductance L_{ac}	THD_I	THD_V
75 µH (2.5%)	30.1%	7.9%
150 µH (5%)	25.85%	6.8%
225 µH (7.5%)	22.9%	6.1%

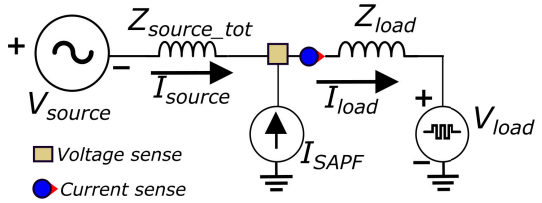

FIGURE 2. Simplified schematic of system with SAPF.

which represents the compensation capability of the active filter. In other words, k can be written as:

$$k = \frac{I_{\text{SAPF}}}{I_{\text{load}}}, \tag{4}$$

considering all the variables in the above equations in per unit, the magnitude of k at the fundamental frequency is supposed to be zero, and, for all the harmonics, its magnitude should be 1.0 to leave the fundamental current component unaffected for full harmonic removal, but can typically vary between 0.7 to 0.9 based on the computation of harmonic references, delay time of the sensing, controller and power converter itself. The necessary condition to eliminate the harmonics from the source current produced by a voltage source type non-linear load is:

$$\left|\left(Z_{\text{source\_tot}} + \frac{Z_{\text{load}}}{1-k}\right)\right| \gg 1.0\,\text{pu}. \tag{5}$$

For obvious reasons, $Z_{\text{source\_tot}}$ is typically not a designer choice to manipulate the harmonic magnitude in (5), thus Z_{load} is chosen as the factor that can be directly influenced by the use of the SAPF. The influence of Z_{load} on the attenuation of the harmonics in the source current by the SAPF can be seen by obtaining the bode plot for the below-simplified transfer function when $V_{\text{source}} = 0$.

$$\left|\frac{I_{\text{source}}}{V_{\text{load}}}\right| = |A| = \left|\frac{2\cdot\pi\cdot f_{\text{base}}}{Z_{\text{source\_tot}} + \frac{Z_{\text{load}}}{1-k}}\right|. \tag{6}$$

The simplified transfer function of k in the continuous domain used in (6) is represented as given in (7).

$$k(s) = G\cdot\left(\frac{s\cdot\tau_{\text{HP}}}{1+s\cdot\tau_{\text{HP}}}\right)\cdot\left(\frac{1}{1+s\cdot\tau_{\text{delay}}}\right), \tag{7}$$

where G is the gain of the SAPF and typically varies between 0.9 to 1.1 (chosen as 0.99), $\tau_{\text{HP}} = 30$ Hz is the cut-off frequency of the high pass filtering action performed by the harmonic current reference extraction algorithm. $\tau_{\text{delay}} = 20\,\mu$s represents the delay incurred in the computation and execution of the control algorithm in the modern digital signal processors. Although the above analysis holds independently of the control algorithm used to generate the SAPF current reference, in this paper we analyze the use of CPT theory.

A. IMPACT OF L_{AC} ON THE FREQUENCY RESPONSE

The inductance L_{ac} plays a critical role in shaping the magnitude and phase response of (6). As L_{ac} increases, the term $\frac{Z_{load}}{1-k(s)}$ becomes more dominant in the denominator. This results in:

- A stronger low-pass filtering effect, reducing the system's bandwidth.
- A phase lag that increases with frequency, due to the higher reactive impedance introduced by L_{ac}.

The bode plots of (6) and (7) are shown in Fig. 3 with varying load impedance. Dashed lines in gain and phase plots show the frequency response of SAPF based on (7). With the existing $Z_{\text{load}} = 2.5\%$, clearly the harmonic attenuation in the source current is not good at the low frequencies which are dominant. Additionally with such low value of Z_{load}, and the bulky dc link capacitance adding very limited impedance to the harmonic currents injected by SAPF, there is overcurrent through the diode rectifier which will be sensed back by the SAPF and compensated. This requires a higher SAPF rating for this type of load. On the other hand, the generalized thumb rule suggests maintaining a load impedance of at least 6% to 7%, assuming a source impedance of $\leq 2\%$ [27], [28], [29], [30], [31]. However, in the minimal sizing design of the considered system, the transformer impedance, which can itself be around 6% to 7%, must also be included as part of the source impedance. As a result, the required load impedance can be reduced to approximately 4.5%. This can be seen from Fig. 3. Even with a 4.5% load impedance, a good attenuation at all the necessary harmonics in the source current is seen. These findings are validated in the following sections, along with the implementation of the CPT-based SAPF, that aims to produce no overcurrent in the diode bridge rectifier.

In summary, L_{ac} directly controls the trade-off between filtering capability and dynamic performance. Larger values improve filtering but reduce bandwidth and phase margin, while smaller values increase responsiveness but may allow higher-frequency components to propagate.

B. INVERSE CALCULATION: ESTIMATING L_{AC} FROM MEASURED MAGNITUDE $|A|$

In practical scenarios, it may be necessary to estimate the inductance L_{ac} from measured magnitudes of A. Since equation (6) does not have a closed-form inverse for L_{ac}, numerical interpolation is employed.

Given a fixed frequency and a vector of magnitude values $|A|$ obtained from the direct calculation, we find the corresponding Z_{load} values by linear interpolation, thus obtaining the inverse relationship:

$$Z_{load} = g^{-1}(|A|), \tag{8}$$

where g represents the mapping defined by the direct calculation.

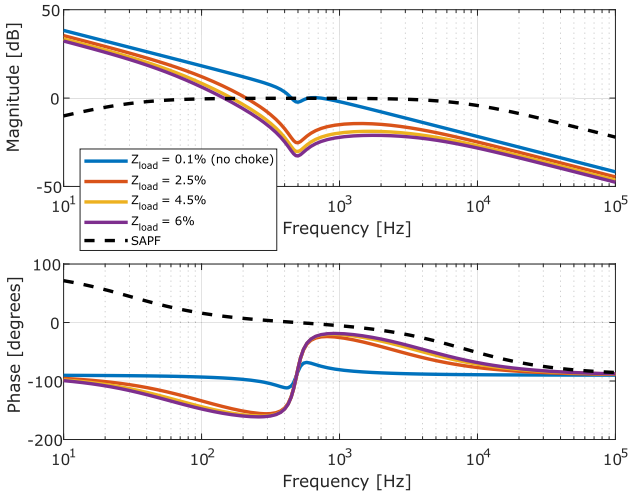

FIGURE 3. Frequency response of source current over load voltage for different Z_{load}, and SAPF.

C. INFLUENCE OF CHOKE INDUCTANCE L_{AC} ON THE CLOSED-LOOP TRANSFER FUNCTION

Fig. 4 relates the variation of $|A|$ in dB with respect to Z_{load} for several frequencies. For fixed frequencies f in the set $\{50, 250, 350, 550, 650\}$ Hz, the magnitude of A is computed over a range of loads. This step allows us to observe how changes in L_{ac} (and consequently in Z_{load}) affect the system response at different operating frequencies.This behavior indicates that the influence of L_{ac} diminishes as frequency increases after the inflexion point around 500 Hz shown in Fig. 3, which contrasts with the intuitive expectation based solely on the increasing reactance of inductors with frequency.

The key factor explaining this behavior lies in the frequency-dependent feedback gain $k(s)$. At low frequencies, $k(s) \approx 0$, and the term $\frac{Z_{load}}{1-k(s)} \approx Z_{load}$, so the inductor's effect appears directly in the transfer function. Additionally, the dynamics of the filters used in the feedback path (a high-pass filter and a delay) shape the overall response, resulting in a saturation effect that limits the variation in A even with larger values of Z_{load}.

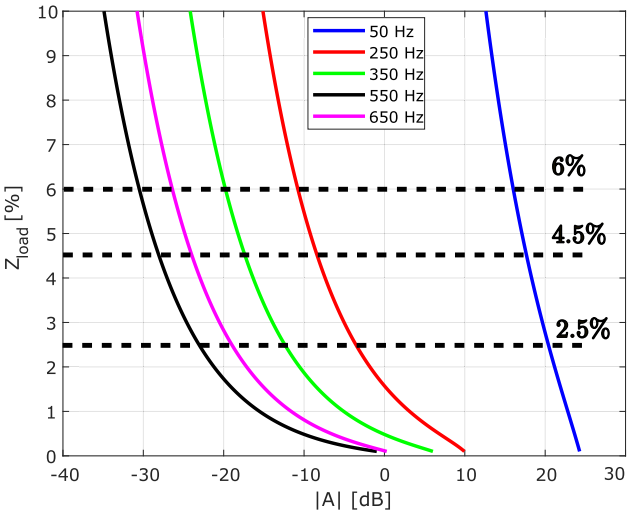

FIGURE 4. Load impedance Z_{load} (in pu) as a function of the closed-loop transfer function magnitude $|A|$ in dB, for several discrete frequencies.

These results highlight that choke inductance tuning is more critical at lower frequencies, where its impact on the closed-loop dynamics is more pronounced. At higher frequencies, the compensator inherently limits the variation of the transfer function with respect to L_{ac}, reducing the effectiveness (or necessity) of fine inductance adjustments.

The analysis of the curves relating the magnitude of the transfer function $|A|$ with the choke inductance Z_{load} across multiple frequencies provides a strong justification for selecting an intermediate value of $Z_{load} = 4.5\%$, rather than the maximum inductance typically used in conventional designs.

From the plots of Z_{load} versus $|A|$, it is observed that beyond approximately 3.5%, the gain increases very little with additional inductance. This indicates a saturation region, where higher values of Z_{load} result in diminishing returns in terms of system gain. Therefore, choosing a value much beyond this point would unnecessarily increase implementation costs and system losses without offering proportional benefits in performance.

Moreover, the intermediate value of 4.5% ensures consistent and satisfactory dynamic behavior across the entire frequency spectrum of interest. The Bode plot further corroborates this by showing that the transfer function A with $Z_{load} = 4.5\%$ maintains a well-balanced magnitude response, with adequate low-frequency gain and attenuated high-frequency response—contributing to stability and reduced sensitivity to noise.

IV. CONSERVATIVE POWER THEORY

The CPT offers a systematic and physically grounded framework for decomposing load currents into orthogonal components, each associated with a specific power phenomenon. This orthogonality is central to CPT, as it enables independent compensation strategies depending on the power quality goals and the converter rating available. In the

context of this work, the CPT is employed to synthesize the reference current for the SAPF. When grid voltage distortion is solely due to the connected nonlinear load, the CPT-based reference guarantees that the source current becomes purely sinusoidal. In contrast, if the grid is already polluted by upstream distortions unrelated to the load, the CPT generates a reference that minimizes the root mean square (RMS) value of the source current while preserving the delivery of the same active power. In such cases, the reference current mirrors the voltage waveform, effectively adapting to the grid conditions while ensuring energy conservation.

This flexibility is one of CPT's major strengths, as it supports multiple compensation strategies—ranging from enforcing sinusoidal currents to simply minimizing source effort—without violating physical constraints. Moreover, by targeting a purely active source current, CPT naturally leads to a more efficient use of the SAPF converter rating. The decomposition process is carried out after the insertion of a load-side impedance of $Z_{\text{load}} = 4.5\%$, corresponding to $L_{\text{ac}} = 135\,\mu\text{H}$, as discussed in the previous section. The CPT framework splits the load current into five orthogonal components: active balanced, active unbalanced, reactive balanced, reactive unbalanced, and void currents [17], [19], [20].

V. ONE CYCLE CPT COMPONENTS FOR THE DESIGN OF SAPF

An additional pillar of this paper is the use of one cycle CPT-decomposed current parcels not just for the control of the SAPF but also for its design. This methodology is very helpful for the reduced sizing design of SAPFs, as it is relatively easy to obtain a few cycles of measured voltage (at the point where SAPF needs to be connected) and the load currents from the site. Based on the customer requirement, the appropriate CPT components for compensation are selected and summed together to create the reference current; thereby the design of SAPF can be done. For the considered system, the requirement is to have a unity power factor at the transformer secondary and keep the harmonic distortion below the levels indicated in the IEEE-519 standard. Hence, all the components from CPT except the active balanced current are added to derive the reference current. The following subsection provides the design equations for the components of the SAPF.

A. SAPF-COUPLING INDUCTOR

The SAPF is designed to track the reference current, which is achieved in this implementation using a hysteresis current controller. The sampling frequency is selected to ensure an average switching frequency of approximately 5 kHz in the simulations. When the motor drive operates at full load and the load impedance is set to $Z_{\text{load}} = 4.5\%$, the true RMS value of the rectifier current—without compensation and including all harmonic components—is measured as 461 A. Under this operating condition, one cycle of the reference current is generated using the CPT method. Based on this reference, the maximum allowable ripple current (i_{ripple}) for the SAPF is set to 50 A, which corresponds to 15% of the peak reference current (330 A). The coupling inductor L_{SAPF} is then calculated according to [32]:

$$L_{\text{SAPF}} = \frac{V_{\text{dc}}}{8 \cdot f_{\text{sw}} \cdot i_{\text{ripple}}} = 650\,\mu\text{H} \tag{9}$$

where dc bus voltage is $V_{\text{dc}} = 1300\,\text{V}$, the average switching frequency is $f_{\text{sw}} = 5\,\text{kHz}$.

B. DC LINK VOLTAGE

To estimate the minimum required DC link voltage, a straightforward approach is adopted by calculating the peak phase voltage at the SAPF terminals ($\text{V}_{\text{phase,SAPF}}$). This estimation is based on a single cycle of the reference current generated via the CPT method and the designed value of the coupling inductor, as expressed in (10):

$$\text{V}_{\text{phase,SAPF}} = V_{\text{source}} + L_{\text{SAPF}} \frac{di_{\text{SAPFref}}}{dt} \tag{10}$$

where V_{source} is the peak phase voltage of the grid, and i_{SAPFref} is the reference current calculated by the CPT to the SAPF control. Using this approach, the peak terminal voltage of the SAPF is estimated to be 645 V. To ensure this voltage is attainable when using conventional sinusoidal PWM (Pulse Width Modulator), the DC link voltage must be at least twice the peak terminal voltage, resulting in a required value of $2 \cdot 645 = 1290 \approx 1300\,\text{V}$.

C. SAPF POWER CIRCUIT PARAMETERS

All remaining circuit parameters, including those of the ripple filters, are determined following the standard design procedures described in [1], [33], and [34]. The final values used in the simulations are summarized in Table 3. The hysteresis modulation strategy was selected for the filter, with an average switching frequency of 5 kHz. The capacitive ripple filter at the converter output was designed with a cutoff frequency of 750 Hz, resulting in a capacitance of 106 µF. In addition, a damping resistor of 2 Ω was used in the simulation.

TABLE 3. Power circuit parameters of SAPF designed considering Z_{load} = 4.5%.

Element	Specifications
I_{peak}	400 A with 20% overload
V_{peak}	645 V
Z_{source}	R_s = 6.4 mΩ, L_s = 143 µH,
Switching frequency	f_{sw} = 5 kHz (average)
DC bus Voltage	V_{dcSAPF} = 1300 V
DC bus Capacitance	C_{dcSAPF} = 7.5 mF
Coupling Inductance	L_{SAPF} = 650 µH
Ripple filter	f_{cutoff} = 750 Hz, R_f = 2 Ω, C_f = 106 µF
Modulator	Hysteresis
IGBT current	500 A
IGBT voltage	1700 V

The robustness of the SAPF circuit recommended parameters values is supported by recent state-of-the-art studies. Following the methodology of [10], which demonstrates, through a ±20% variation in the inductance of the output

SAPF filter, that THD remains within acceptable limits under model mismatches, our design maintains compliance with IEEE 519 requirements even under typical manufacturing tolerances and core saturation effects.

Furthermore, the sensitivity analysis explicitly incorporates digital control delays of 20 μs and high-pass filter dynamics, addressing concerns raised in recent literature regarding sampling frequency effects on system stability [11]. This ensures that the 4.5% recommendation remains valid under practical digital implementation constraints, including the DSP-based controller used in experimental validation.

Additionally, by considering the transformer leakage impedance as part of the source impedance, the required load impedance can be reduced from the traditional 6% rule-of-thumb to the optimized 4.5% value without compromising harmonic filtering performance. This is because practical distribution transformers already contribute to significant leakage impedance that is inherently present in the system. When this existing impedance is properly accounted for, the additional load-side impedance required to achieve adequate harmonic attenuation is correspondingly reduced. The traditional rule-of-thumb, by ignoring this contribution, leads to overdesign and unnecessary cost. This approach aligns with passivity-based design principles discussed in [12], which emphasize proper impedance modeling across the entire system to ensure both stability and performance.

VI. SIMULATION RESULTS AND DISCUSSION

To validate the analysis presented in Section III and the design of the SAPF in Section V, three cases are considered for the simulations, considering the system shown in Fig. 1. CASE A is the baseline case, which is without SAPF and with $Z_{\text{load}} = 2.5\%$. The drive is operating at 500 kW constant power load. The implementation of the CPT on Matlab simulink is shown in Fig. 5. Fig. 6(a)-(c) shows the three-phase transformer secondary phase voltages, transformer secondary currents (distorted due to load currents) and load phase currents respectively. Fig. 6(d) shows the three-phase reference currents generated using the CPT as discussed in Section IV. The transformer impedance is sufficiently large to distort the voltage, and hence utilizing SAPF control algorithms that need a PLL can become complex in such cases, and CPT becomes a particularly suitable choice. Fig. 6(e) shows the power in kW as the connected variable frequency drive (VFD) ramps up.

The rectifier kVA rating at full load is found to be 580 kVA in Table 4, when the SAPF is not connected. In case B, without adding any additional impedance at the load side, the designed SAPF from the previous section is connected and the following observations are made. 1) As the SAPF is connected and the CPT derived references are tracked, source voltages and currents become closer to sinusoidal as seen in Fig. 6(f)-(g), respectively. 2) Despite the significant improvement, the THD of the current is still not lower than the 5% required by the IEEE 519 standard, and the source current is slightly flat-topped, due to the limited attenuation

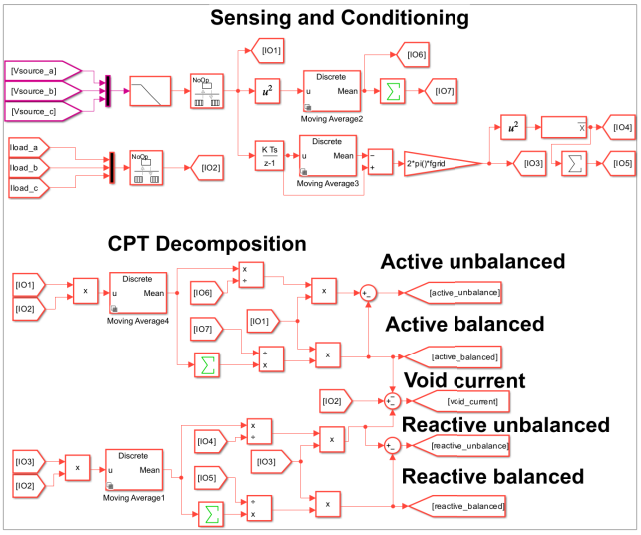

FIGURE 5. Matlab Simulink implementation of CPT.

found in Fig. 3 for dominant harmonics for $Z_{\text{load}} = 2.5\%$. 3) Fig. 6(h) shows a clear increase in the rectifier load currents, when the SAPF is connected at 1 s. This is because the SAPF injects increased harmonic frequency components into the load and then senses them back to compensate them. Fig. 6(i) shows the output current of the SAPF along with the current references generated by the CPT. A good performance is observed, with the output current being very close to the reference value. A proportional integral regulator is employed to regulate the SAPF DC link voltage to 1300 V as shown in Fig. 6(j). This is done by multiplying the PI regulator output with active balanced currents from CPT and subtracting from SAPF reference currents. So with $Z_{load} = 2.5\%$, the estimated increase in rectifier kVA rating is 601 kVAR (3.6%) with a requirement of around 229 kVA of SAPF as shown in Table 4.

Fig. 6 also shows the simulation results of CASE C with the improved design of SAPF and $Z_{\text{load}} = 4.5\%$. As the SAPF is connected and the CPT-based references are tracked, source voltages and currents become close to sinusoidal as seen in Fig. 6(k)-(l) respectively. This is expected as we can see a higher amount of attenuation for CASE C compared to CASE B in source current from Fig. 3. Fig. 6(m)-(n) show that both the load current and the converter current exhibit a clear reduction in amplitude compared to the currents in Case B. Fig. 6(o) shows excellent performance of the dc link voltage regulator and very little increase in the rectifier kVA rating (586 kVA) compared to CASE A, as seen in Table 4. The estimated SAPF rating is found to be around 199 kVA, 13.1% lower than in CASE B, highlighting the advantage of the proposed sizing methodology. Although $Z_{\text{load}} = 4.5\%$. is higher than the existing load impedance, the thumb rule design of placing at least $Z_{\text{load}} = 6\%$ can be avoided for shunt compensation which can save significant space and cost to the concerned customer. The summary of the simulation results is shown in Table 4.

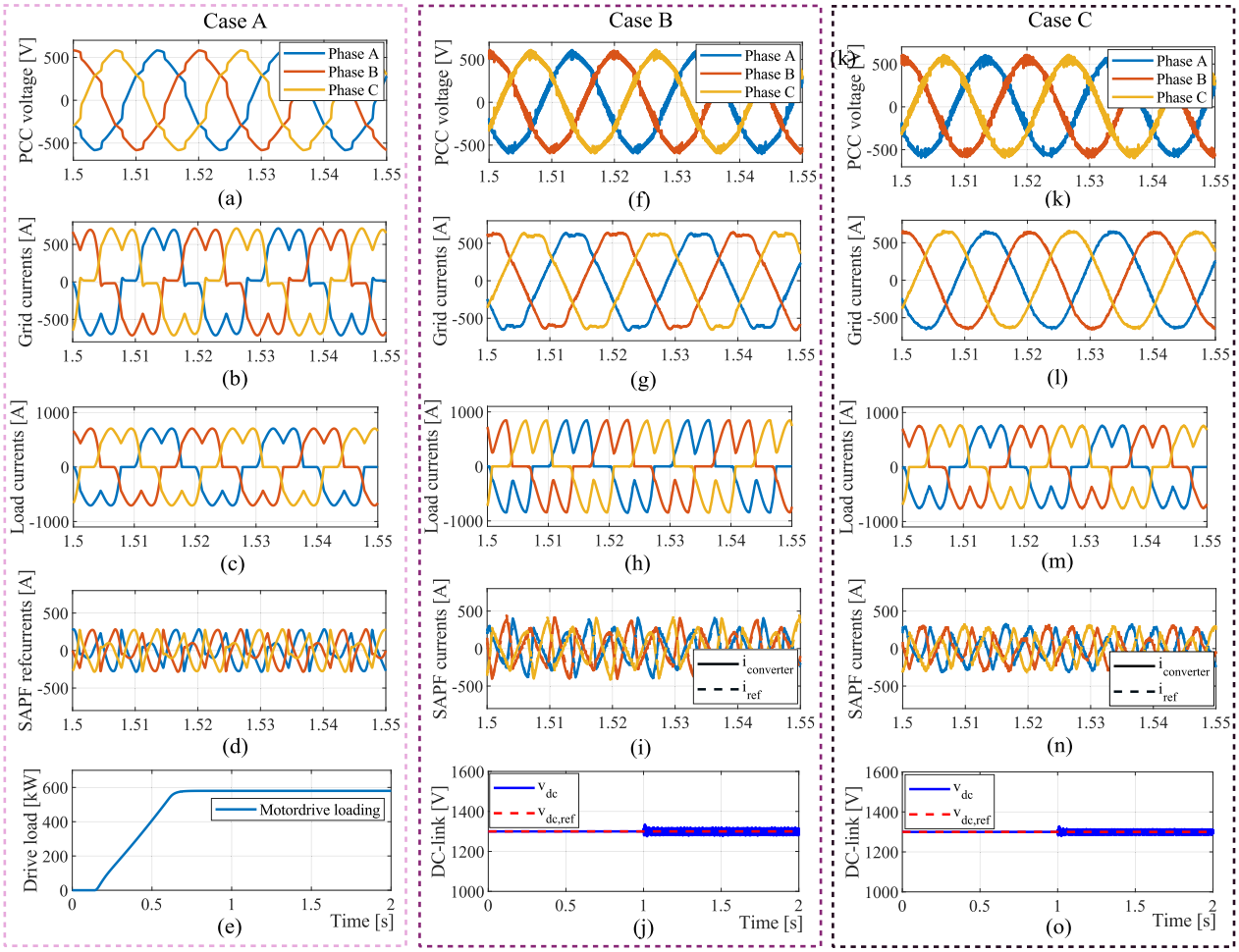

FIGURE 6. Simulated results - CASE A: without SAPF and $Z_{load} = 2.5\%$a) Grid LV voltages (V), b) Grid LV currents (A), c) Rectifier load currents (A), d) SAPF currents (A), e) DC-link voltage (V).CASE B: with SAPF and $Z_{load} = 2.5\%$f) Grid LV voltages (V), g) Grid LV currents (A), h) Rectifier load currents (A), i) SAPF currents (A), j) DC-link voltage (V).CASE C: with SAPF and $Z_{load} = 4.5\%$k) Grid LV voltages (V), l) Grid LV currents (A), m) Rectifier load currents (A), n) SAPF currents (A), o) DC-link voltage (V).

TABLE 4. Summary of simulation results.

Cases	SAPF connection	Z_{load}	Rectifier rating (kVA)	SAPF rating (kVA)	Transformer LV current THD (%)	SAPF DC Voltage (V)
Case A	No SAPF	2.5%	580 kVA	n.a.	28.6%	n.a.
Case B	with SAPF	2.5%	601 kVA	229 kVA	5.6%	1300 V
Case C	with SAPF	4.5%	586 kVA	199 kVA	2.3%	1300 V

VII. EXPERIMENTAL RESULTS

A. THD ANALYSIS

As validation, real-time simulations are used to demonstrate the efficiency and applicability of the proposed solutions. The tests and results presented in this work were conducted on the RT Box 1, developed by Plexim. The RT Box functions as a real-time simulator specifically developed for applications in power electronics, emulating the power stage during HIL testing. This flexible processing unit supports both HIL controller testing and rapid control prototyping (RCP) [35]. This setup allows testing the controller part of the systems without needing a physical power stage. Analog signals from voltage and current sensors, provided by the RT Box's analog outputs, and digital signals like PWM signals, generated through digital outputs, connect to the controller inputs enabling comprehensive, real-time controller evaluation.

Fig. 7 shows the setup used to obtain the experimental results. In RT Box 1, the system presented in Fig. 1 is simulated, as shown in detail in Fig. 8. The active filter control is performed externally by the DSP, which processes voltage and current measurements for CPT calculations and SAPF control. The DSP generates the PWM pulses that are sent to

the switches simulated in RT Box 1. Both the plant and the DSP operate with a sampling frequency of 50 kHz.

The control implemented on the DSP is shown in Fig. 9. A hysteresis control method was chosen for the current loop, while a PI controller regulates the voltage loop to control the dc bus voltage of the SAPF. For voltage control, a reference voltage is compared with the measured circuit value. The error is processed by the controller, which generates a reference for the current loop. The current loop reference is calculated using the CPT. The calculated gains for the dc bus PI controller were: $K_i = 0.61$, and $K_p = 0.01$.

The experiments begin with the CASE A, with the grid supplying the entire power to the load. Fig. 10(a)-(f) present the phase voltages, harmonic spectrum of the grid voltages, phase currents, harmonic spectrum of the grid currents, load currents and SAPF currents for $Z_{\text{load}} = 2.5\%$ without active filter. A behavior very close to the results shown in the simulation is observed. It is possible to observe the harmonic components present in the system through the spectra of the grid voltage and current, shown in Fig. 10(b) and Fig. 10(d), respectively. Harmonic components of the 5^{th}, 7^{th}, 11^{th}, and 13^{th} orders are identified. Table 5 presents the THD values for current and voltage in the grid for impedance values of 2.5% and 4.5%, both with and without the SAPF. The load is observed to exhibit high distortion levels, 28.75% and 25.54%, respectively, which also affect the grid voltage. Fig. 10(g) shows the DC bus voltage of the SAPF. It is important to highlight that even during the period when the converter does not inject current into the system, the dc bus voltage remains close to the nominal value, as the experiments were conducted with the dc bus capacitor already charged.

Fig. 10(h) and Fig. 10(j) show the grid voltages and grid currents for $Z_{\text{load}} = 2.5\%$ when the SAPF injects current to compensate for the non-active portion of the load current. It is noticeable that the grid current visually appears more sinusoidal. Table 5 supports this observation, showing a reduction in current THD to 8.02%. This is also corroborated by the voltage and current spectra shown in Fig. 10(i) and Fig. 10(k), respectively. It can be observed that the amplitude of the harmonic components associated with the load is significantly reduced, since the converter is now responsible for supplying the non-active portion of the load current rather than the grid. Despite the significant improvement, the THD is still not lower than the 5% limit indicated by the IEEE519 standard, and the source current is slightly flat-topped, as explained in the previous section. Fig. 10(l) illustrates a noticeable rise in the rectifier load currents when the SAPF is connected, as it injects additional harmonic frequency components into the load and subsequently senses them for compensation. Fig. 10(m) shows the SAPF currents. The dc bus voltage is shown in Fig. 10(n) at the moment when the SAPF starts injecting current into the system. The control successfully maintains the voltage level close to the nominal value of 1300 V, and a second harmonic oscillation, which is natural in this type of converter, can be observed.

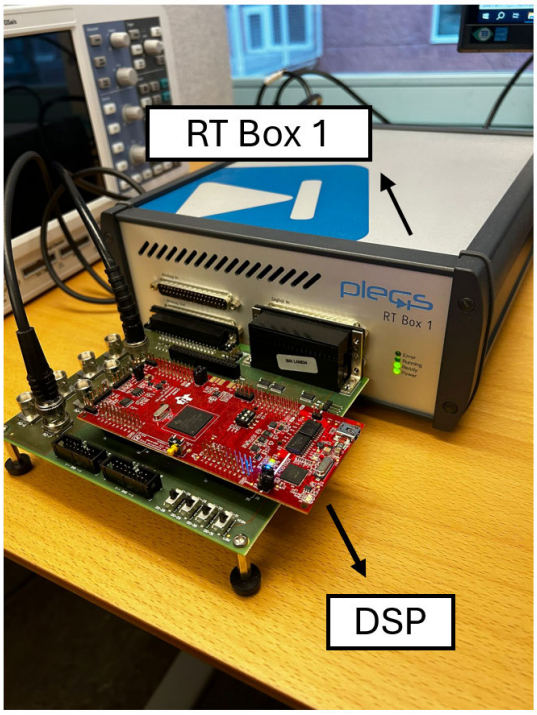

FIGURE 7. RT Box 1 hardware-in-the-loop simulations setup.

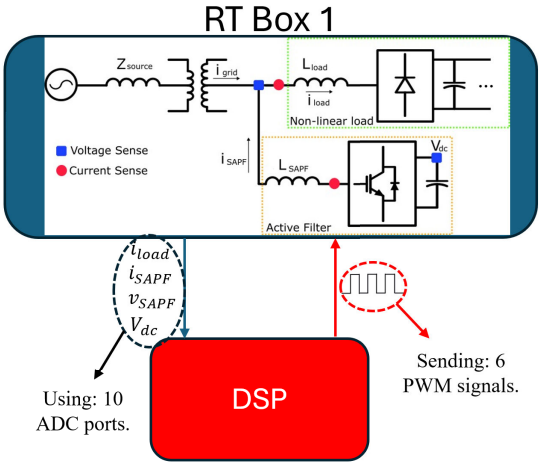

FIGURE 8. RT Box 1 hardware-in-the-loop simulations diagram.

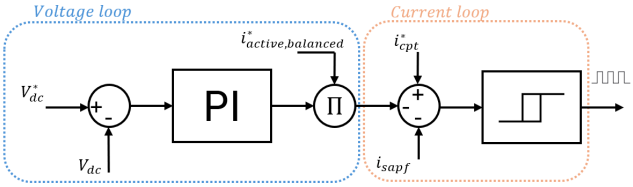

FIGURE 9. Implemented control in DSP for HIL simulations.

Finally, the results for CASE C are shown in Fig. 10(o)-(u). It can be observed from Fig. 10(o) and Fig. 10(q) that the grid voltages and the currents visually

TABLE 5. Comparison of the total harmonic distortion values for current and voltage in the grid for impedance values of 2.5% and 4.5%, both with and without the SAPF.

SAPF connection	Load Impedance	THD current		THD voltage	
		Simulation	Experimental	Simulation	Experimental
No SAPF	2.5%	28.6%	28.75%	7.73%	7.78%
No SAPF	4.5%	25.55%	25.54%	6.98%	6.96%
With SAPF	2.5%	5.6%	8.02%	1.85%	5.13%
With SAPF	4.5%	2.3%	3.93%	1.38%	3.7%

exhibit sinusoidal characteristics. This is confirmed by Table 5, which shows that for a $Z_{\text{load}} = 4.5\%$, the current THD decreases to 3.93%, namely below the limit established by the IEEE 519 standard. This behavior is again observed in the voltage and current spectra at the grid, shown in Fig. 10(p) and Fig. 10(r), respectively. A further reduction in the previously observed harmonic components can be noted, indicating improved performance when $Z_{\text{load}} = 4.5\%$ is used. Once again, Fig. 10(s)-(t) show that both the load current and the SAPF current exhibit a clear reduction in amplitude compared to the currents in CASE B. These results corroborate the findings of the previous sections, proving that the load impedance can be properly designed with lower value than the commonly applied 6%. Once again, the control is able to regulate the dc bus voltage, as shown in Fig. 10(u).

When the SAPF injects current into the grid, the experiment exhibits higher current and voltage distortion compared to the simulation, as shown in Table 5. Fig. 11 presents the harmonic spectrum of the grid current with and without the SAPF for both simulation and experiment. For a load inductance of 2.5% (Fig. 11(a)), the experiment shows higher amplitude in most harmonic components, particularly in the fifth harmonic. A similar trend is observed for $Z_{\text{load}} = 4.5\%$, as shown in Fig. 11(b). The increased distortion observed in the PLECS RT box experiment could be due to delays and limited resolution in the real-time implementation of the hysteresis modulator. These factors reduce the accuracy of current tracking, resulting in slightly higher ripple and increased harmonic content.

Fig. 12 shows the harmonic spectrum of the grid voltage with and without the SAPF for both simulation and experimental results. From Table 5, it can be observed that the difference in the grid voltage between simulation and experiment with the SAPF disconnected is minimal, which is also evident from the zoomed view of the fifth harmonic in Fig. 12(a). When the SAPF injects current, the difference becomes more visually noticeable in the harmonic components. This discrepancy can be explained by the same reason observed in the current results, namely delays and limited resolution in the real-time implementation of the hysteresis modulator. Fig. 12(b) further confirms the higher efficiency achieved when $Z_{\text{load}} = 4.5\%$ is used.

To further confirm the effectiveness of the proposed solution, the ripple in the grid current is also analyzed using the experimental results. The ripple analysis is carried out in discrete time using the measured grid current samples $i[n] = i(nT_s)$, with a sampling interval of $T_s = 4 \times 10^{-7}$ s. Considering a fundamental grid frequency of $f_0 = 50$ Hz, the analysis window covers two complete fundamental periods ($T = 0.04$ s), which ensures an unbiased estimation of the fundamental component.

The fundamental current component is estimated in the time domain using a least-squares sinusoidal fit, expressed as:

$$i_{50}[n] = A \sin(2\pi f_0 n T_s) + B \cos(2\pi f_0 n T_s), \tag{11}$$

where A and B are the fitted coefficients that define the amplitude and phase of the fundamental component, T_s is the sampling interval, and n denotes the discrete-time sample index.

The ripple current is defined as the residual signal obtained by subtracting the fitted fundamental component from the measured current:

$$i_{\text{ripple}}[n] = i[n] - i_{50}[n], \tag{12}$$

where $i[n]$ is the measured grid current sample and $i_{50}[n]$ represents the estimated fundamental component at the same sampling instant.

The RMS value of the ripple current is computed using the discrete-time formulation:

$$I_{\text{ripple,rms}} = \sqrt{\frac{1}{N} \sum_{n=0}^{N-1} i_{\text{ripple}}^2[n]}, \tag{13}$$

where N is the total number of samples within the analysis window.

The RMS value of the fundamental component, denoted as $I_{50,\text{rms}}$, is computed from the fitted waveform using the same discrete-time RMS definition. Finally, the ripple is expressed in percentage relative to the fundamental RMS value as:

$$\text{Ripple}(\%) = 100 \cdot \frac{I_{\text{ripple,rms}}}{I_{50,\text{rms}}}. \tag{14}$$

Table 6 shows the ripple percentage in the grid current for both load impedances. For $Z_{\text{load}} = 2.5\%$, the calculated ripple value is 8.68%, calculated using the grid current, whereas for $Z_{\text{load}} = 4.5\%$, the calculated value is 5.10%. These results further demonstrate that the performance obtained with $Z_{\text{load}} = 4.5\%$ is superior when comparing the ripple in the grid current.

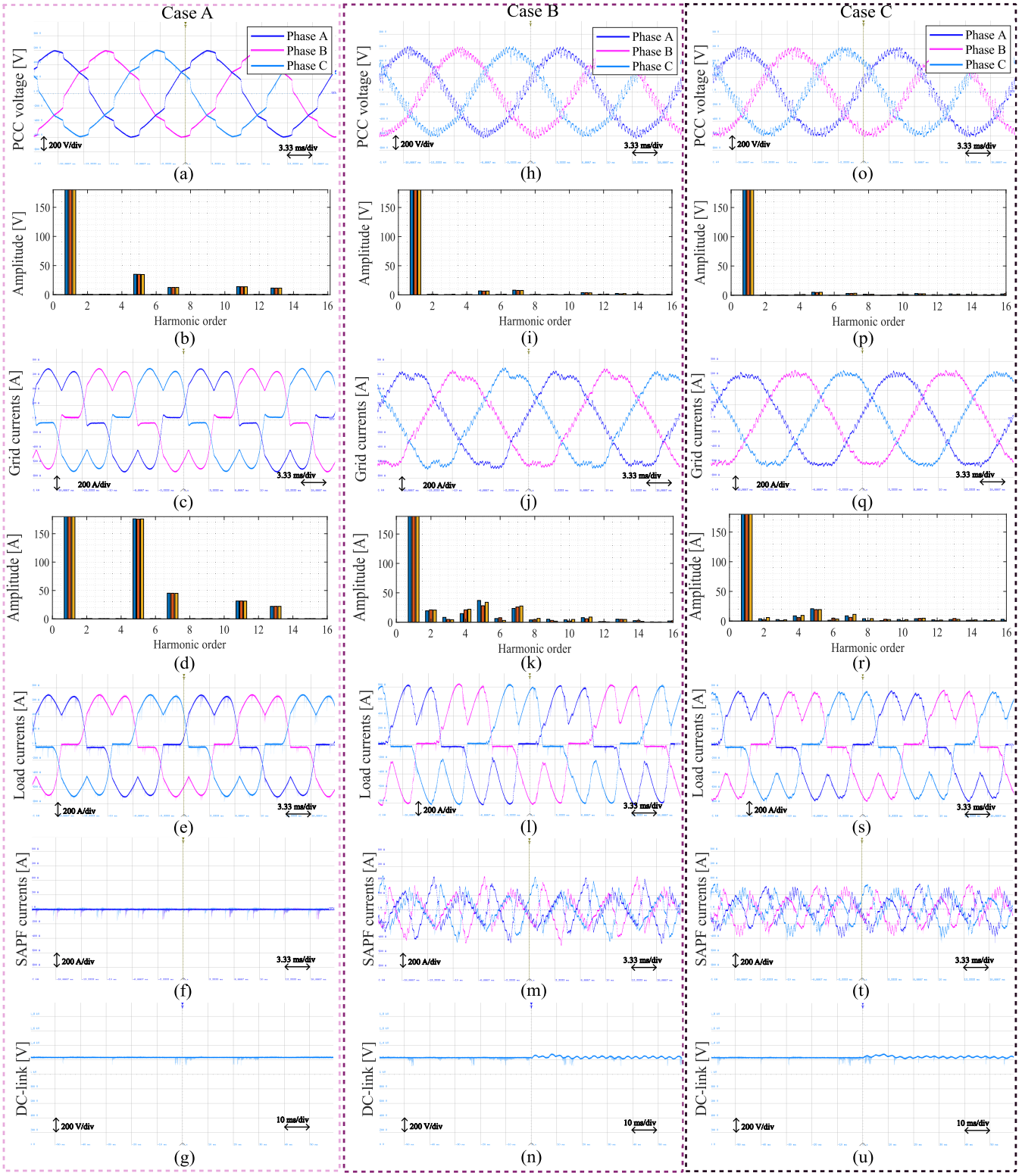

FIGURE 10. Experimental results - CASE A: without SAPF and $Z_{load} = 2.5\%$a) Grid LV voltages (V), b) Harmonic spectrum of the grid LV voltages, c) Grid LV currents (A), d) Harmonic spectrum grid LV currents, e) Rectifier load currents (A), f) Reference currents from CPT (A), g) VFD drive load (kW).CASE B: with SAPF and $Z_{load} = 2.5\%$h) Grid LV voltages (V), i) Harmonic spectrum of the grid LV voltages, j) Grid LV currents (A), k) Harmonic spectrum grid LV currents, l) Rectifier load currents (A), m) SAPF reference currents from CPT and actual SAPF currents (A), n) SAPF V_{dc} reference and actual DC-link voltage (V).CASE C: with SAPF and $Z_{load} = 4.5\%$o) Grid LV voltages (V), p) Harmonic spectrum of the grid LV voltages, q) Grid LV currents (A), r) Harmonic spectrum grid LV currents, s) Rectifier load currents (A), t) SAPF reference currents from CPT and actual SAPF currents (A), u) SAPF V_{dc} reference and actual DC-link voltage (V).

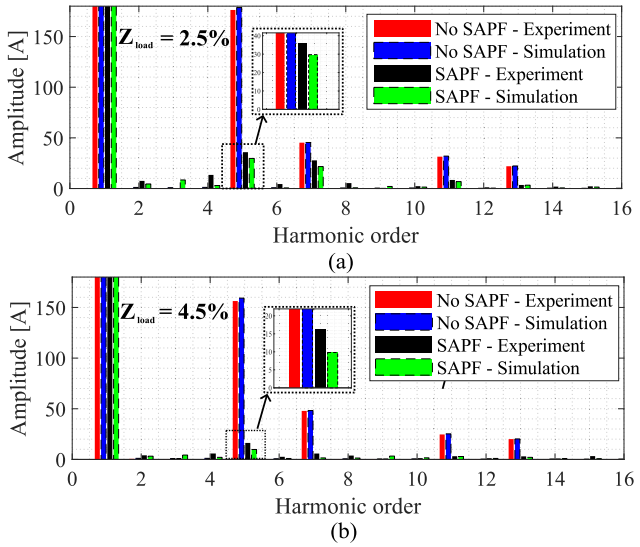

FIGURE 11. Harmonic spectrum of the grid current with and without the SAPF, for simulations and experiments for: (a) Z_{load} = 2.5%, (b) Z_{load} = 4.5%.

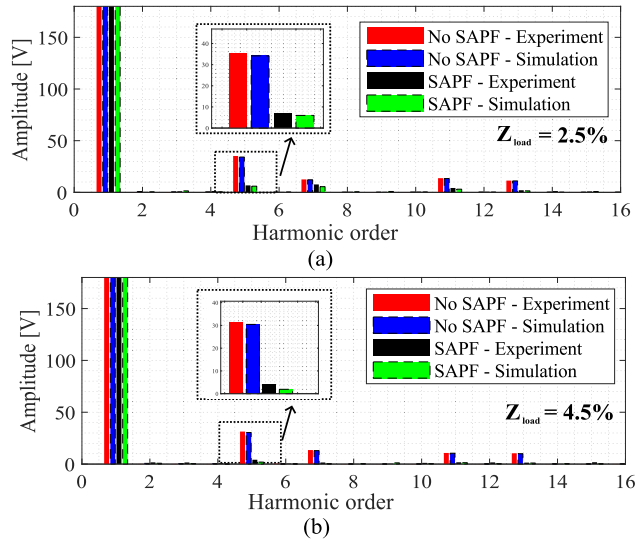

FIGURE 12. Harmonic spectrum of the grid voltage with and without the SAPF, for simulations and experiments for: (a) Z_{load} = 2.5%, (b) Z_{load} = 4.5%.

TABLE 6. Ripple percentage of the grid current.

Impedance load condition	Grid current % ripple
$Z_{load} = 2.5\%$	8.68%
$Z_{load} = 4.5\%$	5.10%

B. DYNAMIC PERFORMANCE AND TRANSIENT ANALYSIS

First, the dynamic response is analyzed when the converter starts compensating the entire non-active portion of the load. Fig. 13(a) shows the converter output currents for $Z_{load} = 2.5\%$. Initially, the converter current is zero until it is connected to the grid. From this moment onward, the converter exchanges current with the grid to control the DC-link voltage. Subsequently, the control system begins compensating the entire non-active portion of the load. The same result for $Z_{load} = 4.5\%$ is observed in Fig. 13(b). In both cases, no overcurrent is observed at the converter output, and the converter successfully tracks the reference generated by the CPT in less than two cycles of operation. It is important to note that all transitions presented in this section were performed without any control technique to minimize transition effects. To connect the converter to the grid, a switch is activated, sending a signal that enables the converter to connect to the grid, regardless of the load current values. A signal is also sent to enable the converter to start harmonic compensation in the grid.

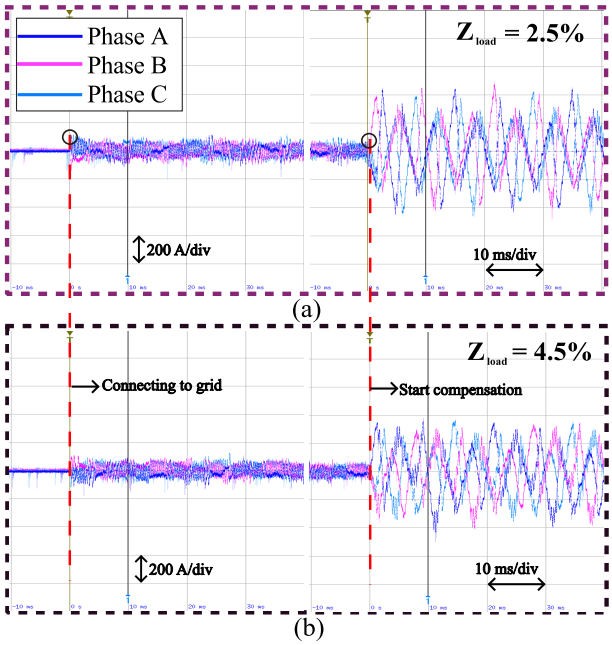

FIGURE 13. Dynamic response of converter currents when the converter connects to the grid, and starts compensating the non-active power of the load, with: (a) Z_{load} = 2.5%, (b) Z_{load} = 4.5%.

The grid currents and voltages when the converter starts compensating the non-active portion of the load for $Z_{load} = 2.5\%$ and $Z_{load} = 4.5\%$ are shown in Fig. 14. It can be observed that the current, previously with a high low-order harmonic content as shown in previous sections, becomes visually more sinusoidal. The current transition is smooth, with no overcurrent in either case. The voltage in both cases also presents a very smooth transition, only reducing the low-order components without overvoltage.

The dynamic response of the system is also analyzed when a load power change occurs. For this analysis, the load initially operates at 60% of the nominal load until a step load occurs and the load starts operating at 100% of the nominal capability. Fig. 15 shows the dynamic response of grid currents and voltages during the load step for $Z_{load} = 2.5\%$ and $Z_{load} = 4.5\%$. In Fig. 15(a), a current peak is observed in the first cycle reaching slightly over 800 A, which

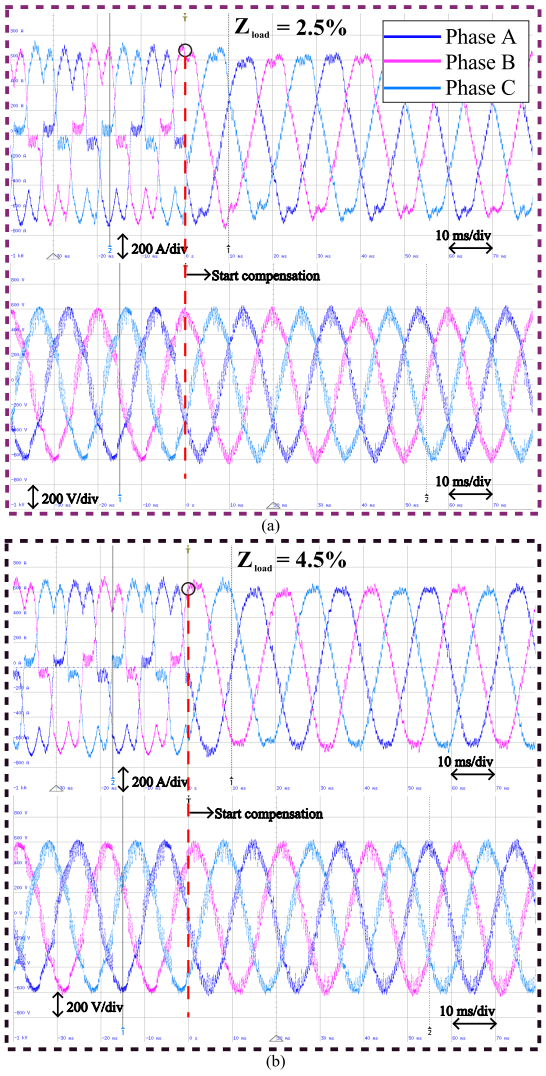

FIGURE 14. Dynamic response of grid currents and voltages when the converter starts compensating the non-active power of the load, with: (a) $Z_{load} = 2.5\%$, (b) $Z_{load} = 4.5\%$.

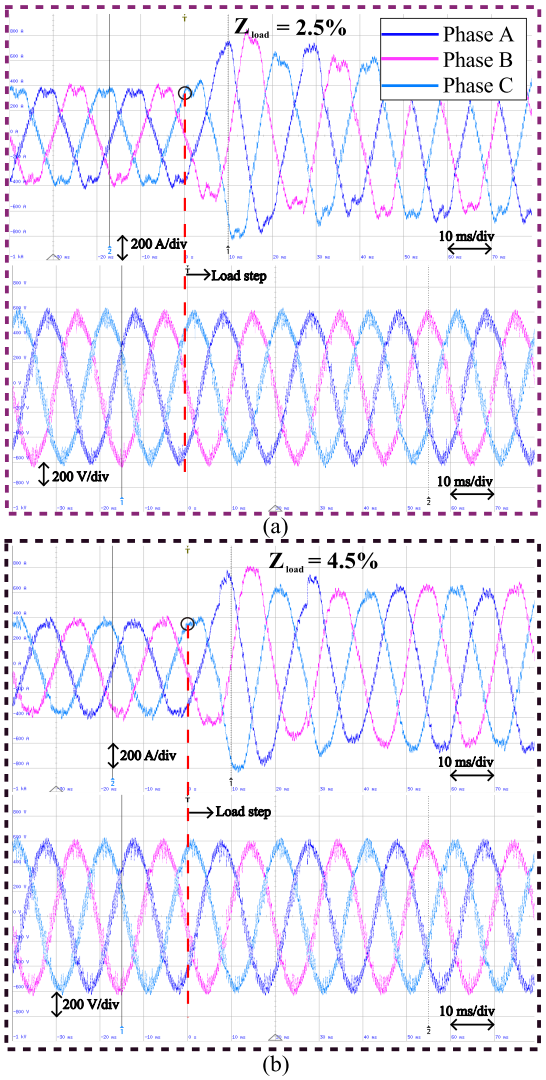

FIGURE 15. Dynamic response of grid currents and voltages during a load step change from 60% to 100% of the nominal load, with: (a) $Z_{load} = 2.5\%$, (b) $Z_{load} = 4.5\%$.

corresponds to approximately 33% of the peak current value when the load is at 100% of the nominal value. For a load step, this is an acceptable value, and the system protection devices are not affected by peaks of this proportion. In the second cycle of operation, the currents already present the nominal value in steady state. The current behavior is similar for both cases, with the only difference being that for the current shown in Fig. 15(b) with $Z_{load} = 4.5\%$, the current presents less low-order distortion, as discussed in the results presented previously. In both cases, any voltage change due to the load variation is imperceptible.

Finally, the converter output current and the DC-link voltage are shown in Figure 15. It can be observed that the converter output current for $Z_{load} = 2.5\%$ and $Z_{load} = 4.5\%$, shown in Fig. 16(a) and Fig. 16(b) respectively, successfully injects the non-active current calculated by the CPT by the second cycle. A negative current peak is observed in Fig. 16(a) reaching 620 A, which is approximately 24% of the peak value of this current in steady state. For the current with $Z_{load} = 4.5\%$ in Fig. 16(b), this peak is even smaller, with the negative peak in the first cycle of one of the phases being about 10% higher than the steady-state value at full load. The DC-link voltage is shown in Fig. 16(c) and Fig. 16(d). After the load step, the voltage oscillates approximately 100 V around the average value and takes about 60 ms to stabilize, which corresponds to 3 cycles of the fundamental frequency. For a DC-link of a converter maintaining a voltage at 1600 V, this represents a good dynamic response considering the power level injected by the converter into the grid.

C. COMPARATIVE ANALYSIS WITH STATE-OF-THE-ART METHODS

To quantitatively benchmark the proposed method against recent advances in SAPF control, a comprehensive comparison was conducted with twelve state-of-the-art works

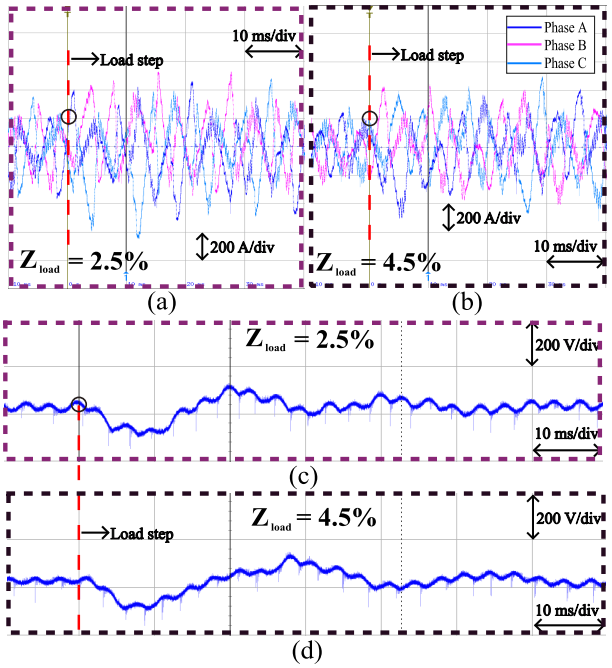

FIGURE 16. Dynamic response of converter currents during a load step change from 60% to 100% of the nominal load, with: (a) $Z_{load} = 2.5\%$, (b) $Z_{load} = 4.5\%$. Dynamic response of the DC-link voltage during this transition for: (c) $Z_{load} = 2.5\%$, (d) $Z_{load} = 4.5\%$.

published between 2014 and 2025, as summarized in Table 7. This comparison focuses on key aspects: choke inductance specification, validation methodology, initial current THD, final current THD achieved in both simulation and experimentation. The analysis reveals several important findings that highlight both the competitiveness and the unique contributions of our proposed approach.

A critical observation from this comparative study is that none of the recent state-of-the-art works specify or analytically justify the load-side choke inductance value used in their implementations. This parameter, which plays a fundamental role in the overall performance and sizing of SAPF systems, is either omitted entirely or assumed without proper justification. In contrast, our work provides a systematic methodology for determining the choke inductance value of 4.5%, based on rigorous transfer function analysis and frequency response considerations. This represents a significant and unique contribution, as proper passive component sizing is essential for practical SAPF applications yet remains systematically neglected.

Regarding harmonic mitigation performance, the final current THD achieved by our method reaches 2.3% in simulation and 3.93% in experimental hardware-in-the-loop tests. These results are fully comparable with the best state-of-the-art results reported in the literature, which range from 1.09% to 5.7% depending on the operating conditions and validation methods employed. For instance, recent MPC-based approaches have demonstrated THD values of 1.59% in simulation and 2.77% in experimental tests, while passivity-based designs have achieved 2.6% experimentally. Similarly, dispersing QPR controllers have reported current THD below 3% in simulation and below 4% in experimental validation. Our experimental THD of 3.93% is well within the IEEE 519 standard requirement of less than 5%, confirming that the proposed method achieves state-of-the-art harmonic mitigation performance while offering additional benefits in component sizing that are not addressed in other works.

Some works included in the comparison utilize Conservative Power Theory, providing particularly relevant benchmarks for our approach. These studies have demonstrated the effectiveness of CPT for harmonic filtering and reactive power compensation under non-ideal voltage conditions, achieving experimental current THD reductions to values between 4.5% and 5.1% for various load configurations. While these works validate the suitability of the CPT framework for shunt active filter control, none of them address the systematic design of passive components. Our work extends the CPT framework beyond its conventional application in control by integrating it with a comprehensive component sizing methodology, resulting in improved THD performance of 3.93% experimentally.

The validation robustness of our approach is evidenced through both simulation and hardware-in-the-loop experiments with an external digital signal processor implementing the complete control in real time. This level of validation is comparable to the most rigorous state-of-the-art works and exceeds those that are purely simulation-based, providing greater confidence in the practical applicability of the proposed method.

Perhaps most significantly, while state-of-the-art methods focus primarily on control algorithm sophistication through approaches such as model predictive control, neural networks, optimized proportional-resonant controllers, and various CPT-based strategies, our work addresses a complementary and equally important aspect that has been largely overlooked. Specifically, our analysis demonstrates a 13.1% reduction in SAPF rating from 229 kVA to 199 kVA achieved through proper choke inductance sizing, representing a quantifiable loss reduction for practical installations.

Furthermore, this work challenges the traditional industry rule-of-thumb that recommends a minimum load impedance of 6%. Through frequency response analysis, we demonstrate that 4.5% is sufficient when combined with proper control design, as increasing the choke inductance beyond 3.5% yields diminishing returns in terms of harmonic attenuation.

In summary, the comparative analysis demonstrates that while our control approach achieves harmonic mitigation performance that is fully competitive with the current state of the art, its primary and most distinctive contribution lies in the systematic design methodology for passive components. This integrated approach to component sizing and control design offers practical benefits for industrial applications that are not

TABLE 7. Comparative analysis of SAPF control strategies.

Reference - Contribution	Choke Inductance (Lac)	Validation Methodology	Initial Current THD	Final <current THD (Sim/Exp)
[8] - MPC with Lyapunov stability	N/S	Simulation + HIL	26.71%	1.59% (sim) / 2.77% (exp)
[9] - ADALINE neural network	N/S	Simulation + Experimental	29.5%	2.46% (sim) / 5.7% (exp)
[10] - GA-optimized PR	N/S	Simulation + Experimental	20.2% (R-L) / 56.1% (R-C)	4.2% (exp R-L) / 4.5% (exp R-C)
[11] - Dispersing QPR	N/S	Simulation + Experimental	25% (estimated)	<3% (sim) / <4% (exp)
[12] - Passivity-based RAPF	N/S	Experimental	25.9%	2.6% (exp)
[13] - Losses and efficiency (SiC vs IGBT)	N/S	Simulation + PLECS	N/A (losses focus)	N/A
[14] - ROGI	N/S	Simulation	19.56% (R-L) / 17.84% (R-C)	1.09% (sim R-L) / 0.69% (sim R-C)
[15] - FPGA with HCSLPF	N/S	Simulation + Experimental	27.7% (sim) / 29.1% (exp)	3.47% (sim) / 5.6% (exp)
[16] - Dual fundamental extraction	N/S	Simulation + Experimental	27.34%	2% (sim) / 3.5% (exp)
[21] - PQ, DQ and CPT comparative study	N/S	Simulation	25% (estimated)	2% (sim) with non-active compensation
[19] - Reactive and harmonic compensation with CPT	N/S	Simulation + Experimental	29.5% (Case 1) / 72.6% (Case 2) / 20.6% (Case 3)	5.1% (exp Case 1) / 35.7% (exp Case 2) / 4.5% (exp Case 3)*
This work - CPT + Impedance Analysis	**4.5% pu**	**Simulation + HIL with external DSP**	**28.6%**	**2.3% (sim) / 3.93% (exp)**

*N/S: Not specified in the work; N/A: Not applicable; HIL: Hardware-in-the-loop; HCSLPF: Harmonic Component Separation Method with Low-Pass Filter; ROGI: Reduced-Order Generalized Integrator; QPR: Quasi-Proportional Resonance; RAPF: Resistive-Active Power Filter. *Values correspond to three different test cases (diode rectifier, thyristor rectifier, and RL-load) presented in [19].*

addressed in the recent literature, including previous CPT-based works, thereby filling an important gap in the field of shunt active power filtering.

VIII. CONCLUSION

This paper performed a detailed analysis of the behavior of SAPF when used to compensate loads with a diode bridge front end supplying a large induction motor as in typical industrial drives. It also proposed a sizing methodology for the passive components of the SAPF, that results in reduced component size. When combined with a SAPF control strategy based on the CPT one cycle current decomposition this approach proves effective in harmonic mitigation. Analysis, design, and control have been validated through PLECS simulations and hardware-in-the-loop experiments.

In fact, the results indicate that the load inductance value of 4.5% determined with the proposed approach is effective, as it allows the use of a SAPF with a lower rating compared to the case with a load inductance of 2.5%, while still enabling a satisfactory current and voltage distortion reduction, in compliance with the IEEE519 standard.

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JOÃO HENRIQUE DE OLIVEIRA (Member, IEEE) received the B.S. degree in electrical engineering from the Federal University of Viçosa (UFV), in 2014, and the M.S. and Ph.D. degrees from the Federal University of Minas Gerais (UFMG), in 2016 and 2024, respectively. He was a Visiting Scholar with Wisconsin Electric Machines and Power Electronics Consortium, University of Wisconsin–Madison, USA, in 2023. He is currently a Postdoctoral Fellow with Norwegian University of Science and Technology (NTNU). His main research interests include control and reliability of power converters, microgrid control, and power quality.

JOSEPH KIRAN BANDA (Member, IEEE) was born in Hyderabad, India, in 1991. He received the B.E. degree in electrical and electronics engineering from Osmania University, Hyderabad, in 2012, the M.Tech. degree in electrical engineering from Indian Institute of Technology Delhi, New Delhi, India, in 2014, and the Ph.D. degree in electric energy from Norwegian University of Science and Technology (NTNU), Trondheim, Norway, in 2025. From 2014 to 2017, he held research and development roles at Eaton Technologies, Pune, India, and Medha Servo Drives, Hyderabad. Subsequently, he was a Research Associate with the Rolls-Royce NTU Corporate Laboratory, Singapore, from 2017 to 2018, and as a Research Engineer at GE Global Research Center, Bengaluru, India, from 2018 to 2021. He is currently a Research Scientist at SINTEF Energy Research, Trondheim. His research interests include the control of grid-tied power electronic converters (grid-forming and grid-following), HVDC and energy storage integrated FACTS for modern energy systems, design and control of multilevel converters, and the control of electrical machines, including induction and permanent-magnet machines.

ELISABETTA TEDESCHI (Senior Member, IEEE) received the M.Sc. degree (Hons.) in electrical engineering and the Ph.D. degree in industrial engineering from the University of Padua, Italy, in 2005 and 2009, respectively. From 2009 to 2011, she was a Postdoctoral Researcher with Norwegian University of Science and Technology (NTNU), working on the grid integration of offshore renewable energies. She was a Researcher/Marie Curie Fellow at Tecnalia, Spain, from 2011 to 2013, where she was the Principal Investigator in the FP7-Sea2grid Project, related to the storage needs for the grid integration of wave energy converters. From 2013 to 2014, she was a Research Scientist at SINTEF Energy Research and an Adjunct Associate Professor at NTNU. In 2014, she became a Full Professor within the offshore grid at NTNU. Since 2020, she has also been a Full Professor at the Department of Industrial Engineering of the University of Trento, Italy. She has a core competence in the design and control of energy conversion and transmission and distribution systems, with a focus on offshore energy and power-quality issues. She has led and/or contributed to more than 15 national and international scientific projects, and she has authored or co-authored two book chapters and more than 150 journals and conference papers in the field of marine energy and energy conversion systems.