Selective PQD Power Control Strategy for Single-Phase Grid-Following Inverters

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***Abstract*—This paper proposes the selective PQD power control strategy based on proportional-integral controllers devised in stationary abc-reference frame for single-phase *grid-following* inverters. Its physical behavior and mathematical model are presented in detail and the system output impedance is derived. It is shown that the proposed control accurately tracks active, reactive, and selective distortion power terms. Experimental results show that the proposed control strategy effectively rejects source disturbances, achieving low values of current distortion even under heavily distorted grid voltages. Stability analysis under stiff and weak grids and DC-link voltage control for photovoltaic applications are evaluated. It is also shown that the implemented technique requires 26% less execution time in the main interruption than conventional solutions using proportional-integral plus resonant controllers.**

***Index Terms*—Converter control, distributed energy resource, harmonics, PQD strategy, power quality.**

I. Introduction

RENEWABLE energy sources (RES) are usually interfaced with the electrical grid through power converters that must comply with standards, such as the IEEE Std 1547-2018 [1], which establish requirements for the connection of distributed energy resources (DERs). Such converters are usually *grid-following* inverters [2] and behave as current sources, with high output impedance [3]. An important index addressed and strictly limited by those standards is the total harmonic distortion of the current (THD). Its value is affected by the converter control and the voltage at the DER connection point, herein referred to as the point of common coupling (PCC).

Current control strategies for current-driven grid-connected converters are broadly categorized as linear and non-linear. Regarding the non-linear category, one of the most used strategies is the hysteresis control [4], [5]. Although it is easy to implement and allows fast dynamic response, its switching frequency is typically variable, complicating output filter design. Repetitive controllers [6] are also common, but are more complex and need careful tuning to avoid instability. Many predictive controls are parameter-dependent approaches that typically present variable modulation frequencies and may result in computation-intensive algorithms [7]. Therefore, the linear approaches are more often applied because of their simplicity [8]. The linear control category can be further subdivided into single, double, and triple-loop controls [9], depending on how many state variables are regulated. The most widely used linear controllers are the proportional-integral (PI), in both stationary and synchronous reference frames; the proportional-resonant (PR); and the PI-resonant (PI-R) [10], [11]. Some repetitive controllers are linear as well (e.g., [12]), but they are not addressed herein.

For the stationary PI, the main setback is its low gain for medium and high frequencies, which causes steady-state errors when tracking sinusoidal reference signals and low rejection of harmonic disturbances. The Park transformation is widely used to overcome this limitation at the fundamental frequency since it converts the control signals to DC quantities in dq-frame, where PI regulators are fairly applied. Still, it does not eliminate oscillations under unbalanced voltages. In this case, it requires the use of two controllers per axis to independently regulate the positive and negative sequence components [13]. Similarly, for harmonic compensation, a reference frame has to be used for each harmonic order [14]. Additionally, in single-phase applications, the Park transformation cannot be directly applied, so a quadrature voltage signal has to be synthesized. In [15] a simplified method to compute the dq components is proposed, improving the system dynamics, but the other above-mentioned issues remain unaddressed.

PR and PI-R controllers solve the drawbacks of the stationary frame PI, in which the high gain at selected frequencies enhances the system disturbance rejection capability. Their main drawbacks, when compared to the PI, are: (i) need for high bit resolution; (ii) stability issues in low-cost fixed-point digital signal processor (DSP) implementations due to the pole-clustering effect caused by truncation, normalization, or quantization of the controller coefficients; and (iii) heavy computational burden since one controller per harmonic frequency is implemented into the main interruption (MI) of the DSP. A down-sampled multi-rate resonant controller is studied to overcome this issue in [16].

The disturbance rejection capability is also widely discussed in the literature. The authors of [17] proposed a strategy to improve the robustness of a grid current control with active damping. The authors of [18] show two ways of improving the inverter response under weak grid conditions by reshaping the inverter admittance. However, they do not thoroughly discuss the effect of their method on the inverter output impedance

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and reduced computational burden.

The emerging scenario of advanced microgrids (MGs) also offers challenges to efficiently exploit RESs, taking advantage of the coordination and control of DERs [19]. DERs can be indifferently driven by current [20] or power [21] commands, exchanged through a low-bandwidth communication infrastructure. Despite the faster dynamics, current commands cannot be used to drive DERs from a central controller if the grid includes phase-shifting or coupling transformers with a transformation ratio (TR) different from unity. In such cases, TR must be considered in this centralized algorithm, demanding thorough grid knowledge and reducing the plug-and-play capability of the strategy. For the aforementioned reasons, power-commanded DERs are preferred and have motivated the proposed so-called PQD strategy. Thus, this paper proposes a control strategy capable of regulating active, reactive, and distortion power terms for single-phase *grid-following* inverters. Since all control loops use only PI controllers, the technique is simple and involves a relatively small amount of digital computations to be implemented in the DSP MI. Additionally, a small number of sensors is required, since the control scheme demands only the measurement of inductor current and output capacitor voltage. It is shown that the proposed control strategy rejects disturbances, dispatches selective power terms, is easily extended to photovoltaic (PV) applications, and achieves low current THD values even under distorted grid voltage.

This paper is an extended version of [22], with significant contributions regarding the output impedance model of the proposed control strategy, further simulation, and experimental results, the applicability of the proposal for PV and coordinated control scenarios and impedance-based stability analysis for a wide grid short-circuit capacity (SCC) range. Notably, an analysis regarding the execution time is presented herein, highlighting the merits of the proposed approach concerning other conventional solutions (i.e., resonant controllers). The paper is organized as follows: Section II describes the inverter structure and conventional current control loop, introducing the inverter output impedance evaluation. Then, Section III proposes the selective PQD power control strategy, controller tuning procedure, and inverter output impedance improvement. Sections IV and V report simulation and experimental results, respectively. Section VI concludes this paper.

II. System Description

The system analyzed herein is a single-phase *grid-following* inverter-based DER [23], as shown in Fig. 1(a). Fig. 1(b) shows the proposed PQD control block diagram, which consists of two-cascaded loops: an outer active (P_{out}), reactive (Q_{out}) and distortion ($D_{h\parallel}$ and $D_{h\perp}$) power control loop for current reference (i_f^*) generation, and an inner current control loop for output current (i_f) tracking. $C_p(s)$, $C_q(s)$, $C_{h\parallel}(s)$ and $C_{h\perp}(s)$ are the active, reactive, h-th in-phase distortion and h-th quadrature distortion controllers, respectively. $h \in \{H\}$, where H is the set of harmonic orders to enhance the converter output impedance. $C_i(s)$ is the inner PI-based current controller. The switch at positions ① and ② selects the

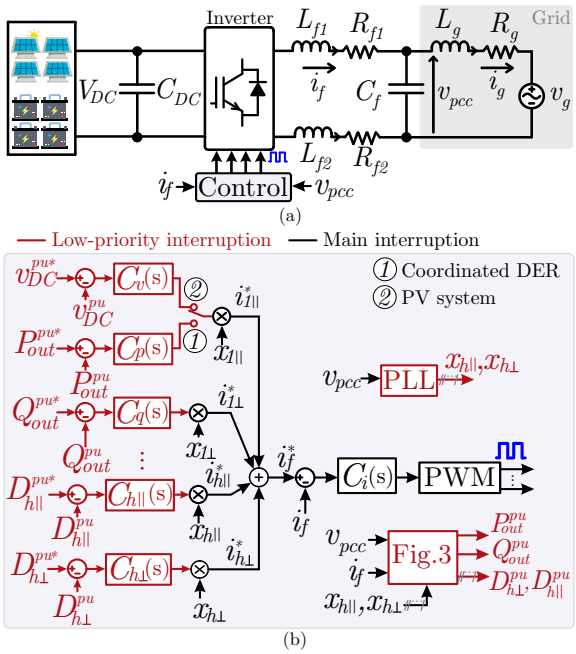

Fig. 1. (a) Single-phase *grid-following* inverter-based DER. (b) Block diagram of the proposed PQD control strategy.

DER control for coordinated and PV applications, respectively. At position ①, the control strategy is essentially suitable for *grid-following* inverters endowed with battery energy storage systems in MG applications. At position ②, the active power loop is replaced by a conventional DC-link voltage (v_{DC}) control loop for PV applications, where the v_{DC}^* reference is tracked by an MPPT algorithm [24]. The DC-link voltage control guarantees an indirect control of the active power flow from the PV modules into the AC grid. Therefore, all the advantages of the PQD strategy are maintained.

A. Current control

Fig. 2 shows the current (i_f) control loop, in which the PWM block models the computational delay from the analog-to-digital conversion and the digital pulse-width modulation (PWM). $G_{conv}(s) = 2V_{DC}$ is the transfer function (TF) between the output of the PWM comparator and the synthesized voltage at the converter bridge, where v_{DC} is the DC-link voltage, Z_f is the output filter impedance, H_i is the current transducer gain, and, finally, v_{pcc} is the instantaneous voltage at the PCC. The open-loop TF of the current loop $G_{OL}^i(s)$ for a uniformly sampled, single-update, unipolar and symmetrical PWM with a triangular carrier is given by [25]:

$$G_{OL}^i(s) = \overbrace{\frac{K_{pi}s + K_{ii}}{s}}^{C_i(s)} \cdot \overbrace{\frac{1 - s\frac{3T_s}{4}}{2C_{pk}(1 + s\frac{3T_s}{4})}}^{\text{PWM}} \cdot \overbrace{2v_{DC}}^{G_{conv}} \frac{1}{Z_f} \frac{1}{H_i}, \quad (1)$$

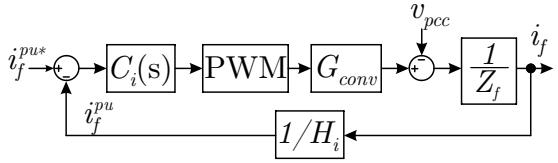

Fig. 2. Block diagram of the inverter-side current control loop.

where T_s denotes the sampling period. C_{pk} is the peak-to-peak value of the PWM carrier. K_{pi} and K_{ii} are the proportional and integral gains of the current PI controller, respectively. Considering the open-loop TF in (1), K_{pi} and K_{ii} are selected based on the frequency method to achieve a cut-off frequency of 1 kHz and phase margin of 60° [25]. It is worth underlining that the cut-off frequency cannot be higher due to hardware constraints. Finally, the DER output impedance for conventional current control is given by:

$$Z_{out}(s) = -\left(\frac{2v_{DC}\cdot \mathrm{PWM}\cdot C_i(s)}{H_i} + Z_f\right), \qquad (2)$$

where Z_{out} is the TF between the disturbance (v_{pcc}) and the controlled quantity (i_f).

III. Selective PQD Power Control Strategy

The proposed selective PQD power control enhances Z_{out} and controls the current harmonic components through the power loops adjusting the current reference accordingly to the measured harmonic currents, as shown in Fig. 1(b). It is composed of a pair of PI controllers, $C_p(s)$ and $C_q(s)$ responsible for regulating the active (P_{out}) and reactive (Q_{out}) power flow, respectively. In addition, H-1 pairs of PI controllers, $C_{h\parallel}(s)$ and $C_{h\perp}(s)$, are responsible for selectively regulating the distortion quantities associated with each frequency component, $D_{h\parallel}$ and $D_{h\perp}$, that are further detailed herein.

The outputs of $C_p(s)$ and $C_q(s)$ are multiplied by unity in-phase and 90°-phase-shifted sinusoidal signals, $x_{1\parallel}$ and $x_{1\perp}$, respectively, whose frequency is equal to the fundamental component of the PCC voltage. These unit signals are generated by means of a distortion-robust PLL-based algorithm proposed in [26] and shown in the zoomed view of Fig. 3. The resulting active $i^*_{1\parallel}$ and reactive $i^*_{1\perp}$ currents are then added to compose the fundamental current reference $i^*_{1\parallel\perp}$. Fig. 3 shows the algorithm used to generate the sinusoidal signals and calculate the PQD power terms. For instance, the average active P_{out} and reactive Q_{out} powers are computed according to (3) and (4):

$$P_{out} = \frac{1}{T}\int_{t-T}^{t} v_{pcc}\cdot i_f \; d\tau \qquad (3)$$

$$Q_{out} = \frac{1}{T}\int_{t-T}^{t} v_{pcc\perp}\cdot i_f \; d\tau, \qquad (4)$$

where T is the fundamental period and $v_{pcc\perp}$ is the homo-integral of the PCC voltage [27], given by:

$$v_{pcc\perp} = \omega\int_{0}^{t} v_{pcc}\; d\tau \; - \; \frac{\omega}{T}\int_{t-T}^{t}\left[\int_{0}^{t} v_{pcc}\; d\tau\right] d\tau. \qquad (5)$$

This strategy may be replicated to other frequencies according to the application requirements and the number of harmonic components present in the grid voltage. It requires adding other pairs of PI controllers. Each of such pairs is responsible for regulating one harmonic frequency. For frequencies higher than the line frequency, $x_{h\parallel}$ and $x_{h\perp}$ are obtained by multiplying the output phase of the PLL

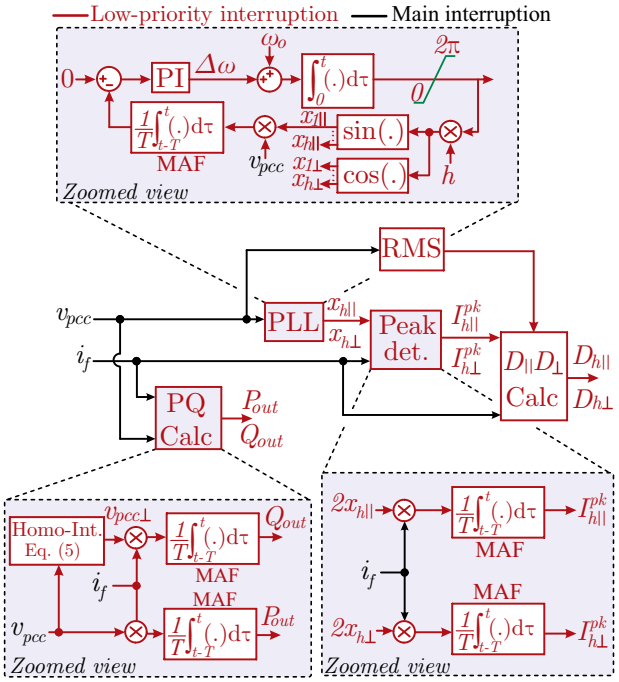

Fig. 3. Signal generation and PQD calculation algorithm.

algorithm by the h-th harmonic order, and subsequently obtaining its sine or cosine - see Fig. 3. The harmonic distortion quantities associated with each component, $D_{h\parallel}$ and $D_{h\perp}$, are computed for each frequency and quantified for the in-phase and quadrature components as shown in (6). Distortion power terms quantify the harmonic components (i.e., linear and non-linear) in the injected current. $I^{pk}_{h\parallel}$ and $I^{pk}_{h\perp}$ are the peak values of the in-phase and quadrature components of the filter current, i^*_f. The PLL algorithm used to generate $x_{h\parallel}$ and $x_{h\perp}$, as well as the peak detection block in Fig. 3, are detailed in [20]. V^{RMS}_{pcc} is the PCC RMS voltage. The PQD strategy is developed as sinusoidal current source synthesis, regardless of the grid voltage waveform [28].

$$D_{h\parallel} = V^{RMS}_{pcc}\cdot\frac{I^{pk}_{h\parallel}}{\sqrt{2}} \qquad D_{h\perp} = V^{RMS}_{pcc}\cdot\frac{I^{pk}_{h\perp}}{\sqrt{2}}. \qquad (6)$$

It is worth underlining that the PLL, root-mean square (RMS) calculation, and the algorithm to detect the peak values are based on moving-average filters (MAF) [29], implemented into a low-priority interruption (LPI) of the digital signal processing, as highlighted in Figs. 1(b) and 3. Such a LPI has its processing time set based on the highest harmonic order selection of the power controllers, to guarantee proper resolution for $x_{h\parallel}$ and $x_{h\perp}$ signals (i.e., at least twenty times the highest harmonic component).

A. Power controller tuning procedure

The sizing of the proposed power loops considers the closed-loop model shown in Fig. 4(a), which is obtained through the feedback of the PQD strategy shown in Fig. 1(b) and 3. Some prior assumptions are considered: (i) active, reactive, in-phase, and quadrature distortion power terms are orthogonal to each other, which allows independent controller tuning; (ii) the inner current loop is much faster than the outer

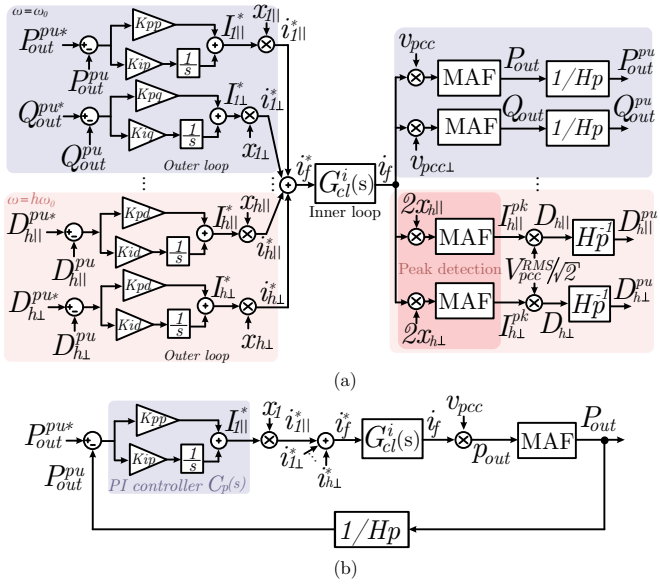

Fig. 4. (a) Closed loop control scheme highlighting the outer power and inner current loops. (b) Active power closed-loop control.

power loop (i.e., at least one/two decades above). Thus, the inner closed-loop TF $G^i_{CL}(s)$ can be considered as a static gain H_i; and (iii) the MAF used to compute the power terms and peak currents is modeled by a low-pass filter (LPF) with cut-off frequency (ω_c) equal to a quarter of the fundamental frequency [29].

The reactive and distortion power closed loops are the same compared to the active power loop, as shown in Fig. 4(a). Based on the aforementioned assumption (i) and without loss of generality, the active power closed-loop control in Fig. 4(b) is used to derive all the power controllers proposed herein. The instantaneous active power, p_{out}, considering the double multiplication ($x_{h\|}$ and v_{pcc}) is calculated as:

$$p_{out} = I^*_{1\|}\cdot x_{h\|}\cdot \overbrace{H_i}^{G^i_{CL}(s)} \cdot v_{pcc} = \frac{I^*_{1\|}\cdot V^{pk}_{pcc}\cdot H_i}{2}[1-\cos(2h\omega_0 t)], \tag{7}$$

where $x_{h\|} = \sin(h\omega_0 t)$, $v_{pcc} = V^{pk}_{pcc}\cdot\sin(h\omega_0 t)$, h = 1, V^{pk}_{pcc} is the grid voltage amplitude and $I^*_{1\|}$ is the output signal of $C_p(s)$. Eq. (7) comprises a constant part and an oscillatory part at twice the frequency of interest ($h\omega_0$). Since the MAF completely rejects the high-frequency components and the power controllers are tuned at least one decade below $2h\omega_0$, then only the average signal value is used for tuning the controller. Therefore, the non-compensated open-loop TF of the power control from Fig. 4(b) is written as:

$$G^P_{OL} = \frac{P^{pu}_{out}}{I^*_{1\|}} = \frac{p_{out}\cdot \mathrm{MAF}}{H_p}\cdot H_i = \frac{V^{pk}_{pcc}}{2H_v}\frac{\overbrace{\omega_c}^{\mathrm{MAF}}}{s+\omega_c}, \tag{8}$$

where p_{out} is given by the DC value of (7), $H_p = H_v\cdot H_i$ and H_v are the power and voltage per-unit base gains, respectively. As the main objective of the power loops is to reject steady-state source disturbances and the power terms are naturally DC quantities, the proposed control loops inherit much lower bandwidth than $G^i_{CL}(s)$ and $2h\omega_0$, as discussed in assumption (ii). The MAF algorithm dominates the dynamics of the power control loops in (8), irrespective of the frequency order - refer to assumption (iii). On this basis, the same K_{pp} and K_{ip} gains are used for all the power controllers.

B. DER output impedance for the PQD control strategy

This section derives the output impedance Z_{out} of the power-commanded DER, considering the proposed PQD strategy loops. Referring to Fig. 4 and considering a steady-state condition, the outputs of power PI controllers (i.e., $I^*_{h\|}$ and $I^*_{h\perp}$) are time-invariant. In the frequency domain:

$$I^*_{h\|}(s) = I^*_{h\|}\overbrace{\frac{h\omega_0}{s^2+(h\omega_0)^2}}^{\mathcal{L}\{\sin(h\omega_0 t)\}},\ I^*_{h\perp}(s) = I^*_{h\perp}\overbrace{\frac{s}{s^2+(h\omega_0)^2}}^{\mathcal{L}\{\cos(h\omega_0 t)\}}, \tag{9}$$

where $I^*_{h\|}(s)$ and $I^*_{h\perp}(s)$ are the h-th in-phase and quadrature TFs of the time-varying references $i^*_{h\|} = I^*_{h\|}\cdot\sin(h\omega_0 t)$ and $i^*_{h\perp} = I^*_{h\perp}\cdot\cos(h\omega_0 t)$. From equations (8) and (9), the non-compensated open-loop TFs of the in-phase $G_{OL\|}(s)$ and quadrature $G_{OL\perp}(s)$ loops are given by:

$$G_{OL\|}(s) = \frac{V^{pk}_{pcc}\cdot\mathrm{MAF}}{2H_v}\frac{h\omega_0}{s^2+(h\omega_0)^2}, \tag{10}$$

$$G_{OL\perp}(s) = \frac{V^{pk}_{pcc}\cdot\mathrm{MAF}}{2H_v}\frac{s}{s^2+(h\omega_0)^2}, \tag{11}$$

which emulate a PR controller TF with zero damping factor tuned to $h\omega_0$. Fig. 5 shows the block diagram relating v_{pcc} and i_f with the PQD strategy, in which the output impedance Z_{out} is calculated by:

$$Z_{out}(s) = -Z_f(s) - \frac{F(s)}{H_i}\left(1+\sum G^{P,Q,D}_{OL}\cdot C_{p,q,d}\right), \tag{12}$$

where $C_{p,q,d}$ are the power loop controllers, $G^{P,Q,D}_{OL}$ are the non-compensated open-loop TFs of the proposed strategy, and $F(s) = \mathrm{PWM}\cdot G_{conv}\cdot C_i$. The proposed PQD power loops selectively increase the DER output impedance, without susceptibility to the pole-clustering effect by truncation, normalization or quantization observed in the resonant-controller coefficients in fixed-point DSPs.

IV. Simulation Results

The parameters used in the simulation model and experimental setup are shown in Table I. Simulations are conducted in PLECS® platform. The LPI (i.e. Timer0)

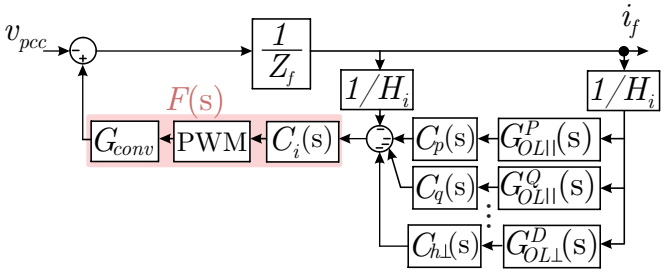

Fig. 5. Z_{out} block diagram considering the PQD loops.

TABLE I
PARAMETERS OF THE *grid-following* CONVERTER.

Parameter	Symbol	Value	
Nominal power	S_{nom}	1.5	kVA
Grid voltage	V_g	127	V
Filter inductance	L_f	2.0	mH
Filter ESR	R_f	0.2	Ω
Filter capacitor	C_f	6.6	μF
Filter resonance freq.	f_{res}	1385	Hz
Grid inductance	L_g	2	mH
Grid resistance	R_g	0.92	Ω
DC bus voltage	V_{DC}	311	V
Carrier amplitude	C_{pk}	2	-
Fundamental grid frequency	f_0	60	Hz
Switching frequency	f_{sw}	24	kHz
MI sampling frequency	f_s	24	kHz
LPI sampling frequency	f_{sl}	8.4	kHz
Set of harmonic orders	H	$\{1,3,5,7\}$	-

TABLE II
PARAMETERS OF THE CURRENT/POWER CONTROLLERS.

Parameter	Symbol	Value	
P Gain - curr.	K_{pi}	0.7990	Ω
I Gain - curr.	K_{ii}	0.0320	F^{-1}
P Gain - power	K_{pp}	0.8577	V^{-1}
I Gain - power	K_{ip}	0.0066	A/J
Cut-off freq. (I)	f_{ci}	1000	Hz
Cut-off freq. (P)	f_{cp}	10	Hz
Phase margin (I)	PM_i	60	deg.
Phase margin (P)	PM_p	75	deg.
I measurement gain	H_i	20	A
V measurement gain	H_v	400	V
P measurement gain	H_p	4000	W

frequency is configured to 8.4 kHz (7·60·20, where 20 samples guarantee proper resolution for $x_{7\parallel}$ and $x_{7\perp}$). Table II shows the parameters of the PI controllers and transducer gains. All control loops are developed in per-unit (pu) values.

A. DER output impedance evaluation

To evaluate the theoretical small-signal linear models calculated by (2) and (12), switched converter model simulations are conducted, and, then, tests are repeated experimentally. In both cases, the converter output impedance is measured considering the inner control loop and the proposed cascade control (PQD and inner control loops) according to the following procedure: a grid voltage disturbance at a specific frequency is applied to the PCC, and the controlled current and PCC voltage are measured. By applying an offline FFT (Fast Fourier Transform) to the voltage and current waveforms for analysis purposes, the magnitude and phase of each harmonic component are determined and Z_{out} is calculated. This process is repeated for a wide frequency range and the results are shown in Fig. 6.

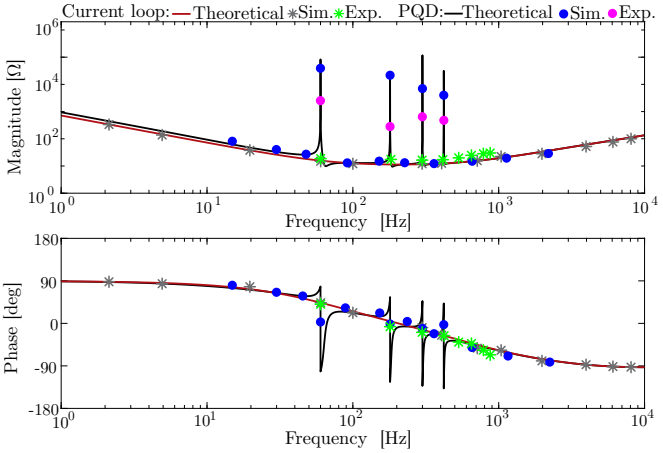

Fig. 6. Theoretical, simulated and experimentally measured output impedance (Z_{out})

The grey and green measured dots show the DER output impedance of the current-driven inverter for simulated and experimental evaluation, respectively. The blue and magenta dots show the DER output impedance for the proposed power-commanded inverter. In all cases, the experimental and simulated results match the theoretical models.

B. Impedance-based stability analysis

The stable operation must be ensured for both stiff and weak grids. The SCC at the PCC is an index commonly used to measure grid stiffness, which is defined by:

$$\text{SCC} = \frac{(V_{pcc}^{RMS})^2}{Z_g}, \tag{13}$$

where Z_g is the grid line impedance. Weak and stiff grids are characterized by SCC $\leq$ 190 kVA and SCC $\geq$ 760 kVA, respectively [30]. Figure 7 shows the Norton circuit-equivalent model of the power-commanded DER connected to the grid, where the relationship between i_f, power references, and v_g can be derived. G_{CL}^i is the current control closed-loop TF, obtained from (1). Z_{out} is the DER output impedance calculated in (12), Z_c is the filter capacitor impedance, and g(s) describes the ratio i_f^* by the power references:

$$g(s) = \frac{C_{p,q,d}}{1 + G_{OL}^{P,Q,D} \cdot C_{p,q,d}}. \tag{14}$$

Fig. 8(a) shows the main closed-loop poles $G_{CL}^{p,q,d} = i_f/v_g$ of the PQD strategy with active/reactive and distortion H=$\{1,3,5,7\}$ power loops, considering a wide range of grid SCC variation (8∼800 kVA). As noted, the stability margins of the system are reduced as the grid SCC decreases. For a SCC of approximately 8.8 kVA, the system becomes unstable due to the pole crossing to the right s-half plane, as shown in the zoomed view of Fig. 8(b).

Fig. 8(c) shows the stability curve as a function of h-th selective power loops. The stable and unstable operating regions of the PQD strategy are highlighted. More distortion power loops reduce the stability range of the PQD strategy (i.e., lower robustness). This shows a trade-off between increasing the set of H and preserving the system stability. Particularly for H=$\{1,3,5,7\}$, the critical stability occurs for low SCC of 8.8 kVA, which indicates high robustness to the PQD control.

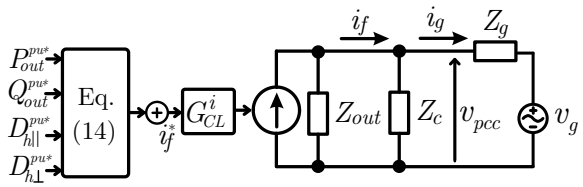

Fig. 7. Norton circuit-equivalent model of the proposed power-commanded DER.

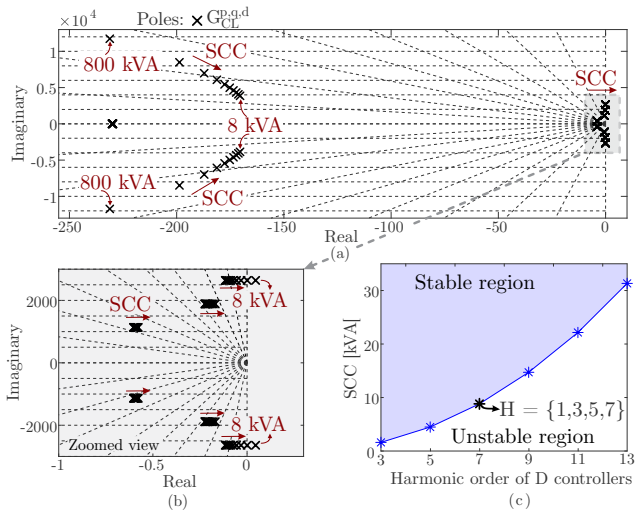

Fig. 8. Stability analysis of the proposed PQD strategy to grid SCC variation set to H={1, 3, 5, 7}. (b) Zoomed view of the poles crossing to the right side of the s-half plane. (c) Stability limit curve over different sets of H.

C. Sampling frequency analysis

As shown in (2), the DER Z_{out} is proportional to the PWM TF, being susceptible to changes on the sampling frequency. Fig. 9 shows the DER output impedance analysis for different values of f_s, while f_{sw} and f_{ci} are kept constant. The Tustin virtual-discretization method is employed. Z_{out} is slightly modified according to the sampling frequency, but there is no significant output impedance improvement even considering f_s equal to eight times f_{sw}. Although using a faster controller would improve the converter output impedance, f_{ci} cannot be increased any further because of hardware limitations.

D. PQD control in PV applications

In the simulated scenario of Fig. 10, the grid voltage is set according to the individual voltage harmonic limits described at IEEE std. 519. Fig. 10(a) shows the converter operation on the P-V curve of the PV array, for both strategies: (1) without (i.e., single-loop PI current control) and (2) with the proposed PQD control. For suitable comparisons, the same inner loop controller is employed for both cases. The simulated

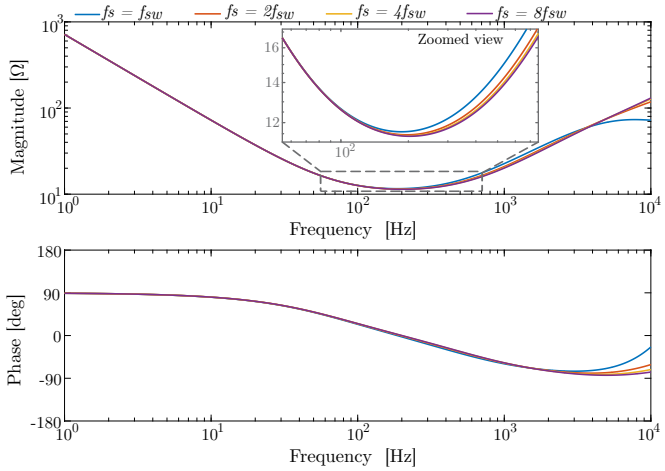

Fig. 9. Z_{out} curves over variations of sampling frequency considering both switching frequency and current controller bandwidth constant.

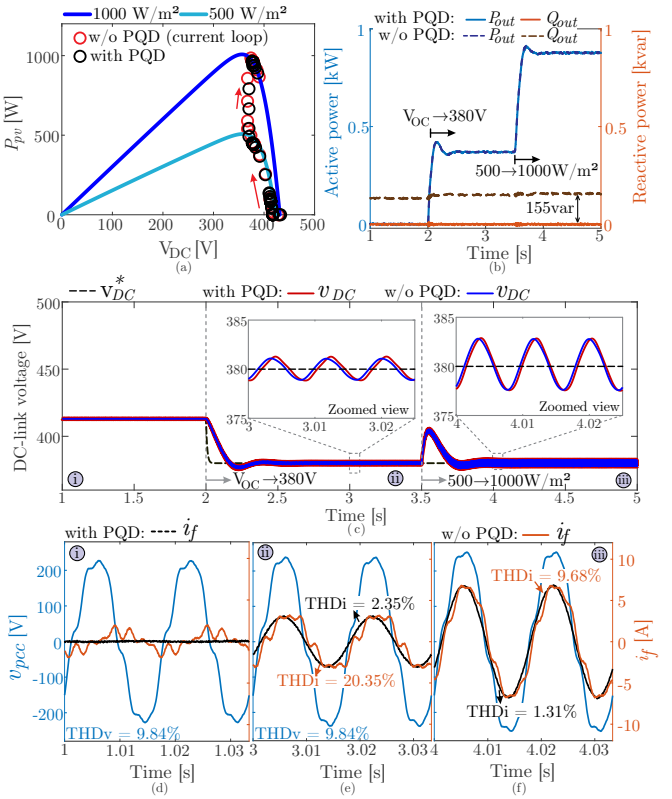

Fig. 10. (a) P-V curve of the PV array and the respective operating points computed by the control with and without PQD control. (b) Active and reactive power injected into the grid for both strategies. (c) Dynamic response of DC-link voltage control during variations in v_{DC}^* and solar irradiance for both strategies. (d)-(f) Current response of conventional and proposed control under distorted PCC voltage.

events are the same for both strategies and consist of: (i) v_{DC}^* is initially set to the PV array open-circuit voltage (v_{DC} = 414 V), operating under solar irradiance of 500 W/m^2 and ambient temperature of 25 °C; (ii) at instant t = 2 s, v_{DC}^* is ramped down to 380 V, following the PV array curve up to its maximum power point (MPP); (iii) at instant t = 4 s, a sudden change in the solar irradiance from 500 to 1000 W/m^2 occurs, while the DC-link voltage reference is kept at 380 V.

As noted in Fig. 10(a), the behavior in terms of active power drained from the PV array is similar for both control strategies, which is also shown in Fig. 10(b). However, due to the absence of a fundamental-frequency quadrature controller (i.e., reactive power), the grid voltage disturbs considerably the conventional single-loop strategy at about 155 var. Fig. 10(c) shows the controlled DC-link voltage with and without the PQD control. As highlighted in the zoomed views, the DC-link voltage is well-controlled for both strategies.

Figs. 10(c), (d), and (e) show the PCC voltage and the injected currents for both control strategies during intervals (i), (ii) and (iii), respectively. Regarding the conventional single-loop control, the injected current is heavily disturbed by the distorted grid (i.e., low stiffness). Whereas in the PQD control, the inverter injects practically sinusoidal current, suffering low effect in the current waveform in the selected frequencies. The current THD values are reduced from 20.35% and 9.68% to 2.35% and 1.31% for 2< t ≤3.5 s and 3.5< t ≤5 s, respectively.

It is worth underlining that the current THD results in Figs. 10(e)-(f) could be improved for the single-loop PI current control by increasing the controller bandwidth. However, the interaction between the LC filter and the equivalent grid impedance yields a resonance at 1.38 kHz, restricting the cut-off frequency for both strategies to a low value. Since the proposed PQD strategy employs the same inner loop as the single-loop PI current control, the THD comparisons in Figs. 10(e)-(f) are fair and suitable, reinforcing the valuable contributions of the proposed strategy.

V. Experimental Results

A commercial 1.5 kVA single-phase PV inverter, model 1500-NS, manufactured by PHB Solar, is employed. The DC link is powered by a DC voltage source and the AC side is formed by a programmable AC voltage source (*Pacific Power, 354-ASX*). The voltage and current measurements are obtained from a Tektronix DPO 2014B oscilloscope equipped with A612 and P5200A probes. The PQD strategy is programmed in the Texas Instruments 60 MHz 32-bit TMS320F28034 low-cost fixed-point DSP.

A. PQD control strategy for coordinated control applications

As a benchmark, the single-loop PI current control is implemented on the experimental setup, and the system is connected to the grid. Afterward, the power loops are inserted and the results are compared. Due to the inherent grid conditions, the PCC voltage is distorted with a significant presence of 3rd, 5th, and 7th harmonics, which indicates the implementation of distortion power loops at these frequencies. Fig. 11 shows the PCC voltage and disturbance currents when i_f^* is set to zero without PQD control strategy enabled, while Fig. 12 shows the same currents when the proposed PQD loops are implemented. In both cases, the inverter has the same switching frequency and the current controller has the same design. The improvement is due to the intervention on the current reference signal, provided by the proposed PQD power loops.

The FFT of these waveforms is shown in Table III. Note that there is a significant reduction in harmonic circulation. Although there is still a small grid current due to the filter capacitor, there is almost no disturbance in the filter current, showing that the power loop enhanced the system Z_{out}.

Fig. 13 shows the filter current when a step in the power reference of 600 W is applied to the active power loop. Fig. 14 shows the zoomed view of the voltage and current waveforms in steady-state for a reference of 800 W. Fig. 15 shows the transient when a step in the Q reference equal to 600 var is applied to the Q control loop after the system is already injecting 600 W. After the system reaches the steady state, the grid current THD is equal to 3.58%. In all cases, the references of the harmonic control loops are zero to reduce the THD value of the grid current.

B. Main interruption execution time comparison

It is common practice to implement the current control using PI-R or multi PI-R (PI-MR) controllers [31], [32] in the MI for single-phase *grid-following* inverter. However, it adds computational complexity when compared to PI controllers.

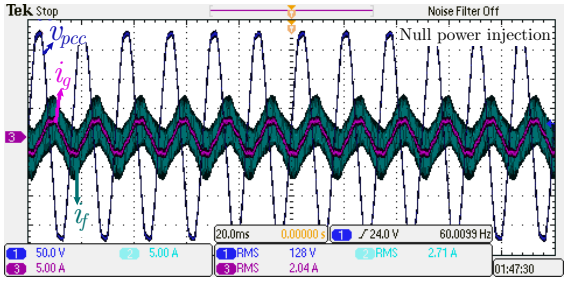

Fig. 11. Disturbance current with single-loop PI current control.

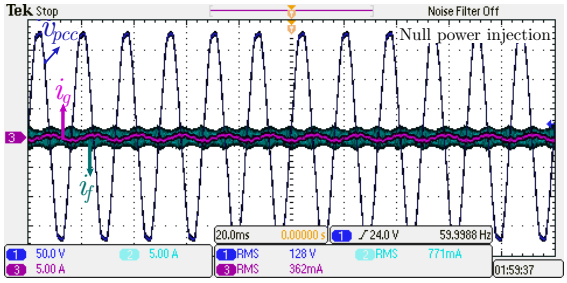

Fig. 12. Disturbance current with PQD control.

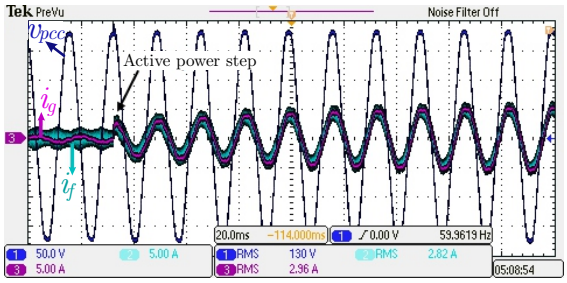

Fig. 13. Filter and grid current for a step of 600 W in P_{out}^*.

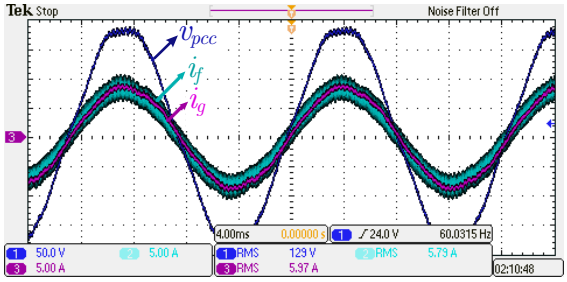

Fig. 14. Filter and grid current for P_{out}^*= 800 W (THD = 3.91%).

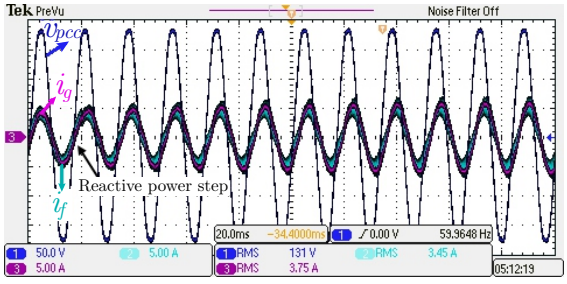

Fig. 15. Filter and grid current for a step of 600 var in Q_{out}^*.

The measured MI execution times of both controllers are shown in Table IV. The execution time for the analog-to-digital (A/D) conversion, without any control calculation, is also reported. Note that the increase of the execution time for the PI, when compared to the A/D conversion alone, is 16.67%

TABLE III
COMPARISON OF CURRENT SPECTRUM COMPONENTS.

Component	Amplitude [%]			
	Curr. Control		PQD Control	
	i_f	i_g	i_f	i_g
1	11.64	14.36	0.37	2.32
3	0.15	0.17	0	0
5	0.79	1.05	0.11	0.45
7	0.37	0.50	0.09	0.29
f_{sw}	13.74	0.75	4.74	0.32

TABLE IV
COMPARISON OF EXECUTION TIME.

Test	Execution time (μs)
A/D conversion	7.28
PI control	9.88
PI-R_{60Hz} control	10.40
PI-MR control	13.52
Signal generation	18.84

less than the PI-R_{60Hz} (only 60 Hz). Also, the PQD control requires 3.64 μs less MI processing time than the PI-MR for the same set H.

Regarding the PQD strategy, the signal generation algorithm shown in Fig. 3 is part of the code that demands the highest processing time, as shown in Table IV. Nonetheless, it does not have to be executed within the MI. Moreover, it is executed in a lower priority interruption with a lower processing frequency, since the power loop has very slow dynamics. In addition to the flexibility offered by the proposed power-based control, the proposal alleviates the computational burden of fast main control interruptions processed by the DSP since the PI controller is computationally less expensive than multi PI-R controllers. This advantage of the proposed strategy allows the use of low-performance and low-cost DSPs, such as those used in commercial PV inverters.

VI. CONCLUSION

This paper proposed the double-loop selective PQD control structure for single-phase *grid-following* inverter-based DERs. Its mathematical model and physical behavior were explained in detail and validated by simulation and experiments. It was shown that the proposed control accurately tracks the power and current references, achieves good results with low distortion values in steady-state, rejects disturbances even under heavily distorted grid voltage, proved resilient to grid short-circuit level variations, and can be used for coordinated control and PV applications. Also, the proposed selective PQD control strategy uses 26% less computational processing time within the main interruption than the conventional approaches, requiring no hardware changes and allowing a straightforward retrofit of the current DER technology.

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