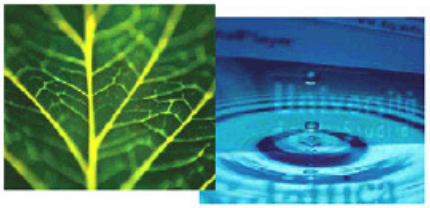
PhD Dissertation



International Doctorate School in Information and Communication Technologies

DISI - University of Trento

Design and characterization of SPAD based CMOS analog pixels for photon-counting applications

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Abstract

Recent advancements in biomedical research and imaging applications have ignited an intense interest in single-photon detection. Along with single-photon resolution, nanosecond or sub-nanosecond timing resolution and high sensitivity of the device must be achieved at the same time. Single-Photon Avalanche Diodes (SPADs) have proved their prospectives in terms of shot-noise limited operation, excellent timing resolution and wide spectral range. Nonetheless, the performance of recently presented SPAD based arrays has an issue of low detection efficiency by reason of the area on the substrate occupied by additional processing electronics.

This dissertation presents the design and experimental characterization of a few compact analog readout circuits for SPAD based arrays. Targeting the applications where the spatial resolution is the key requirement, the work is focused on the circuit compactness, that is, pixel fill factor refinement. Consisting of only a few transistors, the proposed structures are remarkable for a small area occupation. This significant advancement has been achieved with the analog implementation of the additional circuitry instead of standard digital approach. Along with the compactness, the distinguishing features of the circuits are low power consumption, low output non-linearity and pixel-to-pixel non-uniformity. In addition, experimental results on a time-gated operation have proved feasibility of a sub-nanosecond time window.

Keywords
[CMOS, SPAD, image sensor, analog circuit, readout electronics]

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Chapter 1

Introduction

The present chapter comprises the context of the thesis work together with a brief discussion and description of the faced design challenges and proposed solutions. Additionally, the innovative aspects of the research and its distinctive features are summarized. With a short description of each chapter the structure of the thesis is outlined.

1.1 The Context

At the present time a particular attention is focused towards non-destructive and non-invasive measurements with optical techniques. Photon counting applications are becoming popular due to many possible application areas such as astronomy, chemical, material analysis, biomedical research and imaging methods as well as the most recent area of quantum cryptography. Lately a significant improvement has been achieved in the fluorescence analysis of the structure and function of biological molecules.

For some applications (3D imaging, Positron Emission Tomography and Fluorescence Lifetime Imaging) each single photon must be detected. Without affecting the properties of the sample, low light level detection allows high precision and high sensitivity measurements. Thus, these measurements are widely used for cell qualitative and quantitative analysis by

detecting fluorescence emitted from cells labeled with a fluorescent dye. In clinical testing and medical in-vitro diagnosis photon counting technique is used for blood analysis, blood cell counting, hormone inspection and diagnosis of cancer and various infectious diseases. In addition, fluorescence and luminescence measurements are used for rapid hygienic testing and monitoring processes in inspections for bacteria contamination.

For these low-level light applications single-photon resolution is not the only requirement. The detector has to possess picosecond timing resolution and at the same time high sensitivity as the signal may consist only a few photons per emission. Along with that, the device must provide an intrinsic amplification to allow the subsequent signal processing.

Currently, there exist several devices ensuring detection of single photons. Photomultiplier tubes (PMTs) multiply electrical current from free carrier using dynodes in their structure. The dynodes also may be implemented as channels, known as microchannel plates (MCPs). These two types of single-photon counters are still the most used detectors assuring high single-photon detection efficiency and high timing resolution at the same time. The detector efficiency of PMT is about 35% for the whole visible range. Cooled with scintillators, PMTs are also used as radiation detectors in positron emission tomography. However, by reasons of the high cost, fragility, sensitivity to external magnetic field, their exploitation is limited to very specific applications. Moreover, a high voltage supply of 1-2 kV is required for the proper operation.

Charge-coupled devices (CCDs) were the first solid-state imager. The operating principle is based on photon-generated charge transfer between MOS capacitors. In order to achieve single-photon resolution, an additional amplification stage and readout should be designed. Such a structure is called an electron-multiplying CCD (EMCCD). CCDs are not autonomous, thus, their use is restricted for some applications. Along with that, the

device requires an additional cooling system in order to decrease the noise to acceptable levels.

An active-pixel sensor (APS) contains a photodetector and an amplifier used to amplify the photon-generated signal before the conversion into digital signal. Typically, an APS structure is formed of p-n or p-i-n reversely biased junctions. The benefit of implementation in CMOS technology is a relatively low cost of devices. However, these sensors do not have sufficient time-resolution and sensitivity.

Linear-Mode Avalanche Diodes (APDs) allow amplification of photon-generated carriers due to ionization, caused by high electric field into p-n junction of the diode. The applied operating voltages are near the breakdown values. The number of carriers is directly proportional to the number of detected photons. For single-photon counting APDs lack for timing accuracy and suffer from quite large non-uniformities.

Single Photon Avalanche Diode (SPAD) based devices are currently gaining the research interest as a perspective alternative solution to PMTs. The reason of such an interest is the excellent timing resolution of the detector that reaches a few tens of picoseconds. Along with that, SPADs have significantly higher quantum efficiency and a large measurement range from 300 nm to the near infrared.

SPAD is a photodiode biased above its breakdown voltage operating in the so-called Geiger-mode. The structure of the diode is specially designed to detect photons. It contains an active sensitive area and a guard ring that is used to prevent edge breakdown. The single-photon resolution is attainable due to the impact ionization effect taking place into the bulk of the device. Each single photon hitting the active area of SPAD may trigger a self-sustaining avalanche current of up to the mA range. This current continues flowing until the voltage across the junction drops close to the breakdown value, causing the avalanche to be quenched. Thus, dur-

ing this reset time the detector remains insensitive to impinging photons. To sustain the diode operating conditions, restore the bias voltage and prevent damage of a SPAD, an additional quenching circuit is required. The circuit functions are:

- to sense the leading edge of the avalanche current;
- to generate an output pulse corresponding to the avalanche current;
- to quench the avalanche, that is, lower the excess voltage down to the breakdown voltage;
- to restore the photodiode to the operative level, that is, bias the diode to a voltage above the breakdown.

The first SPADs were fabricated in a dedicated planar-silicon process. Recently, SPADs have become feasible for assembling into arrays in CMOS technology. Although CMOS process is initially not tailored for SPAD fabrication, due to technology optimization a few very successful designs have been lately demonstrated [1, 2, 135]. This breakthrough of CMOS technology employment has allowed the additional circuitry, which is necessary for SPAD quenching, data storage and signal processing, to be fabricated inside the pixel. Along with the compactness and high functionality, the design has also greatly lower cost.

Since the 2000s many SPAD arrays have been presented with the design targets on picosecond response and time-gated operation. In spite of the achieved high performance, there are still a number of issues which should be addressed in image sensor design. The common drawback of SPADs is their low fill factor.

1.2 The Problem

Even though there are several devices showing single-photon resolution, their exploitation is limited for mass-production typically by reason of high cost. Not least importance has the requirement of the intrinsic gain provided by the device and device uniformity. Among the aforementioned perspective devices, the most promising imagers in terms of sub-nanosecond timing accuracy, robustness and cost at the same time are SPAD based arrays.

However, a few issues should be addressed in the arrays performance for wide-field applications. Analysis of the related latest work on SPAD arrays design reflects an issue of a small pixel fill factor. Fill factor is restricted by both the SPAD guard ring and the additional circuitry.

To improve the pixel fill factor the area occupied by the guard ring was shrunk [2]. In addition, an array of optical microlenses aligned with a SPAD array can be employed to recover the fill factor [3, 9]. Nevertheless, the good yield and uniformity remains an unsolved issue until now.

Shrinking dimensions in CMOS technology could be exploited to minimize the circuitry area and increase the in-pixel functionality at the same time. Lately there have been several arrays implemented in 0.13 μm CMOS technology. Each photon detected by SPAD corresponds to an event which should be stored and processed. To transmit the data a very wide bandwidth is required introducing additional parasitic noise. However, this wire parasitic capacitance can be eliminated with in-pixel design. This leads to further reduction of pixel fill factor. Signal processing in SPAD arrays is usually based on Time-To-Digital Converters and in-pixel digital counters. Typically, digital implementation consists of a few hundreds of transistors thus limiting the effective photosensitive area to a few percent. This fact is evident in 2-D arrays [5, 6, 73, 120]. The fill factor achieved in linear

arrays is slightly better [2, 7, 8]. However, the area occupied by the circuitry is still much larger compared to the detector active area. In other words, whereas a high timing resolution is an absolute benefit of SPADs, low sensitivity worsens the array performance.

1.3 The Solution

In this thesis the challenge of low fill factor of SPAD based image sensors is addressed. Analysis of the related work suggests that additional in-pixel electronics should be revised. One of the possible approaches to minimize the electronics area on chip is technology scaling. A CMOS array fabricated in scaled technology benefits smaller pixel size, increased resolution and more functionality integrated on the same chip with the detector.

Along with this, the research is focused on the design of analog in-pixel readout for photon counting. Whereas a standard digital implementation is area consuming, an analog circuit can consist of only a few transistors. At the same time, on the assumption of careful design, analog approach can assure the accuracy comparable to the digital implementation. At the present time only few studies have been carried out on the analog readout circuit design [143, 144, 145, 146]. Nonetheless, the first results have proved an increase of the pixel fill factor [143] and, hence, the overall array detection efficiency.

This thesis presents the design and experimental characterization of several compact analog in-pixel readout circuits for photon counting. A number of preliminary simulations have been performed in CAD to evaluate and adapt the circuit performance. The first results have held considerable promise, the circuits have been assembled into arrays and manufactured in a standard 0.15 μm CMOS technologies. Along with the compactness, the design goal was in-pixel functionality. Each pixel is comprises a SPAD,

a quenching circuit, a time gating circuit and an analog counter. Based on different operating principles, the number of detected photons is proportional to the voltage decrease at the circuit's output. Aiming a wide dynamic range, some proposed structures have a programmable resolution which can be tuned externally. Additionally, the design was targeted at low power consumption, good output linearity and high pixel-to-pixel uniformity. Also it is necessary that electronic noise of the circuit be low, so that the signal could be easily derived from the noise background.

The Ph.D. thesis also reports on the experimental characterization of an array of CMOS analog counters. An array of 20×20 has been manufactured in a standard 0.35 μm CMOS technology. The circuit delivers an output voltage proportional to the input pulse count, with a programmable voltage step. The resolutions of 7 or 8 bits with a low readout noise and low output non-uniformity across the array have been measured. Both the integral and differential non-linearities are comparable to digitally implemented counters. In addition, the circuit has a small power consumption, which is one of the key parameters for large array assembling.

The analysis of the proposed designs proved analog readout to be a good alternative for in-pixel signal processing in SPAD based image sensors of high-spatial resolution.

1.4 Innovative Aspects

This research expands the scope of analog circuits exploited as in-pixel processing circuitry. The proposed solution would bring significant improvements to the state-of-art approaches.

It is required that an additional circuitry be placed with SPAD in pixel in order to minimize parasitic connections. The basic functions to be performed are SPAD quenching, time gating, photon counting and storage

of the data.

First of all, given the experimental results, the analog implementation has achieved characteristics comparable to digital standard circuits.

Programmability of the output is a certain benefit of an analog counter that has been tested for the Ph.D. It has shown a low non-uniformity, a low readout noise and low output non-uniformity across the array at resolutions of 7 and 8 bits.

Thus, a certain advantage of the second structure reported in Chapter 3.2 is its programmable output, that is, programmable resolution. This means that the circuit can be easily tailored satisfying any particular demands of applications. This circuit can be particularly efficient for the applications where a high output linearity is a key requirement.

The circuit structure described in Chapter 3.3 has a benefit of a low electronic readout noise which remains constant during the acquisition time. This design is remarkable due to a low non-uniformity among the pixels (only 1%). Moreover, the time gating function realized within the circuit achieves sub-nanosecond resolution.

The forth stricture presented in section 3.4 has shown an output non-linearity of 3.7% and an electrical non-uniformity among the pixel of 3.5%.

Compared to the former designs, all four structures presented in this dissertation are notable for their compactness. The area occupation of this analog implementations (less than $300\mu m^2$) is a factor 10 smaller than a digital counter of the same resolution [73].

Along with this, in virtue of a low power consumption per pixel assembling of large arrays of detectors becomes feasible.

These characteristics are well-suited for single-photon counting applications. Therefore, the circuits can be suggested as in-pixel counters for SPAD based image sensors for wide-field applications.

1.5 Structure of the Thesis

The structure of this dissertation is following. In Chapter 2 the main light properties are presented together with the figures of merit of semiconductor photodetectors. Then, a brief historical overview of image sensors development is given, including the evolution both in the technology and sensor architecture. The structure, main characteristics and prospectives of CMOS SPADs as photodetectors possessing single-photon resolution are presented. The most important figures of merit of imaging sensors are introduced. The developed SPAD arrays used for photon-counting applications are discussed with the main interest focused on the implementation of the addition in-pixel circuitry. Finally, an overview of existing attempts towards the SPAD based sensors of high spatial resolution are analyzed.

Chapter 3 reports on the design of several analog readout circuits for SPAD arrays to be implemented in a standard CMOS technology. The main target of these designs was circuit compactness. Additionally, the main challenges for the development are also discussed in this Chapter. The circuits design and their operating performance are described in detail. In addition, the circuits' preliminary characterization performed by means of numerical simulations in CAD is shown. The configurations satisfying the set goals are presented.

The design of the test array and the experimental setup are discussed in Chapter 4. An external electronics is required for the following data transfer and processing and signal triggering. Hence, row and column decoders and window gating circuit have been implemented in chip. Chip architecture and chip layout are also presented. The test setups used for the electro-optical characterization is described.

The pixel design and experimental characterization of the fabricated CMOS linear test arrays are reported in Chapter 5. The architecture of

each pixel, including a SPAD, a quenching circuit, a gating circuit and an analog readout are presented. The results of an electro-optical characterization of the arrays are discussed. The main characteristics of the circuits response are given. Along with the architecture and characterization of designed pixels, the characterization of a large array of counters has been carried out and the results are also described.

Finally, Chapter 6 contains a critical analysis of the achieved results. The comparison with the related works is presented. This Chapter also contains the ideas for further possible improvement of the analog circuits in order to meet all requirements for single-photon counting applications.

Publications Related to the Ph.D. research

- E. Panina, G.F. Dalla Betta, L.Pancheri and D.Stoppa, Design of CMOS gated analog readout circuits for SPAD pixel arrays, PRIME 2012 8th Conference on Ph.D. Re-search in Microelectronics, Aachen, Germany, June 12-15, pp. 39-42, 2012.
- E. Panina, L. Pancheri, L. Gasparini, G.F. Dalla Betta and D. Stoppa, Compact CMOS analog readout for photon counting applications, SPIE Optics+Optoelectronics 2013, Prague, Czech Republic, April 15-18, 2013.
- L. Pancheri, E. Panina, G.F. Dalla Betta, L. Gasparini, D. Stoppa, Compact analog counting SPAD pixel with 1.9% PRNU and 530 ps time gating, ESSCIRC 2013, Bucharest, Romania, 16-20 Settembre, 2013.
- E. Panina, L. Pancheri, N. Massari, G.D. Dalla Betta, D. Stoppa, Compact CMOS ana-log counter for SPAD pixel arrays — accepted for publication in the Transactions of Circuits and Systems II.

Chapter 2

State-of-the-Art

2.1 Light Detection: Properties of Semiconductor Photodetectors

A photodetector is an electronic device, which detects photon flux transforming the photon energy into an electric charge or voltage on its output [22, 23]. The detection principle is based on one of these two effects: thermo- or photo-electric effect. Thermal detectors convert the photon energy into heat. However, these devices are rather unsuitable for many photonic applications by reason of a relatively long time needed for their temperature change. The photoelectric effect occurs in several materials due to photon absorption, which cause mobile charge carriers generation and, therefore, an electric current flow. Photon detectors can be subdivided in three main classes accordingly to the physical effect of the detector response:

- Photoconductive: the photogenerated carriers stay inside the material lattice and increase its conductivity as a function of the impinging light intensity (photoconductivity process);
- Photovoltaic: a voltage is generated over a semiconductor p-n junction when optical energy impinges the device (photoelectric emission);

– Photoemissive: incident photons release electrons from the surface of the detector.

The internal photoelectric effect is the basis of operation of many silicon photodetectors. The energy of light can be transferred to the electrons into the valence band. The effect can be divided into three basic processes. During the first one – generation – photons, quanta of electromagnetic energy, are absorbed and generate electrons and holes. These two carriers flow into different directions, thus, causing a current flow (transport process). In order to travel through the bandgap E_g and generate an electron-hole pair, photons should have a sufficient energy E_{ph} at wavelength λ $[\mu m]$ and frequency ν

$$E_p h = h\nu = \frac{hc_0}{\lambda} \geq E_g, \tag{2.1}$$

where $h = 6.626 \cdot 10^{-34}\ J \cdot s$ is Plancks constant, $c_0 = 3 \cdot 10^8\ m/s$ is the speed of light in vacuum. The shorter the wavelength, the more energy each photon contains. Only the photons with the energy E_{ph} equal or exceeding the bandgap energy of semiconductor E_g can be absorbed. In this case, the photon absorption excites the electron from the valence band into the conduction band. As a result, one electron-hole pair is created. The generated current can be detected in the external circuit. The generated electrons and holes under a large electric field may liberate more electrons and holes within the device by a process of impact ionization [22]. This internal amplification process increases the detector responsivity. Several photodetectors are capable for amplification of the photocurrent.

Another important parameter for photodetectors is the optical absorption coefficient α, which represents the capability of the detectors material to absorb photons and generate photocurrent. The optical absorption

coefficient α depends on the semiconductor used for the detector fabrication and the light wavelength. It determines the light penetration into the bulk, which decreases with the depth, therefore, the light intensity I can be described with Lambert-Beers law:

$$I(x) = I_0 \exp(-\alpha x). \tag{2.2}$$

where I_0 is the initial beam light intensity. At present, silicon is the most important material among other semiconductors in terms of cost and technological effectiveness despite the relatively low optical absorption coefficient and optical range confined in the visible and near infrared spectrum.

2.2 Figures of Merit of Photodetectors

There are several parameters, so-called, figures of merit, which are used to estimate the photodetector performance [24].

– *Quantum efficiency* η $(0 \leq \eta \leq 1)$ of a photodetector is the probability that a single photon coming into the bulk of the device generates an electron-hole pair that contributes to the photocurrent. In other words, η reflects the efficiency and sensitivity of the device to the incident optical energy. Not every photon impinged on the device contributes to the current because of a few possible reasons:

  a) the probabilistic nature of the absorption process;

  b) reflection from the device surface;

  c) recombination process (mainly near the detector surface);

  d) detector active area limitations (more related to the device rather to the intrinsic properties).

Therefore, the quantum efficiency can be described as

$$\eta = (1 - \Re)\zeta[1 - \exp(-\alpha d)], \tag{2.3}$$

where $\Re$ is the optical power reflection coefficient at the surface, ζ — the fraction of electron-hole pairs that contribute successfully to the detector current, α — the optical absorption coefficient of the material, d — the photodetector depth. The first component $(1 - \Re)$ corresponds to the effect of reflection at the surface of the device and can be diminished with antireflection coating. The fraction of electrons and holes, which contribute to the useful photocurrent, is expressed as ζ. Finally, the last constituent $[1 - \exp(-\alpha d)]$ represents the fraction of the photons absorbed into the bulk. In order to maximize this factor, the detector should have a high depth. Being a function of α, the quantum efficiency depends on the wavelength and the properties of the material used to fabricate the detector. The quantum efficiency drops to 0 at longer wavelengths $\lambda \geq \lambda_g = \frac{hc_0}{E_g}$ as the photon energy becomes insufficient to overcome the bandgap and to be absorbed. This limiting bandgap wavelength λ_g is called long-wavelength limit. For very small values of λ, η also decreases as the impinging photons are absorbed near to the surface, where electrons and holes recombine before being collected and therefore do not contribute to the photocurrent (short-wavelength limit).

– *Responsivity* relates to the detector output photocurrent per unit of input optical power at a certain wavelength. A photon flux Φ_{ph} would cause an electron flux Φ_e, therefore, this current can be described as

$$i = \eta e \Phi_e = \frac{\eta e P}{h\nu} = RP, \tag{2.4}$$

where $P = h\nu\Phi_e$ $[W]$ is an optical power at frequency ν. The propor-

tionality factor R $[A/W]$ is defines as the responsivity of the device

$$R = \frac{\eta e}{h\nu} = \eta \frac{\lambda}{1.24}. \tag{2.5}$$

– *Linearity* — optical detectors are characterized by their linear response to the light intensity. The lowest detectable light level is determined by noise, while the upper range depends on the maximum current, which can be produced by the detector without saturation. When the optical power reaches excessively large values, the detector output become irresponsive. This operation mode, called the saturation region, limits the detector dynamic range.

– *Spectral response* response characterizes the sensor response at different wavelengths. Mainly this parameter depends on the detector material.

– *Noise:* the noise in optical detectors can have an internal or external origin. The external noise is caused by environmental factors outside the system. The internal noise is generated by internal sources of noise, delimiting the lower border of the dynamic range. The main contributions are introduced by:

  - *Photon noise* is the most fundamental source of noise and given by the fluctuations in the photon arrival rate (described by Poisson statistics);
  - *Johnson noise* or *thermal noise* is generated by thermal fluctuations in conducting materials. Each electron in a semiconductor is in continuous movement, thus, producing a small current;
  - $\frac{1}{f}$ *Noise* — sometimes called "flicker noise". This is a fluctuation whose spectral density increases for lower frequencies. It occurs

in most devices and is caused by traps, often near surface interfaces. The resulting slow drifts in signal level can be removed by chopping (modulating) the incident light to bring it to a higher electrical frequency.

Moreover, if an external circuitry is used for the processing of the signal from the detector, it as well contributes to the *receiver circuit noise* caused by the various components such as resistors and transistors. Electronic noise is composed by thermal and $\frac{1}{f}$ noise. While a conventional photodiodes noise is pure shot noise, thermal, $\frac{1}{f}$ noise and sometimes additional shot noise are contributed by additional electronics.

2.3 Image Sensors Evolution: Brief Historical Overview

2.3.1 Photomultiplier tubes

Photomultiplier tube (PMT) developed in 1934 by L. Kubetsky [25, 26] became the first photodetector with single-photon resolution and it currently is still being widely exploited. In the core of its operation principle lays the photoelectric effect and the process of secondary emission. The structure of PMT is displayed in Figure 2.1. Electrons emitted from the surface of a photoemissive cathode travel towards an electrode (anode) passing through a number of secondary emitting dynodes, placed in such a way that electrons are delivered from each dynode to the neighboring in series. Emitted electrons are accelerated by the voltage applied to each dynode and generate secondary electron emission. Thus, a large current pulse is produced at the anode. For a long time since its development, PMTs had been the only exploited devices in virtue of their high gain, low noise, ultra-fast response, excellent timing performance and wide dynamic

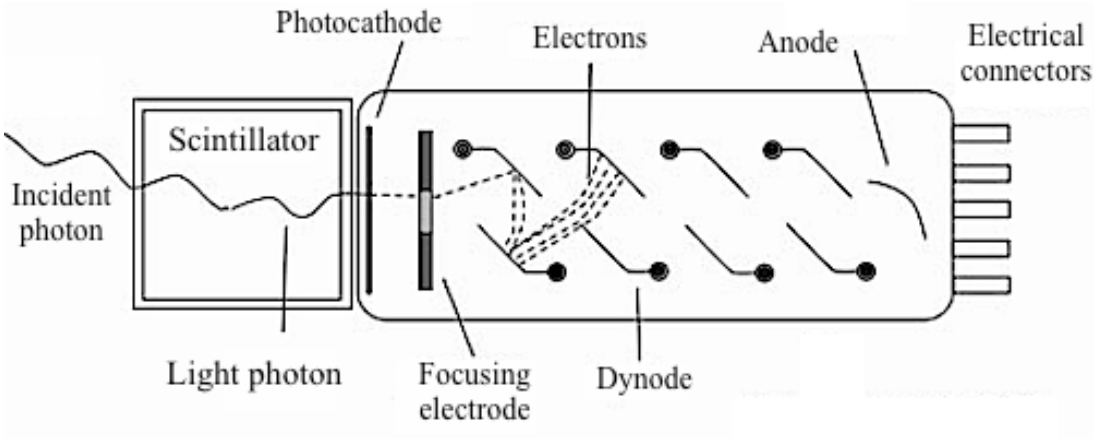

Figure 2.1: Typical structure of photomultiplier tube

range linearity. However, PMTs are costly and fragile devices, sensitive to ambient light and external magnetic field. In addition, they require high operating voltages. These disadvantages shrank PMTs exploitation.

2.3.2 Microchannel plates

Later, in 1960th, the idea of extension of PMTs into an array has lead to the design of microchannel plates (MCPs) [27, 28, 29, 30, 31], which were originally developed for image intensifiers. A microchannel plate and its single pore are depicted in Figure 2.2.

At that stage, many photon fluxes could be detected at once assuring spatial resolution. MCPs comprise small bundled electron multiplier channels made of glass with a resistive coating. Channel diameter varies from 3 to 15 μm. For the proper operation of the device a high voltage of a thousand volts is applied to the metallized surfaces of these plates. The internal surfaces of the pores are semiconducting. A weak current through each pore produces a uniform electrical field inside each channel. Therefore, a single photon hitting the channel surface releases a photoelectron. The strong electrical field accelerates the electron towards the back end of the channel. This electron will hit the channel wall and may release sec-

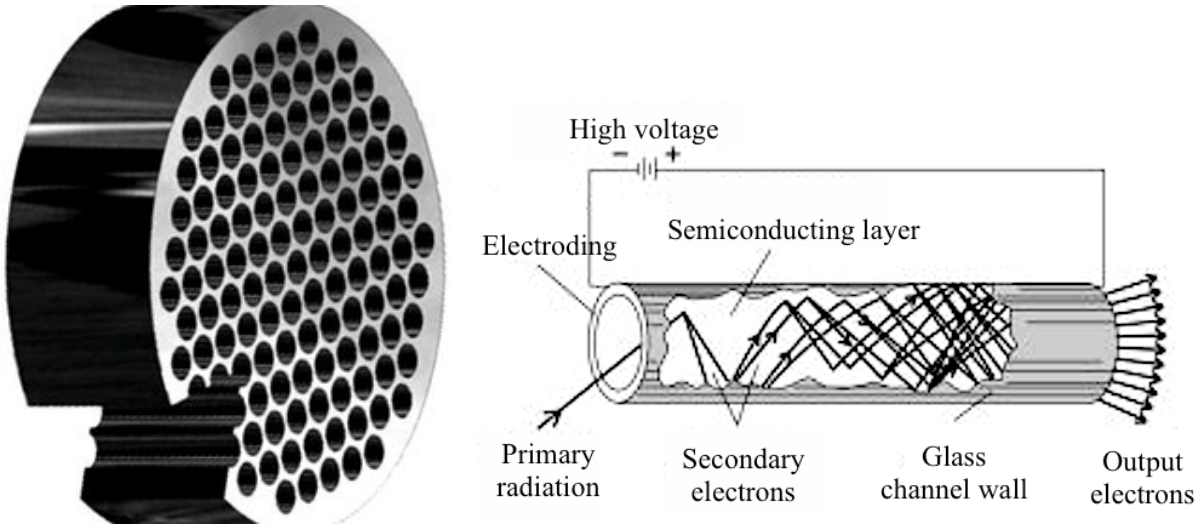

Figure 2.2: A circular microchannel plate (on the right) and its single pore (on the left)

ondary electrons. Thus an electron avalanche occurs in the microchannel and an amplified current can be collected at the output of the channel. Due to the small size of a channel and the small distance between them, a photoelectron transient time as low as 25 ps can be achieved [32, 33, 34, 35]. Similarly to PMTs, signal amplification is produced by secondary electron emission. Been built later in the 1980s, MCP-based detectors were spread to diverse fields in virtue of their high spatial resolution, high electron amplification, low dark current, high sensitivity. Nonetheless, these detectors still could not be exploited in low cost systems, as MCPs require expensive high vacuum equipment and high operation voltages power supplies. Along with the aforementioned drawbacks, a set of complexities lays into the manufacturing process: limited durability of photocathodes and channel reproducibility. Since then, many techniques varying from the different materials of the substrate to additional coating have been applied, but the detector performance was improved just partially. Not least importance has a pretty costly manufacturing process of MCPs.

2.3.3 Charge-coupled devices

A breakthrough in imaging has been done with the progress in solid-state electronics. Charge-coupled devices (CCDs) invented in 1969 [36, 37, 38, 39] provide high-quality image data and are therefore widely used in professional, medical and science applications. CCD operates as a shift register and its operating principle is shown in Figure 2.3.

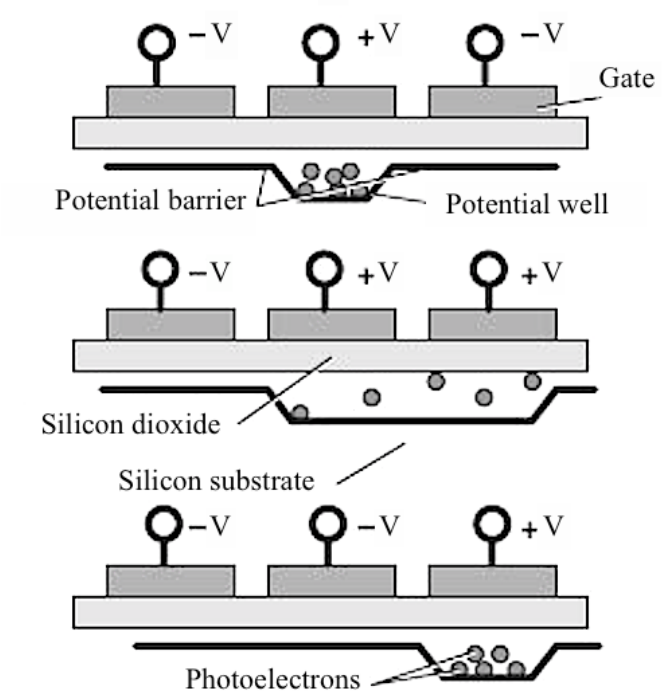

Figure 2.3: Operating principle of CCD

A CCD consists in a pixel array, where each pixel is a MOS capacitor, reversely biased and, thus, strongly inverted, and some readout circuitry, which is needed to convert the photocurrent into a voltage or an electric charge. An image is projected on the surface of the array through a lens. Impinging on the surface of semiconductor-oxide photons create proportional electric charges. Each gate pair is connected to an alternate clock line, which are pulsed in counter-phase. Triggering the gate voltages, the charge of a single pixel is transferred to its neighboring pixel. The process

is repeated until it reaches a readout circuit, which converts the total array charge into a voltage map. Distinguishing features of CCD matrix are high spatial resolution and its high quantum efficiency (above 70% for back-side illuminated devices), which can be further improved up to 90% by optical microlens array deposited on the top of the pixel array. However, the device suffers from dark current, thus an additional expensive cooling system is often required. CCDs can be fabricated only in specialized technologies, which are optimized for charge transfer implementation. Adjustability of these technologies allows pixel size scaling without significant performance deterioration. However, other camera functions cannot be integrated in the same chip.

2.3.4 CMOS Passive, active and digital pixel sensors

In the 1960s there were many research groups putting efforts on image sensor for implementation in a Complementary Metal Oxide Semiconductor (CMOS) process. The use of this technology could help to dramatically reduce the manufacturing cost. The first image sensors were the bipolar and MOS photodiode arrays developed by Westinghouse, IBM, Plessy, and Fairchild in the late 1960th. The passive-pixel sensors (PPS) was proposed first by Weckler in 1967 [40]. Nevertheless, the modern CMOS imaging systems are based on work reported in the mid 1980th. Thereby, until the early 1990th the PPS fabricated in a CMOS technology [41] became the sensor of choice. The PPS contains a photodiode and a transistor, fabricated in Bulk CMOS, which performs the function of pixel reset and row selection for the pixel readout by an external circuitry. In order to keep the bus voltage constant a charge integrating amplifier (CIA) is set at the end of each column. The structure of PPS is depicted in Figure 2.4. Figure 2.5 displays a passive-pixel based array.

PPS suffered from high fixed-pattern noise brought by active ele-

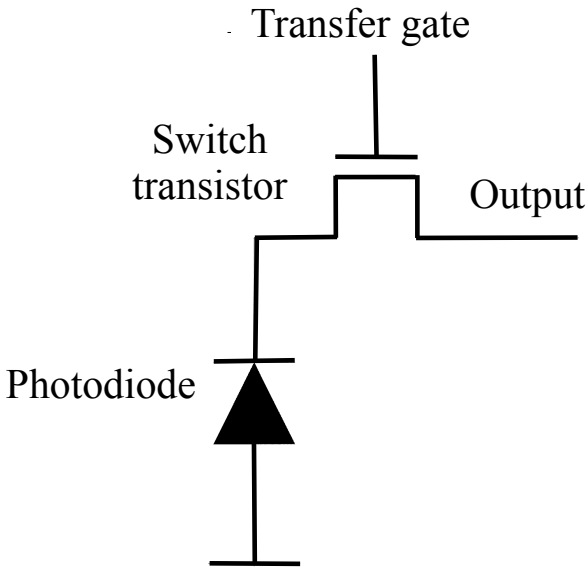

Figure 2.4: A passive pixel sensor structure

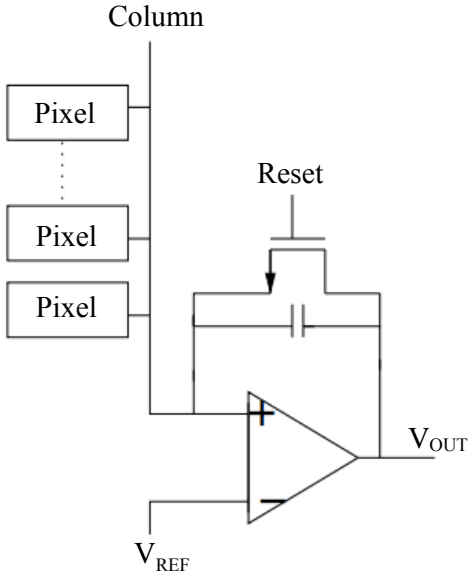

Figure 2.5: An passive-pixel based array

ments of readout, and slow readout speed as the charge of each pixel is transferred in series. Much later in 2000th, some efforts were taken to solve the high FPN issue [42, 43], but still PPS are not suitable for a large array implementation.

As CCDs do not have the drawback of temporal and fixed-pattern noise,at that time they became the base for image sensor performance. The main challenges for CCD technology and design have been set at quantum efficiency improvement, high fill factor, dark current reduction, charge transfer efficiency, low electronics readout noise, gated operation and high frame rate. A large effort was also applied to reduce the operating voltage and power supply and has led to the development of many new types of CCDs.

MOS based sensors were investigated inertly as the achieved results were unfavorable in comparison to the set criteria. Only in the early 1990th CMOS image sensors found new prospects for developers not in terms of excellent performance, but overall system low cost and chip functionality.

As a result of intensive work on CMOS imagers, the CMOS active-pixel image sensor (APS), conceived in 1968 [44], was refined in the 1990s [45]. The structure of a three-transistor active pixel sensor is presented in Figure 2.6. Figure 2.7 depicts an active pixel based array.

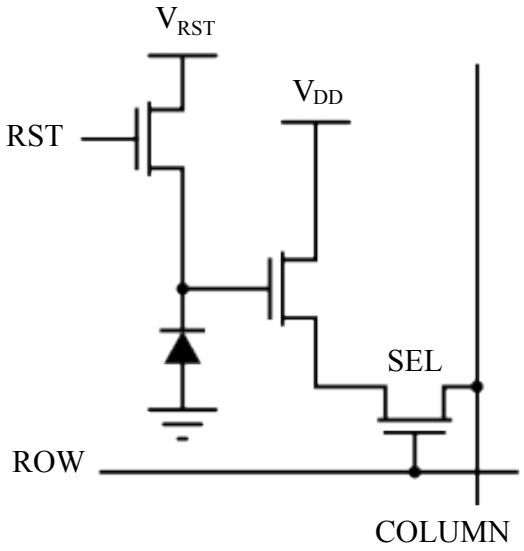

Figure 2.6: A three-transistor active pixel sensor

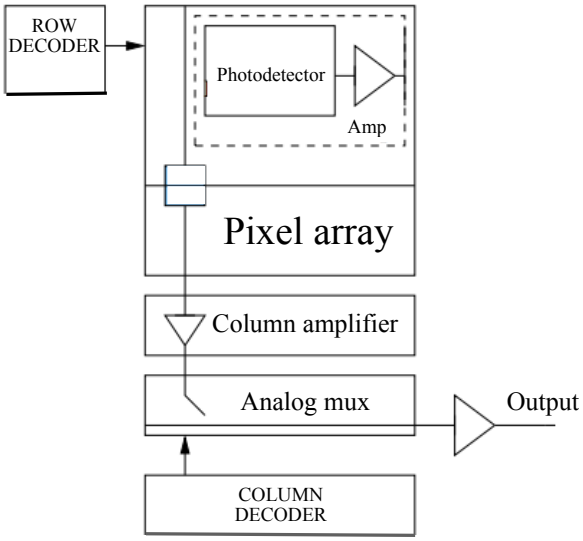

Figure 2.7: A 3-T APS based structure from [50]

Each pixel in APS array consists of a photodetector (photodiode) and an active amplifier. This new sensor solved the problem of its precursor PPS: an individual pixel amplifier serves to suppress the noise at each pixel, to buffer the signal and read out the output as voltage. Due to the advent of CMOS deep-submicron and integrated microlense technologies, the performance of APS achieved a level comparable and competitive to CCDs in image resolution, readout speed and noise, power consumption, dimensions and cost [46, 47, 48, 49, 50]. Moreover, due to the use of CMOS technology, the image processing circuitry shares the same substrate with the image sensor, while CCD requires many separated chips with different functions.

With the progress in technology scaling, digital pixel sensors (DPS)

were fabricated [51]. Its structure is depicted in Figure 2.8. An analog-to-digital converter was integrated into each pixel. The parallel conversion and digital implementation allows a high-speed readout and a wider dynamic range. There are a few examples of arrays operating at hundreds of frames per second with megapixel and more functionality in pixel [52, 53, 54]. An example of array based on DPS is shown in Figure 2.9. Fill-factor in such sensors is typically in order of 20% [55, 56, 58].

Refinement of in-pixel circuit was addressed in [57]. A test prototype of 64×64 with a shared column-parallel comparator was presented. Due to this approach and source follower placed outside the pixel, a 33% fill-factor was achieved. Moreover, the pixel power consumption is reduced by two orders of magnitude compared to a conventional 3-T pixel.

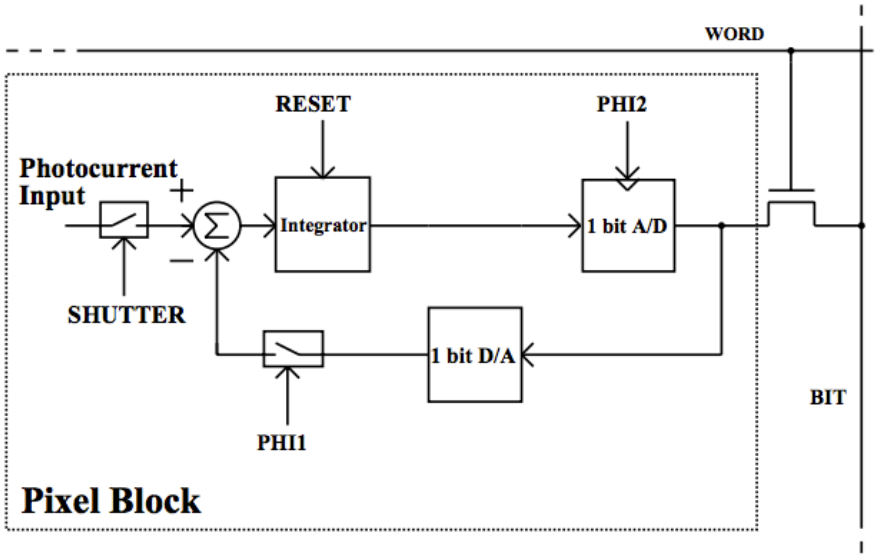

Figure 2.8: A digital active pixel sensor structure presented in [51]

Very high resolution imagers nowadays are based on 4T pixels. The feature that make them fast are on-chip ADCs, either a single one or column-level, and massive parallelization of the output signals. This breakthrough made CMOS sensors perfectly fit for very high-resolution imagers implementation with megapixel resolution and video applications.

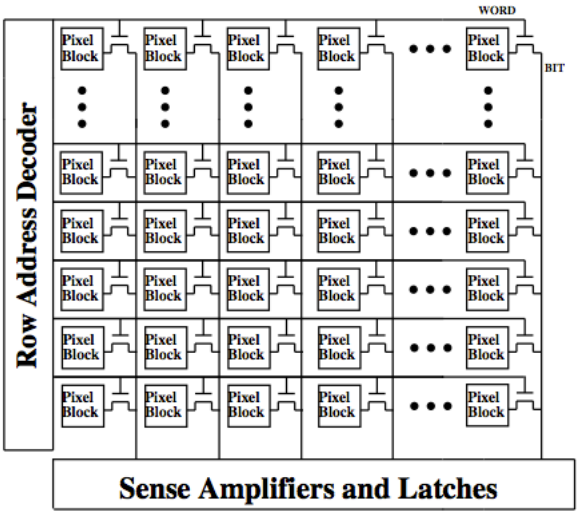

Figure 2.9: A pixel array based on DPS

2.3.5 Single-photon detectors based on superconducting nanowire

Single-photon detectors based on superconducting nanowire (SNSPDs) have been recently elaborated and this technology immediately became a very promising solution for infrared range of wavelength. In 2001 the first time the single-photon sensitivity at 790nm of a current-biased NbN superconducting nanowire was demonstrated By Gregory Gol'tsman et al. [11]. The SNSPD devices possess high efficiency, low dark counts and excellent timing resolution thus allowing their exploitation in many of applications such as quantum information science and photon-counting in the 1-1.7 μm wavelength [21]. Whereas conventional single-photon-detector technologies operate at wavelengths shorter than 1000nm, SNSPDs have a unique performance at longer infrared wavelengths. Infrared operation is desirable for quantum cryptography [13, 14, 15], optical quantum computing [16, 17], space-to-ground communications [18], characterization of emission from CMOS circuitry [19, 20] and other sources.

The operation of an SNSPD is based on a phase transition between the superconducting and resistive states in a current-biased nanowire. A

thin (less than 10nm) superconducting wire with a width of approximately 100 nm. The detection cycle is shown in Figure 2.10. Initially, this wire is cooled down well below its superconducting critical temperature. The direct current is maintained below its critical current value. A single infrared photon has energy sufficient to form a resistive barrier or a resistive hotspot across the width of nanowire (2). This electronic excitations forces the current flow over the hotspot, therefore, the local current density increases beyond its critical value (3). This leads to an increase of resistance barrier across the nanowire (4). The growth of the resistive region is also supported by heating. The current keeps flowing until the external circuits blocks it and shunts the bias current. Thus, the operation conditions and bias current are restored to the initial values and the nanowire is superconducting.

An electrical equivalent circuit of a SNSPD is presented in Figure 2.11 where L_K os the nanowire inductance, R_K - the hotspot resistance, I_{bias} - the bias current of the nanowire. The switch emulates photon absorption. The output pulse in the circuit is measured at the load resistor R_0.

A simulated output voltage pulse of the nanowire after amplification is shown in Figure 2.12. The blue and the red lines are the rising and the falling edges of the SNSPD output pulse, respectively.

Over the past decade engineering approaches and solutions to SNSPDs have significantly improved the performance of these devices. In the center of attention was the design of wire geometry with the goal to cover the desired active area. Narrower, highly uniform nanowires, optimized geometries, and improved material selection and deposition have also contributed to higher detection efficiency which has approached 90%. Recently, research group of Rosenberg [10] has presented a packaged SNSPD system that shows 68% detection efficiency at a photon flux of 100 million photons per second in the input fiber. A timing resolution of and a dark

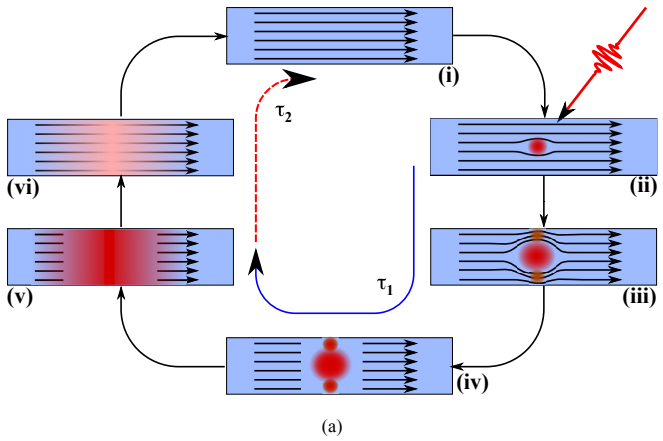

Figure 2.10: A schematic illustrating the detection cycle of single photon detector based on superconsucting nanowire [12]

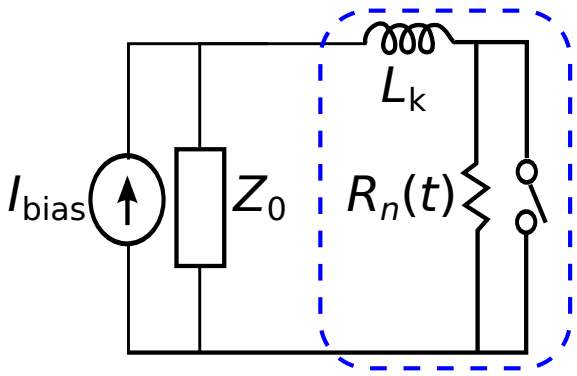

Figure 2.11: A simple electrical equivalent circuit of a SNSPD [12]

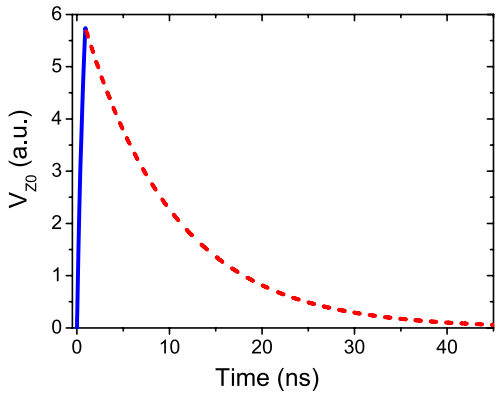

Figure 2.12: A simulation of the output voltage pulse of the SNSPD [12]

count rate of a few kcounts/s has been demonstrated.

SNSPD's design targets larger arrays, new optical coupling and packaging approaches and a high-speed readout. A drawback of the system at present is the cryogenic operating temperatures. This complicates and limits the exploitation of nanowires.

The SNSPD detectors are currently in their early stage of research. However, further development of SNSPD devices might allow their exploitation for a wider range of high-speed single-photon applications.

2.4 Single-Photon Avalanche Diodes

At present there are many photonics applications that require highly efficient and ultra-fast photodetectors. Moreover, single-photon sensitivity is an assigned priority for many applications, for instance, advanced microscopy applications (Fluorescence Lifetime Imaging Microscopy (FLIM) [59, 60, 61, 62, 63], Raman spectroscopy [68, 69, 70, 71], Positron Emission Tomography (PET) [65, 66, 67], space-to-ground communications [72], 2-D imaging [64] and 3-D ranging [73]. The devices have to also possess high timing resolution and provide a sufficient internal amplification to deliver a useful output pulse for each single detected photon.

As the photocurrent caused by single photons is too little to be discriminated, the photodetector should provide an internal gain at the absence of thermal background noise. The phenomenon of multiplication of a single photoelectron in semiconductors is named avalanche effect. In order to obtain such a regime, a photodiode operate at a reverse voltage high enough that the photo carriers break off new electron-hole pair from the material lattice. Single-photon avalanche diodes (SPADs), first designed in 1981 [78, 79], at present attract an increasing attention due to their high timing resolution, high sensitivity and shot-noise limited operation. For the first time the physical phenomena of avalanche multiplication as a result of single-photons entering p-n junction was observed in the early 1960th [80, 81, 82]. Initially the diode was not conceived as a photodetector. In comparison to PMTs, SPADs also benefit of a wider spectrum range including red and near infrared regions.

A SPAD is a photodetector, consisting in a p-n junction operating above its breakdown voltage. This regime is also called Geiger mode. A cross-section of SPAD is represented in Figure 2.13.

The reverse voltage applied to the device creates a depleted region

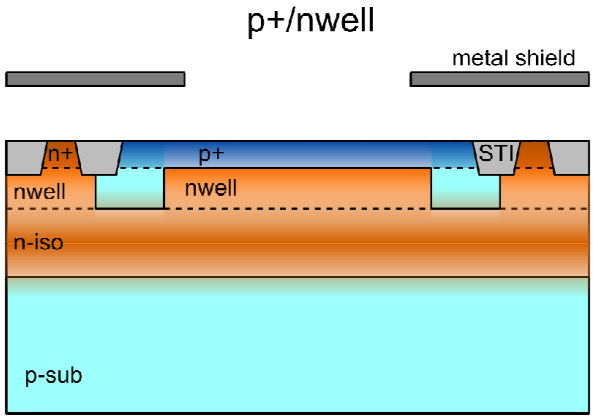

Figure 2.13: Cross-section of SPAD presented in [133]

into the bulk of the device. A single photon coming into the bulk generates and electron-hole pair. Then, these carriers are accelerated by the electric field at the junction to an extent that they gain energy sufficient to overcome the energy gap. This effect is called impact ionization and therefore an electron-hole pair may occur. These carriers accelerated by the electric field can produce another electron-hole pair. This behavior explains the carrier multiplication arising in SPAD. The current increases rapidly up to milliampere range due to the internal gain (Figure 2.14), therefore, no additional amplification is required. Thus, the time of the photon arrival can be estimated. Sometimes the avalanche might be mis-triggered by the thermal carriers and photons trapped into the bulk. These spurious ignitions are called dark counts and present the intrinsic noise of the device. It should be noted that SPAD is a binary device, thus, the current does not represent a number of photons that ignited the diode, but the ignition event. The current keeps flowing until the voltage across the device drops close to the breakdown.

The main difference from an avalanche photodiode (APD) is that APD is operated close to the breakdown voltage of semiconductor, but still slightly below this value. The applied high electric field assures an internal

multiplication gain of few hundreds, which is less than the gain of SPAD. The resulting avalanche current is linearly proportional to the intensity of optical signal. In comparison to APD, SPAD, being biased above the breakdown voltage, is able to detect each single photon. Whereas the APD is a linear amplifier for the input optical signal with limited amplification gain, for the SPAD definition of gain is meaningless.

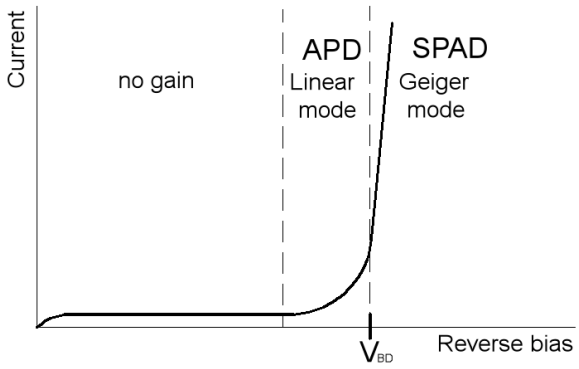

Figure 2.14: SPAD Current-voltage characteristic

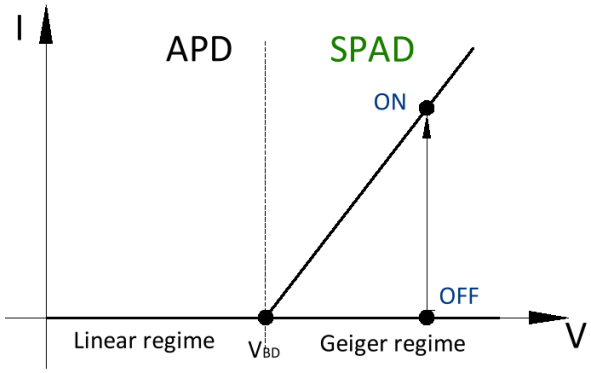

Figure 2.15: SPAD Current-voltage characteristic showing on- and off-states

The SPAD sustains the avalanche current when a photon triggers an avalanche. This event corresponds to ON state in Figure 2.15. When no carrier has been generated, no current flow is observed through the SPAD (OFF state). If the ignition event occurs while SPAD is biased above breakdown voltage, the OFF-state turns rapidly into the ON-state.

2.4.1 Key parameters for SPAD performance characterization

A complete characterization of SPAD performance should be based on the following main figures of merit:

– *Photon Detection Efficiency* (PDE) is the ratio between the number of the detected photons to the number of the incident photons. The ideal 100% PDE is unattainable in reality due to three main factors: self

reflection, absorption (discussed 2.2) and self-quenching. A common approach to minimize the reflectance from the surface is to use an antireflection coating. In order to increase the impact ionization, thus reducing the self-quenching effect, the applied bias voltage should be high enough to ensure very high electric fields.

– *Dark count rate* (DCR) — the number of avalanche ignition events contributed by tunneling effect, the thermally generated carriers and, for thickSPADs, the carriers trapped into the bulk. DCR linearly depends on the overvoltage as it increases the probability of an avalanche ignition. As the thermal generation is one of the main constituents, the increase in temperature entails an exponential increase of DCR. This effect can be reduced by exploiting a cooling system.

– *Afterpulsing probability* — the probability of a secondary avalanche ignition caused by the carriers trapped into the bulk of photodetector and then released later. The charge trapping is caused by impurities and defects of semiconductor. This factor can be minimized only with the fabrication process and technology improvement.

– *Time resolution (jitter)* the precision of the photon arrival time estimation represented either in a standard deviation of photon arrival time distribution or with the full-width half-maximum [FWHM] of photon arrival time distribution. The jitter is modeled as an Gaussian distribution that represents the timing uncertainty by the statistical nature of the impact ionization process. Time resolution reduces as the overvoltage increases.

– *Dead time* is the time needed to the detector to recover after an avalanche event. For passive quenching this time has two constituents: the time needed to quench the avalanche current and the time needed

to reset the detector to its operating conditions. For active quenching, there is an additional hold-off time that can be programmed either digitally or with a monostable circuit. During this period, the detector remains insensitive to the impinging photons. Obviously, to ensure high photon counting dynamic range, the dead time should be reduced. As previously discussed, active quenching circuits guarantee a better performance compared to passive ones. However, reduced dead time leads to an increase of afterpulsing probability.

– *Breakdown voltage* — the minimum reverse voltage value applied between the anode and the cathode of the device and sufficient to generate a diverging avalanche current.

– *Crosstalk* is a phenomenon that takes place into arrays of SPADs, when an undesired avalanche in one SPAD is caused by an avalanche of a neighboring SPAD.

2.4.2 Technology requirements for SPAD implementation

To be used as a SPAD, the structure of a p-n junction diode should meet several conditions. First of all, the exploited technology has to assure a structure free from local lattice imperfections in order to prevent a premature breakdown. In order to avoid edge breakdown, a guard ring should be formed. The intrinsic noise of the detector depends on the substrate material purity. Its value, expressed as dark count, should be low. Finally, the probability of afterpulsing should be low. At the dawn of SPAD development, the technology simply could not satisfy all fabrication requirements to the substrate quality. In the 80s, several diodes were implemented in planar-silicon technology [78, 79]. Even though CMOS processes became widely available in the 1980s, the first CMOS SPAD was demonstrated only in 2003. In 2000s the photodiode could be implemented in the same sub-

strate with an additional circuitry needed for quenching or signal processing. Moreover, design has a high degree of complexity at low dimensions and reasonably low fabrication cost. The first CMOS SPAD [96] was implemented in a high-voltage 0.8 μm CMOS technology. This device showed a 50ps timing resolution and was favor- ably compared with commercially available PMT. This SPAD was the forerunner of array assembling. This finding opened the way to the development of compact and cost-effective large SPAD based imagers that could be potentially competitive with CCD cameras.

At the present time, silicon remains the main semiconductor suitable for SPAD fabrication due to its advanced technology. Currently there are three main processes used for SPAD implementation:

- *Standard CMOS process* is a CMOS process with no modifications. The process does not completely correspond to the all technological requirements imposed by SPAD fabrication. As consequence, a high DCR and low PDE are typically obtained with standard process. However, the main advantage of the process is its accessibility at low cost for prototyping.

- *High voltage CMOS process*: Not only single detectors, but also integrated arrays containing an additional circuitry have been presented. HV process provides high voltage devices from 20 V to 120V for the absolute maximum rating voltage. Such devices may have different structures and dopant concentration in order to provide particular capabilities for operating at particular voltages. However, the junctions between low voltage and high voltage CMOS technologies shrinks the scope for large integration.

- *Fully customized CMOS compatible process* targets to obtain the best SPAD performance [97] in terms of dark count rate and crosstalk. The

technology is suitable for implementation of small arrays only [98, 99], but on-chip circuitry large-scale integration is limited.

Recently, a new generation of CMOS process has been developed which became a new stage in image sensor technology. Scientific CMOS (sCMOS) technology has overcome the drawback of conventional CMOS in imaging applications. Thus, sCMOS based cameras achieved extremely low noise, fast frame rates, wide dynamic range, high resolution and quantum efficiency. These sensors show a peak quantum efficiency above 55% without deterioration neither spatial nor temporal resolution. sCMOS image cameras recently presented by PCO-TECH Inc. [100, 101] have promising performance for low-light conditions, but precise localization is still unattainable for this technology when it comes to single-photon detection [102, 103].

Currently, InGaAs/InP SPADs are also being investigated due to the material properties [104, 105, 106, 107]. These devices benefit of high photo detection efficiency within the wide spectral range (from 900nm up to 1600 nm). Their main drawbacks are a high dark count rate and a high afterpulsing probability requiring a long dead time up to a several microseconds. Nonetheless, recently a few InGaAs SPAD based modules have become commercially available: "CountQ" by LaserComponents [108] and "InGaAs SPAD" by Micro Photon Devices [109]. "InGaAs SPAD" achieved a remarkable PDE up to 40% and state-of-the-art timing resolution of 150 ps. Along with that, gate width can be adjusted from 0.2 to 10 ns, gate repetition frequency can reach values up to 133 MHz. However, the dark count of this device is high in order of 10-40 kcps. Module "CountQ" shows PDE of maximum 10%, instead, the detector achieved a dark count rate of only 1kcps, only 1% of afterpulsing probability and requires low operating voltages (12 V). Both devices are thermoelectrically cooled down. The future progress in InGaAs/InP SPADs completely

depends on front-end circuit design and the device fabrication technology.

2.4.3 Quenching circuits

In order to restore the photodetector to its operating condition, to bias the voltage down below the breakdown value, and prevent the avalanche destroying the diode, an additional quenching circuit is needed. Several different active and passive quenching circuits have already been proposed in the literature [83, 85, 86, 87, 88, 89]. An example of passive quenching circuit (PQC) is depicted in Figure 2.16 and consists of a ballast resistor connected in series.The value of the ballast resistor is typically in order of a few hundred $k\Omega$. When an avalanche occurs, the current rises to its peak value which corresponds to the ratio between the excess bias voltage V_{ex} and the SPAD's series resistance R_S. This current, therefore, discharges the parasitic capacitance C_P of the cathode of SPAD at a constant time τ that can be expressed as:

$$\tau = C_P(R_S \| R_B) \tag{2.6}$$

The diode becomes conductive and the voltage over it drops to V_B, therefore, the current flows though the diode and the load. The current final value is the excess bias voltage over the ballast resistance:

$$I_F \simeq \frac{V_{ex}}{R_B}. \tag{2.7}$$

This value defines whether the avalanche is self-sustaining or self-quenching. If I_F is large enough, there are enough carriers present in the space charge region and the avalanche current maintains flowing. On the other hand, if the value of I_F is small enough, avalanche multiplication can stop since there are no more carriers in the space charge region. That is, the avalanche is self-quenched. Practically, I_F tends to be approximately 100

μA, named "quenching threshold". Figure 2.17 displays cathode voltage (a) and diode current (b) over the SPAD during its ignition. The voltage across the diode drops down below the breakdown in a few nanoseconds. The quenching time can be calculated as

$$t_Q = \tau ln\Big(\frac{I_0 - I_F}{I_S - I_F}\Big), \tag{2.8}$$

where $I_0 = \dfrac{V_{ex}}{R_S}$ is the maximum value of the avalanche current corresponding to the beginning of the ignition and I_S is the quenching threshold.

The parasitic capacitance of the connection between the SPAD and an external ballast resistor is typically large. That fact does affect the quenching time of SPAD which typically is around 150 ns [84, 122]. However, ballast resistor integrated directly with SPADs can significantly lower the value of C_P by a factor of 10. Therefore, the quenching time in this case is also 15 ns, which is 10 time smaller in comparison to the external resistance.

Circuit simplicity and compactness are the main features of PQC. Since PQC occupies much smaller area by comparison with the detector itself, fabrication of large SPAD arrays becomes feasible. By reason of undesirable afterpulsing effect, which may occur due to the carriers trapped into the trapping centers and then released after a random time, an additional hold-off time should be kept. This time should be sufficient so that all the carriers can be released from the trapping center without causing a spurious avalanche. PQC are not able to provide this time and an additional circuitry must be designed. Additionally, SPAD may create a current avalanche before its complete recharge to the initial operating conditions, thus causing distortion in the timing response. That means that afterpulsing effect can be an issue even with a low repetition rate.

To solve this issue, active quenching circuits (AQC) based on an

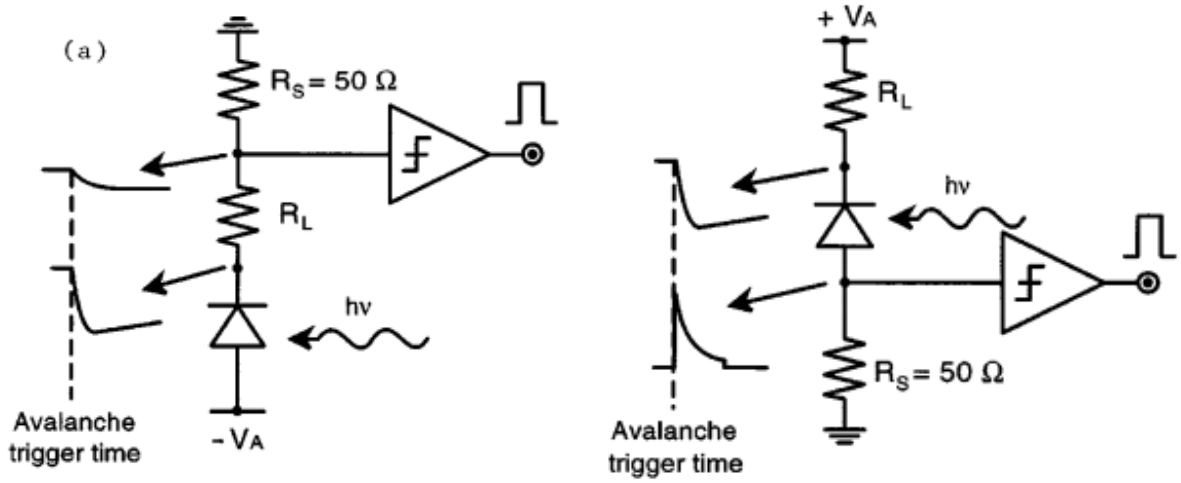

Figure 2.16: Basic quenching circuits with current output (on the left) and voltage output (on the right) [88]

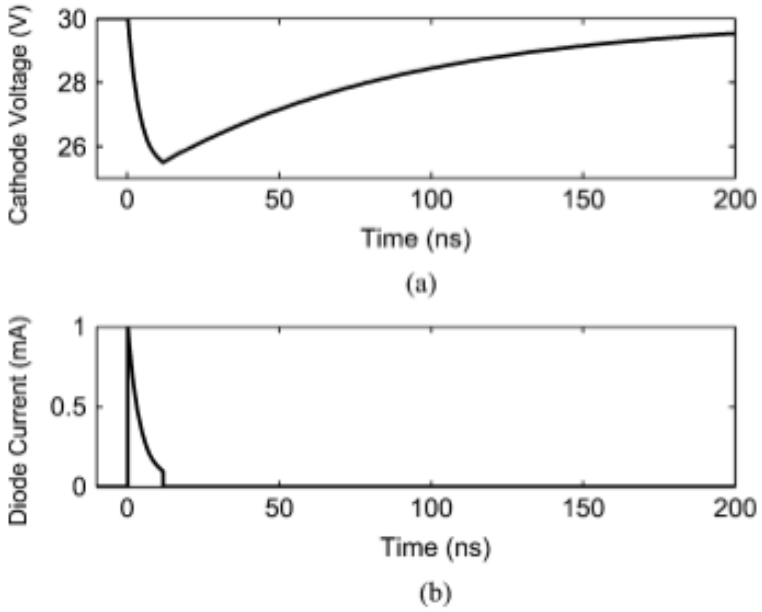

Figure 2.17: Cathode voltage (a) and diode current waveforms (b) for a SPAD connected to passive quenching circuit [88]

electronic circuit were developed by S.Cova and co-workers [83, 85, 87, 90, 88]. The key idea of the design was to shorten the time needed for quenching and diode reset by using a feedback circuit. An example of

AQC is presented in Figure 2.18. Avalanche is detected by a comparator whose output brings the bias voltage below the breakdown value. In the reported implementation, the quenching circuit reduced the excess bias voltage of the photodiode below its breakdown value for 20-50 ns. This hold-off time can be precisely adjusted by the bias voltage control. Then, the circuit restores the voltage over the SPAD to its initial state within a few ns and the device is ready to detect a new photon. The voltage on the cathode (a) and the current waveform (b) of SPAD quenched by means of active circuit are depicted in Figure 2.19. Quenching circuit exploitation allows for quenching times in order of a few nanoseconds.

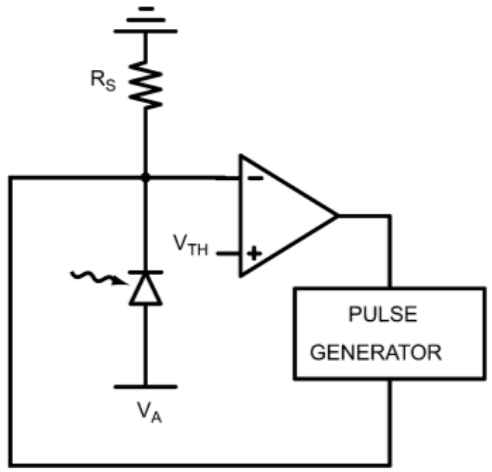

Figure 2.18: A basic active quenching circuit [88]

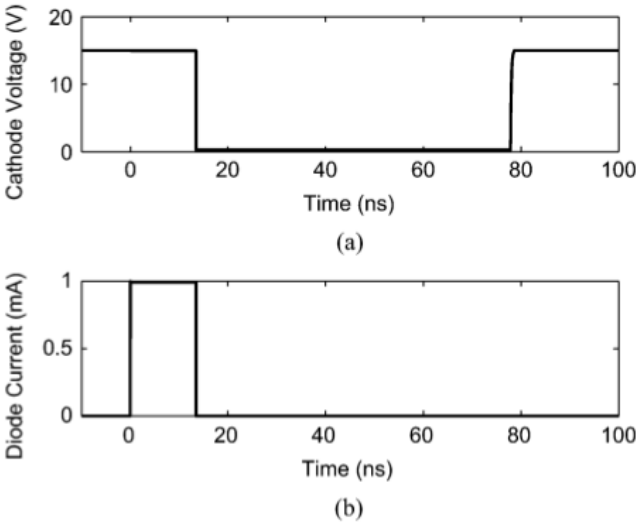

Figure 2.19: Cathode voltage (a) and diode current waveforms (b) for a SPAD connected to active quenching circuit [88]

AQC assures the best exploitation of the physical limits of SPAD. AQC assures much faster reset of the photodetector and a adjustable hold-off time. However, the circuit design is more complex, its implementation requires much larger area on the substrate and also higher power consumption [91]. In other words, AQC is not very suitable for applications foe which high fill factor is a key requirement.

Attempts to reduce the circuit area and combine the advantages of both approaches led to the design of mixed passive-active and active-passive quenching circuits [88, 92, 93, 94, 95]. Most mixed circuits are implemented with active reset. An example of mixed active-passive quenching circuit is represented in Figure 2.20.

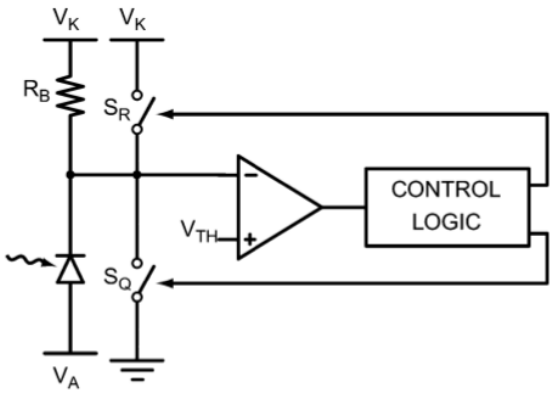

Figure 2.20: A mixed active-passive quenching circuit [88]

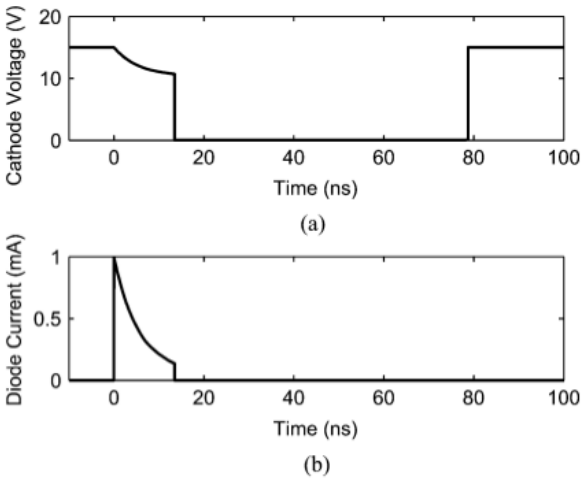

Figure 2.21: Cathode voltage (a) and diode current waveforms (b) for a SPAD connected to mixed active-passive quenching circuit [88]

The first stage of the quenching is passive as the avalanche current flow over the ballast resistor and the process is identical to PQC operation. Then, the active circuitry senses the rising edge of avalanche, holds SPAD off and restores it to the bias voltage. Therefore, at this point the circuit operation corresponds to AQC. Cathode voltage and current diagrams of the circuit are represented in Figure 2.21.

The proposed passive-active circuit approach benefits low afterpulsing probability and shorter hold-off time. The circuit is not very compact, hence, it could not be suitable for a high-resolution array implementation.

2.5 SPAD Arrays

2.5.1 Figures of merit

There are several parameters used for characterization of the overall SPAD array performance. Among the key parameters are photon detection efficiency, pixel pitch and pixel fill factor.

– The resolution and performance of image sensors can be characterized by the *modulation transfer function (MTF)* from the subject to the image. In other words, this function reflects the ability to transfer contrast and reproduce details from the object to the image produced by the imager.

  MFT depends on:

  - *Fill factor*(FF) reflects the ratio of the active pixel, sensitive to the impinging light, to the total pixel area. Generally, FF is limited by a SPAD guard ring and by the additional in-pixel circuitry. The MTF is depressed as the fill factor decreases. Low light and low contrast conditions require detectors with large sensitive area as fewer photons arrive at the detector.
  - *Pixel Pitch* (PP) is the distance between the centers of neighboring pixels. Larger PP, higher the spatial resolution of the detector.

– *Non-uniformity* of sensor is affected by:

  - *Temporal noise* — the noise resulting from photodetector shot noise, pixel reset and readout circuit noise. This noise contribution is different from one frame to another.
  - *Fixed Pattern Noise* (FPN) is the pixel-to-pixel output variation in the same light conditions due to device, dark current and internal interconnection mismatches. This variation includes offset

FPN, which is constant and independent on pixel signal, and gain FPN, a.k.a. photo response non-uniformity (PRNU).

In SPAD arrays, both temporal noise and FPN are entirely due to SPADs. In conventional image sensors, the readout circuit is the major contributor of noise at low light levels.

2.5.2 Array assembling and pixel design

The first implementation of a 32x32 pixels SPAD array was performed in 2005 [110]. Each pixel of the matrix consists of an independent SPAD, quenching, inverter and column-access circuitry. Time-resolved measurements were performed off-chip. The architecture of Random Access Readout is simple, but it is highly inefficient and only low frame rates can be achieved. The device presented has a major disadvantage: only one pixel at a time can be connected to the external read-out, so that the output of the other pixels is lost.

The integration of column readout circuits solving this problem was later proposed in [111, 112, 113, 114]. Event-driven architectures proposed in [111, 112, 113] allowed non-sequential row-wise and simultaneous column-wise detection. Therefore, no data on the photon arrival time gets lost. Using this approach, the output of all pixels in the same column are processed simultaneously. The column operates similarly to a digital bus consisting of a high-speed line with N addresses corresponding to the number of pixels in the column. When a SPAD ignition event is detected, the generated pulse is transferred to the bottom of the line. Calculated photon-detection time carries the information of the place of the pixel that was ignited as the pulse is well-defined in correspondence with the location in the pipeline [115, 116, 117]. Data processing can be performed outside the pixel array. However, the architecture has a long dead-time

The main problem of readout channels placed outside of the pixel is the parasitic capacitance of bus sharing and interconnections to an external circuitry. This fact significantly increases the total parasitic capacitance, thus, limiting the array scalability.

Another approach is in-pixel readout which implies that the circuit for quenching and preliminary processing is placed in the same pixel with the SPAD. The pixels can be read out in parallel thus processing is done simultaneously and less time-consuming. Moreover, this approach allows low power consumption as no continuous readout is required. The circuit is enabled for a short time of photon arrival. The complexity of the implementation is dependent on the functions performed at the pixel level. However, there are some design challenges for in-pixel Fully Parallel Processing architecture. First of all, circuit area is limited to a few hundreds of μm^2 in order to obtain a reasonable pixel fill-factor and pitch. Power consumption per pixel should be low to large allow array size. To provide high image quality, the circuit should assure a low non-uniformity among the pixels' time resolution without any additional calibration.

Since the first CMOS SPAD was designed, several image sensors with in-pixel architecture based on CMOS technology have been presented [64, 118, 119, 120]. Each pixel contains additional circuitry that provides quenching of SPAD, data storage and preliminary processing. Even though these devices present remarkable timing resolution, a small fill-factor of only a few percent could be achieved on account of the area occupation of guard-ring and readout circuitry. The summary of the characteristics achieved in the latest SPAD arrays is presented in Table 2.1

Currently, SPAD arrays perform the fastest measurements (300 kfps) and have shown the best precision (10%) compared to CCD and sCMOS cameras [121]. They would be ideal detectors due to their single-photon sensitivity and shot-noise limited operation. Nonetheless, their restricted

Research group	CMOS Technology	Pixel size	Fill Factor	PDP (max)	Readout
Guerrieri [64]	0.35 μm HV	100μm	3.14%	43%	Digital Counter
Niclass [111]	0.35 μm HV	25 μm	6%	35.4%	Time-to-Digital Converter
Walker [119]	0.13 μm	45 μm	3.17%	5%	Digital Phase-Domain $\Delta\Sigma$
Veerappan [120]	0.13 μm	50 μm	1%	27.5%	Time-to-Digital Converter
Pancheri [143]	0.35 μm HV	25 μm	20.8%	31%	Analog gated counter
Maruyama [6]	0.35 μm HV	25 μm	4.5%	20%	Gating+1bit digital memory
Gesrbach [124]	0.13 μm	32μm	2%	25%	Time-to-Digital Converter

Table 2.1: SPAD arrays characteristics

quantum efficiency below 35% and fill factor of 2-4% still significantly limits the range of possible applications. Several research efforts have been directed towards technology scaling, in order to reduce pixel size, increase resolution and integrate more functionality at the pixel level. Single SPADs were implemented in deep-submicron CMOS technologies and presented in [128, 129, 130, 131, 132, 133]. A few SPAD arrays were fabricated in 0.13 μm CMOS technology [122, 123, 124, 125, 126]. Despite the benefits of the advanced technologies in terms of design compactness, the fabrication of SPADs with good output characteristics is not a trivial task. A few challenges in deep-submicron technology have to be faced to produce low-noise SPADs [127]. First of all, the interface between Shallow Trench Isolation (STI) oxide and silicon includes a high density of generation centers [128]. Second, in order to prevent punch through between the source and drain of the transistor, a large doping concentration is used in the well regions. As it was shown in [123], a large doping brings to a large dark count rate due to carrier tunneling. Recently, good results were achieved in the implementation of SPAD in 0.18 μm High Voltage CMOS technolo-

gies [129]. In addition, low-noise SPADs were recently demonstrated in 0.13 μm CIS process [132]. The area occupied by the guard ring was decreased. Two different SPAD structures for 0.15 μm technology were fabricated and characterized [133] offering a good dark count rate and timing resolution. Although they are still not optimized in every respect, these devices can be employed for the realization of single-photon image sensor prototypes.

A challenge to the spatial resolution and array scaling is the SPAD size attainable without deterioration of the device performance. In [134, 135, 136] SPADs with different diameters of active area (from 100 μm down to 2 μm) were compared in terms of DCR and timing performance. The median DCR increases more than linearly with the SPAD area. In [135] it was observed that the breakdown voltage is lower for SPADs with a larger area. Regarding time resolution, the smaller detectors have a lower jitter due to a lower lateral avalanche spreading time. The main problem for pixel size scaling is found in DCR. Smaller the pixel, higher DCR. So, for instance, for a SPAD active area of 8 μm the smallest feasible DCR is expected to be about 100Hz [137, 138, 130, 139]. The SPAD reported in [135] a SPAD, having a 4-μm active area diameter, achieved a DCR lower than 30 Hz. For a device with an active area of 2 μm the DCR reaches hundreds of kilohertz [128]. However, the high DCR could be explained with the lack of a real guard ring. The future progress in the SPAD detector miniaturization fully depends on the semiconductor process innovation.

Different geometric shapes of SPADs have also been explored. Currently most of the SPADs have been designed with a circular shape that ensures the absence of electric field peaks in the device periphery. Although there are a few works [137, 140] that employed octagonal and square geometries, no direct comparison with circular design was carried out. Only the work in [135] reports a comparison among photodetectors having circular, square and square with rounded edges geometries. The results in [135]

show that DCR is lower for the circular shaped devices. The fill factor can also be improved by using microlens arrays, offering a way to enhance light collimation and collection efficiency [141, 142]. In [141] a SPAD array with microlens array concentrator was presented. Exploiting this approach the photon detection efficiency can be enhanced by factor of 35, thus, significantly recovering a fill factor. Also microlens arrays are promising for large array. However, even though the proposed technique enables acquisition of photons outside active area, it is also sensitive to noise generated in the guard ring region. Thus, a technique to improve signal-to-noise ratio should be considered.

2.5.3 Read-out circuitry for in-pixel implementation

In addition to the aforementioned activities on SPAD scaling, research is also being done on smart readout circuitry able to deal with the large amount of data generated by SPAD arrays. As presented in Table 2.1, in most of the SPAD pixels presented so far, the active area is only a few percent of the total pixel area. The advantages offered by single-photon sensitivity are therefore spoiled by the low pixel fill factor. Since a digital readout channel typically consists of a few hundreds of transistors and is thus area consuming, a solution to overcome this problem could be found in replacement of digital counter and active quenching by analog circuit. This approach allows reduction of the number of in-pixel transistors without loss of functionality. A few recent research works have proposed to implement compact analog readout circuits to improve the fill factor [143, 144, 145, 146]. A carefully designed analog scheme can achieve the same count accuracy with lower number of transistors than a digital implementation.

Researchers at Fondazione Bruno Kessler (FBK) [143, 144] presented an in-pixel analog circuit for time-resolved image sensing. The circuit

consists of only 12 NMOS transistors and includes a passive quenching transistor, a gating circuit and an analog counter (Figure 2.22).

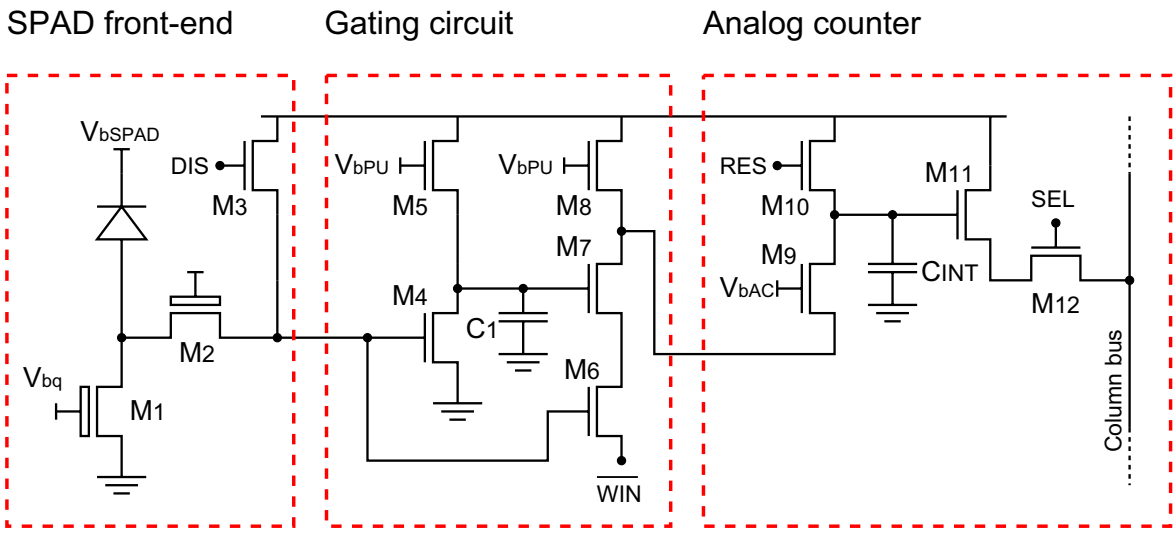

Figure 2.22: Circuit schematic of the analog counter presented in [143, 144]

A 32x32 pixel array was manufactured in a 0.35 μm high voltage CMOS technology. A pixel pitch of 25 μm was achieved with a remarkable fill factor of 20.8% and 1.1ns minimum gate width. The state-of-the-art fill factor was obtained not only due to the circuit compactness, but also to the SPAD rectangular shape. One of the problems of this circuit lies in the large current consumption of the NMOS-load inverter circuit, which makes it difficult to realize larger SPAD arrays. Another shortcoming of this design is related to its non-uniformity, which is affected not only by threshold voltage mismatches of the resistive switch, but also by the shortened pulse width non-uniformity.

Researchers from the University of Oxford proposed an analog counter suitable for manufacturing in a 0.18 μm UMC process [145]. The schematic of the circuit is displayed in Fugire 2.23. Each pixel of the proposed circuit contains a quenching circuit, an inverter, a counter and a source follower. Also in this implementation, the operation relies on a MOS switch dis-

charging a storage element, a capacitor, by a constant voltage value at each avalanche. Thus, the circuit output voltage is proportional to the number of SPAD pulses. The key idea of the design was to place the additional circuitry in the free area between the circular SPADs. At the chosen pixel pitch of 30 μm and 10 μm SPAD active area, an area of only 12x12 μm^2 was available for the design. The capacitor is a Metal-insulator-Metal capacitor and is formed into the upper metal layers (Figure 2.24).

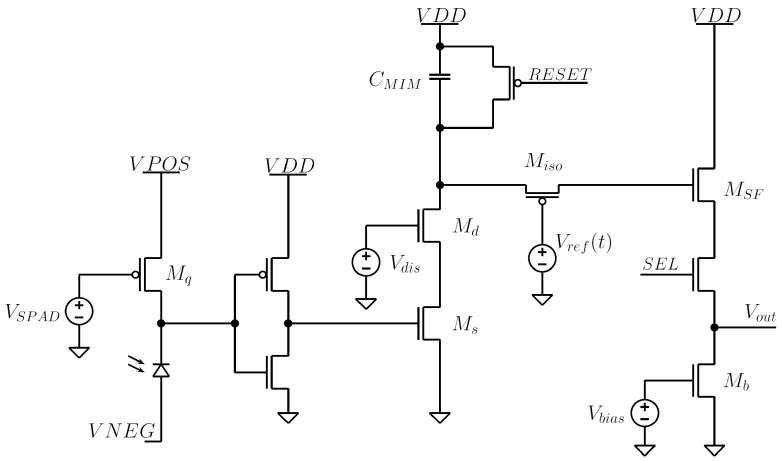

Figure 2.23: Schematic and the design proposed in [145]

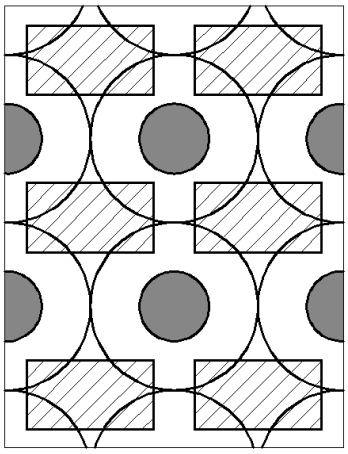

Figure 2.24: The area between the SPADs available for the circuit design

This approach allows using the inactive pixel area to create a reasonably large capacitance (400 fF), thus, increasing the circuit dynamic range. With this implementation, however, only 14 photons could be counted at the threshold voltage needed for MOS switch operation. Moreover, the proposed circuit is not suitable to be used in time-resolved detection applications.

Recently, an analog readout circuit based on 11 NMOS transistors was proposed by researchers from the University of Edinburgh [146]. The circuits schematic is shown in Figure 2.25. A 0.13 μm CMOS imaging technology was chosen for fabrication of a 3x3 pixel array. Each pixel if the

array comprises a SPAD with an active area of 2 μm, a quenching circuit, a time gating, a charge transfer amplifier (CTA) and a standard source follower. Due to the technology scaling a state-of-the-art 9.8 μm pixel pitch with a fill factor of 3% was demonstrated. An advantage of the design is the output programmability (from 13.1mV/event to 0.15mV/event) allowing the accumulation of up to 1000 events by the analog counter. The readout also benefits of a relatively low PRNU of 2% for the range 5.5mV to 13.1 mV per event. However, the characterization of the time-gated operation is not reported.

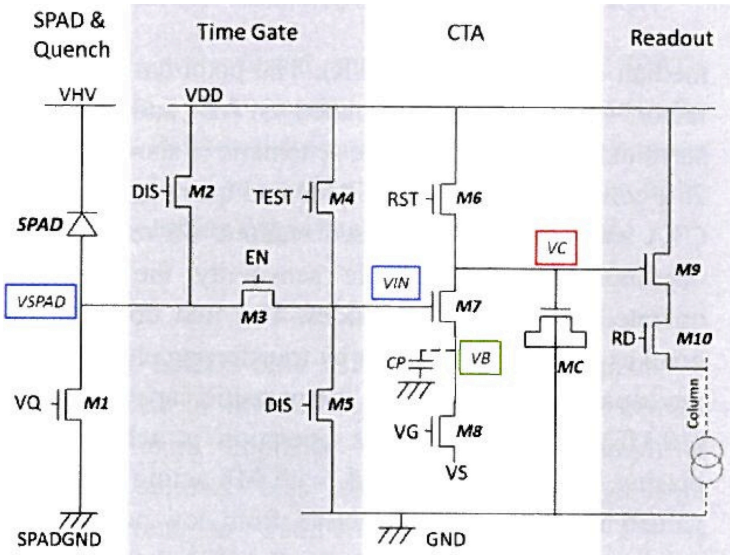

Figure 2.25: Circuit schematic of the analog readout presented in [146]

Chapter 3

Analog Readout Circuits for Single-Photon Pixels

In this section, the design and simulation of four different analog counting circuits are presented. Consisting of only a few transistors, the proposed circuits can be integrated into compact SPAD-based pixels benefiting from a larger fill factor and smaller pixel pitch with respect to a standard digital counting readout. The circuits have been designed in CAD Cadence to be implemented in a standard CMOS technology. The key design guidelines were sub-nanosecond timing resolution, low power consumption and a good uniformity between the pixels in a small area. The main challenges for the circuit design are listed hereafter:

- Compactness — in order to improve pixel fill factor and reduce pixel pitch
- Low power consumption is the key factor for large pixel array assembling;
- Sub-nanosecond gating allows observing fast optical signals;
- Uniformity of pixel response;
- Linearity of the output;

– Good dynamic range — to achieve at least 100-200 counts within one acquisition.

3.1 Circuit I. Analog Readout Circuit Based on Charge Sharing

The circuit described in this paragraph was designed in SOI, FBK, before the starting of my PhD term, and fabricated in a 0.35 μm technology. In the first part of my PhD work, I have been in charge of the experimental characterization of the circuit reported here. Besides that, I carried out additional circuit simulations to ease the interpretation of experimental results. The readout circuit of the counter is based on the charge transfer concept. Its schematic is shown in Figure 3.1.

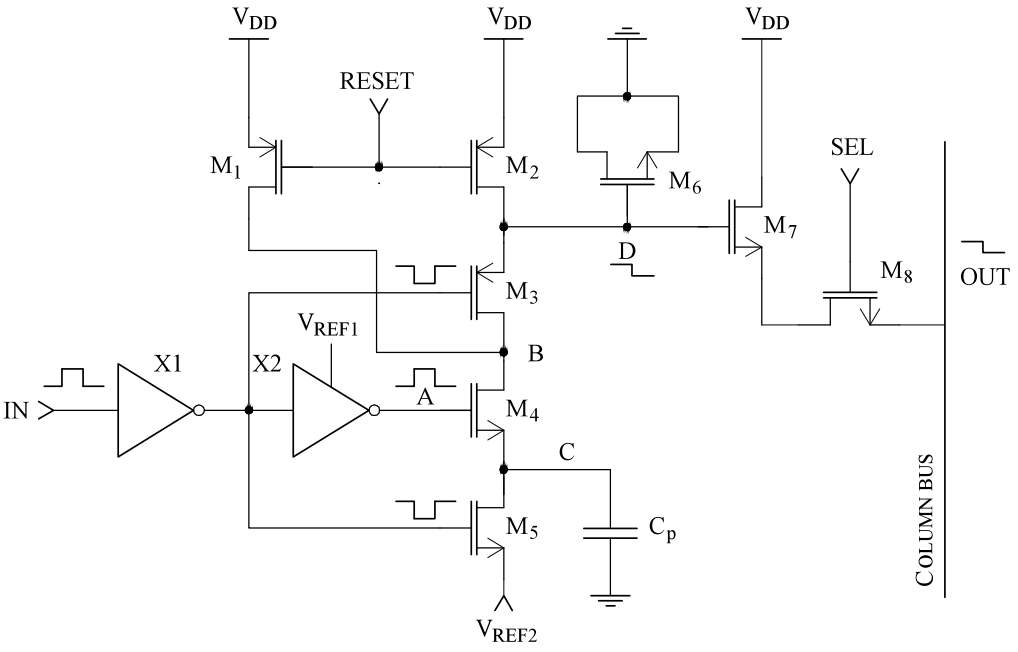

Figure 3.1: Analog counter circuit based on charge-transfer principle

Table 3.1 contains dimensions of the MOS transistors in Circuit I.

Figure 3.2 presents the timing diagram of the most meaningful signals at nodes. The circuit does not contain either SPAD or quenching circuit.

For the test purpose an externally applied digital signal IN was used with a pulse width corresponding to the SPAD ignition event. The

Transistor Name	W/L, μm	Transistor Name	W/L, μm
M_1	0.7/0.35	M_5	0.7/0.35
M_2	0.7/1.0	C_{M6}	22.5/5.0
M_3	0.4/0.35	M_7	0.8/0.35
M_4	0.7/2.8	M_8	2.0/0.35

Table 3.1: Dimensions of the MOS transistors in Circuit I

duration of the SPAD output pulse is usually in the range from a few tens to a few hundreds of nanoseconds. The inverter $X1$ has to buffer the signal, isolating the SPAD from the rest of the circuitry. Initially, during the RESET phase, the MOS capacitance C_{M6} and node B are pre-charged to V_{DD} through transistor M_2 and M_1 respectively. When no photon is detected (IN=Low), the high level of $X1$ output keeps transistor M_5 in its ON state. Thus, node C and parasitic capacitance C_P are charged to the reference voltage V_{REF2}, which is typically close to ground. In order to prevent a direct current path during input transients between node D and V_{REF2}, charge transfer is controlled by two complementary transistors M_3 and M_4 driven by slightly delayed signals. Transistor M_1 is used to preset node B to the reset voltage V_{DD}, properly defining the initial state of the circuit. When a photon is detected (IN=High), transistors M_3 and M_5, both driven by $X1$, are forced to switch on and off respectively, while the voltage at the gate of transistor M_4 (node A) changes from ground to a reference voltage V_{REF1}, supplied by the inverter $X2$. This voltage change, being $V_{REF1} > V_{REF2}$, causes a proportional positive voltage change at node C equal to $(V_{REF1} - V_{REF2} - V_{THM4})$ which, consequently, generates a charge transfer ΔQ through M_4 and towards node C equal to

$$\Delta Q = (V_{REF1} - V_{REF2} - V_{THM4}) \cdot C_P, \tag{3.1}$$

where V_{THM_4} is the threshold voltage of transistor M_4. This charge passes

through transistor M_4 towards node C and then is sequentially extracted from capacitor M_6 at each counted by SPAD photon. The discharge of the MOS capacitor M_6 creates a proportional voltage step ΔV_D at the output of the circuit (node D) equal to

$$\Delta V_D \approx (V_{REF1} - V_{REF2} - V_{THM4}) \cdot \frac{C_P}{C_{M6}}. \tag{3.2}$$

Equation 3.2 asserts that the output voltage step ΔV_D is defined by the capacitance ratio $\frac{C_P}{C_{M6}}$, set to be $\ll$1, and by the voltage difference $V_{REF1} - V_{REF2}$, fixed externally, which allows to program the charge packet transfer and thus the resolution of the counter.

During the falling edge of IN (corresponding to the end of the SPAD dead time) transistor M_3 is switched off, sampling the node D, while M_5 turns on, pre-charging again node C to V_{REF2}. In this condition, the circuit is ready to generate a new voltage step at the next incoming pulse. During this transition, the counterbalance of charge at output node is dominated by clock feedthrough and charge injection from M_3, causing a positive voltage step. This effect, confirmed by simulation and experimental results, is represented in Figure 3.2. In order to minimize this effect, a minimum size transistor M3 was used while the output capacitance C_{M6} was designed as large as possible. The cycle is repeated several times, leading to a multistep decrease of signal at node D, as it can be seen from Figure 3.2. At the end of the integration time, the output signal is read out. To this purpose, transistors M_7 and M_8 play the role of source follower and select switch, respectively, like in standard three-transistor active pixel implementations.

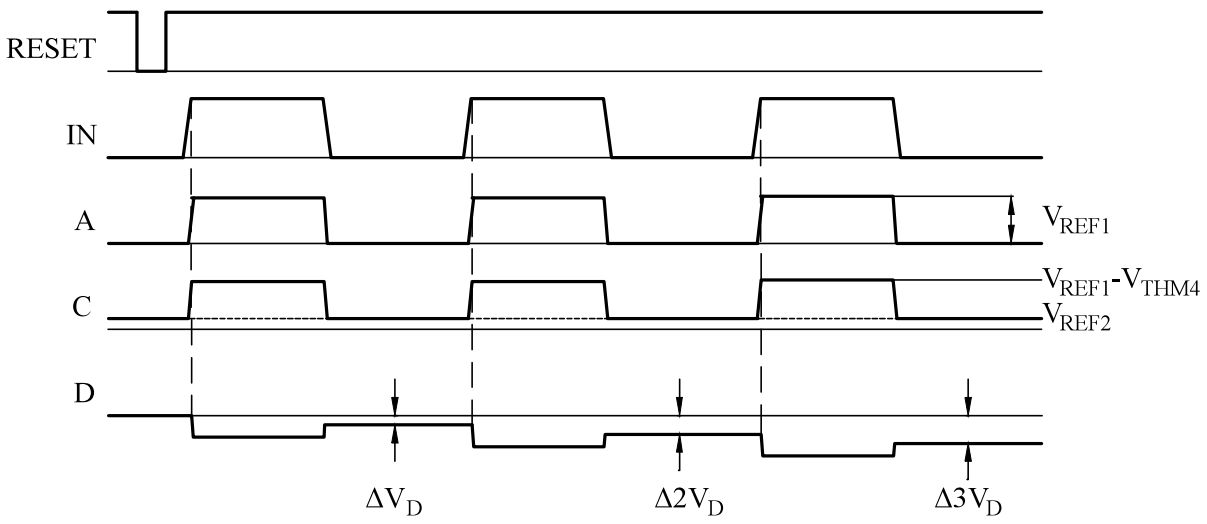

Figure 3.2: Timing diagram

3.1.1 Simulation results. Transient response

According to Equation 3.2, the step size, hence, the number of steps per acquisition (which should preferably be large) depends on the C_P to C_{M6} capacitance ratio. While C_P is a parasitic capacitance depending on the technological characteristics and layout design of transistors M_4 and M_5, the value of C_{M6} is designed as big as possible proportionally to the occupied area of transistor M_6. In order to obtain shot-noise limited operation, the capacitance ratio should be large enough to provide a voltage step considerably larger than the noise background. The main noise contribution at the output is due to the thermal noise of the readout chain, which can be estimated in the order of 1 mV RMS. Therefore, a voltage step of at least 3-5 mV is desirable to guarantee a single-photon counting resolution. For the current design the capacitance C_{M6} is set to 350 fF, whereas C_P is estimated to be 1.5 fF. The voltage step ΔV_D, and therefore the counting resolution, can be adjusted by changing the reference values V_{REF1} and V_{REF2}. To quantify the tunability of ΔV_D, a set of simulations was performed where V_{REF1} was varied from 1.2 to 3.2 V and V_{REF2} was in

the range 0.1-0.3 V. Figure 3.3 shows the results of a transient simulation, where the IN signal had a pulse period of 2 μs, a pulse width of 100 ns, and the reference voltage V_{REF1} was kept at 2 V. Easy to notice that a larger voltage step could be achieved at higher voltage V_{REF2}.

The output voltage step as a function of count number is presented in Figure 3.4. As it can be seen, a wider voltage step could be achieved with a higher voltage V_{REF2} assuring a linear output for a large fraction of the available output range. From the graph it is evident, the output step remains linear for about 150 steps, corresponding to a counting resolution of at least 7 bits. Then, the voltage step decreases as V_{DS} of transistor M_4 approaches 0 turning the transistor off.

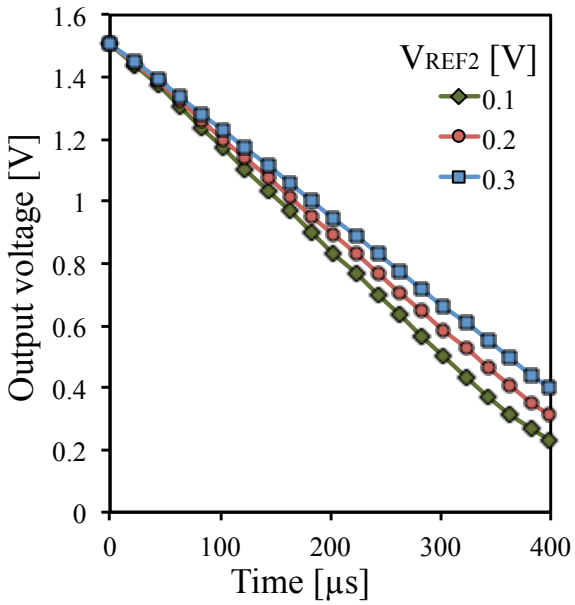

Figure 3.3: Transient simulations at different V_{REF2}

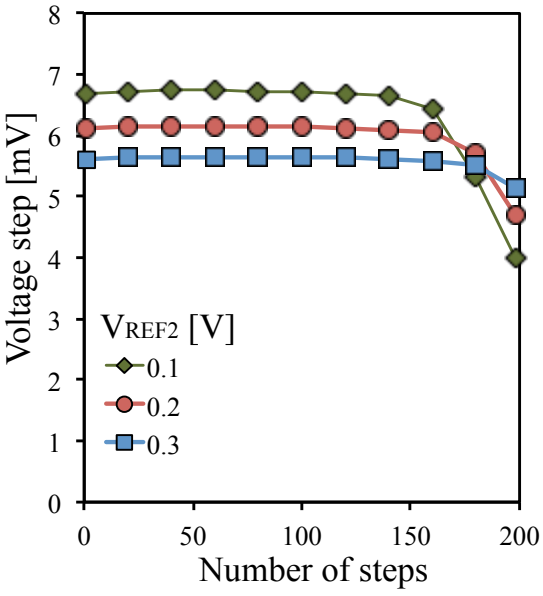

Figure 3.4: Output voltage step as a function of count number

The circuit layout for a standard 0.35 μm CMOS technology is depicted in Figure 3.5. The circuit occupied area is 230 μm^2.

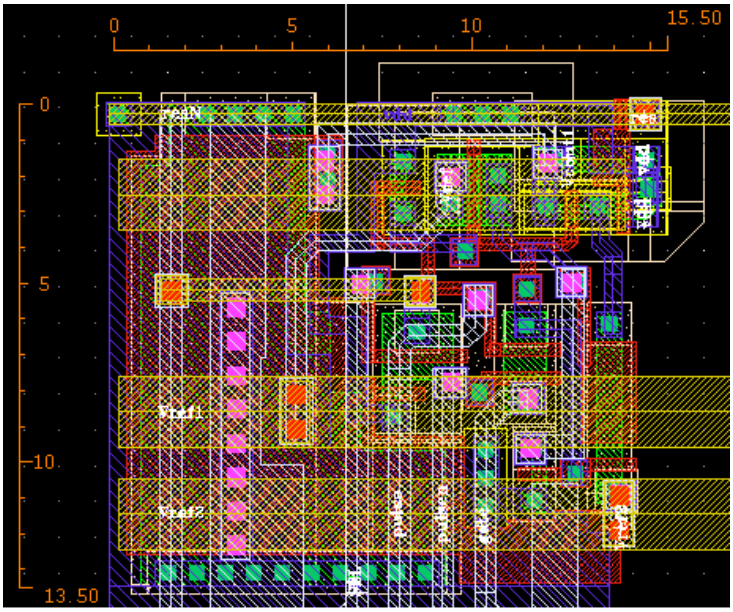

Figure 3.5: Counter layout

3.2 Circuit II. Analog Readout Circuit Based on Resistive Switch Principle

This circuit is based on the work previously reported in [143, 144] by FBK. The design in [143, 144] included only NMOS transistors and had the shortcomings of high power consumption in inverter and high non-uniformity of 11%. In order to improve the circuit performance, PMOS transistors were exploited. This design modification leads to an increase of the circuit area as n-well regions should be included to accommodate the p-type MOSFETs.The non-uniformity was improved with a careful design based on Monte Carlo simulations.

The readout circuit consists of a passive quenching circuit, an inverter, a gating circuit and an analog counter. The gating circuit works as a shutter, enabling pulse transmission to the next stage only when an event is detected inside a predefined observation window. The last circuit block, which provides the same functionality as a digital counter but in a reduced area, delivers an output voltage proportional to the number of counts inside the observation window. The schematic of Circuit II is shown in Figure 3.6.

Table 3.2 contains dimensions of the MOS transistors in Circuit II.

Figure 3.7 depicts the most relevant signals. The operation principle is described in the following. The SPAD is connected to a passive quenching circuit formed by transistor M_1. The circuit quenches the SPAD after each avalanche event and recharges the detector to the initial operating conditions. Transistor M_2 is used to clamp the voltage pulse at node 2. This approach is used to isolate the circuit from high excess bias voltage applied to the SPAD, which may damage transistors M_3 and M_4. Moreover, it reduces the impact of SPAD pulse amplitude non-uniformity. Thus, a SPAD ignition creates a positive clamped pulse at node 2. Then, the pulse

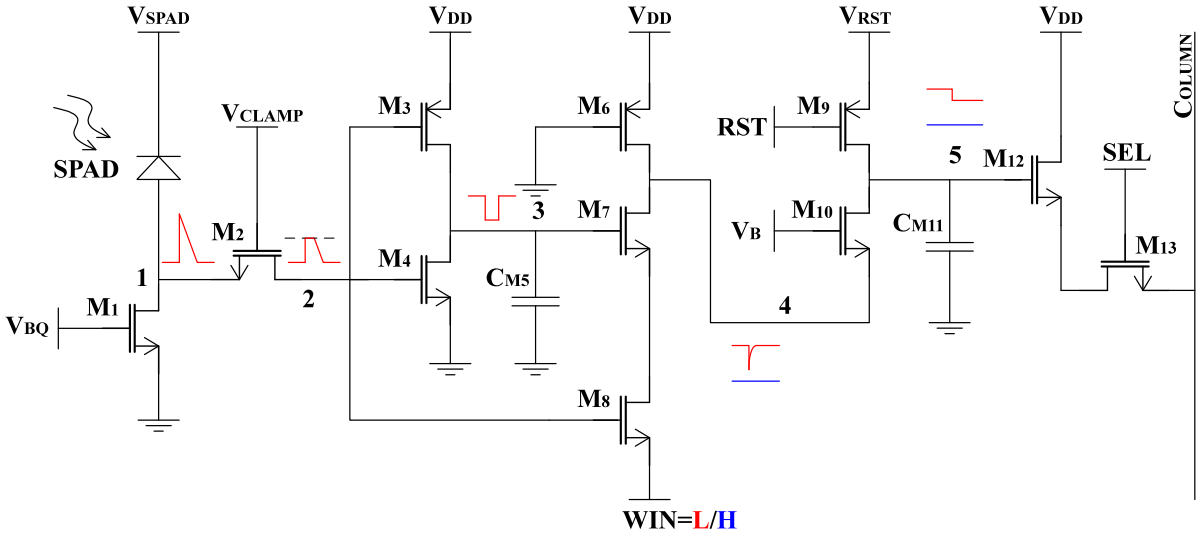

Figure 3.6: Schematic of Circuit II, based on resistive switch counter

Transistor Name	W/L, μm	Transistor Name	W/L, μm
M_1	0.80/7.0	M_8	3.5/0.35
M_2	3.0/0.35	M_9	0.80/0.35
M_3	0.80/2.4	M_10(1 version)	0.80/4.0
M_4	2.4/1.6	M_10(2 version)	0.80/7.2
C_{M5}	2.0/1.2	C_{M10}	3.0/3.0
M_6	0.80/0.80	M_{12}	3.0/0.80
M_7	1.6/0.70	M_{13}	3.0/0.35

Table 3.2: Dimensions of the MOS transistors in Circuit II

is negated by the inverter composed by M_3 and M_4, thus, a slightly delayed negative pulse is created at node 3. The gating circuit is a NAND gate composed by transistors M_7 and M_8 with a resistive PMOS load M_6. The gating signal WIN applied at the source of M_8 defines the time window when the avalanche event can be counted. The negative pulse width at node 4 depends on the delay between signals at nodes 2 and 3. Thus, its value is adjusted by changing the value of MOS capacitor C_{M5}. The

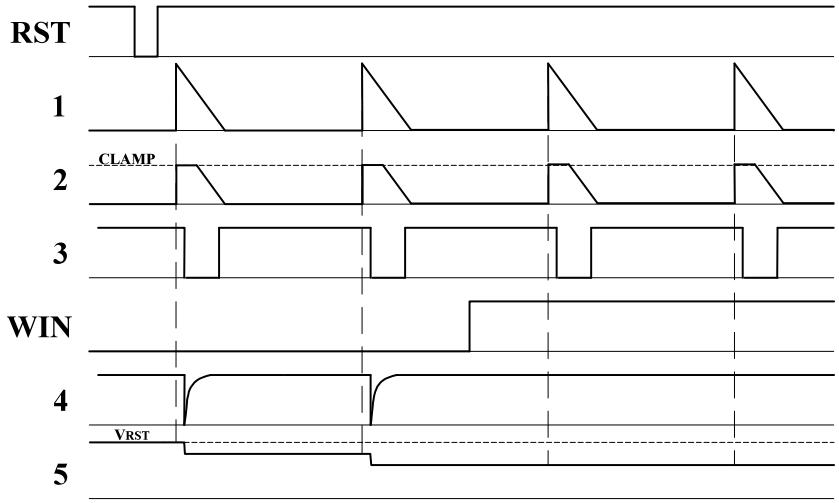

Figure 3.7: Voltage signals in Circuit II

circuit is capable of counting photon arrival event only when the gating signal WIN is in low state. The pulse at node 4 opens transistor M_{10} for a few hundreds picoseconds, so that a small charge packet is extracted from the MOS capacitance C_{M11}. As a consequence, a voltage step ΔV appears at the circuit output. This voltage step can be adjusted by biasing the reference voltage of M_{10}, V_B. If an avalanche event is triggered outside the gating window (signal WIN is high), no voltage drop is observed. The last part of the circuit is the same as used in conventional 3T active pixels. Transistor M_9 is used to reset the capacitance C_{M11} back to the value V_{RST}, while transistors M_{12} and M_{13} play the role of source follower and select switch, respectively.

3.2.1 Simulation results. Transient response

A set of simulations has been performed in order to better understand the circuit behavior and to adjust MOSFET parameters to the desired circuit characteristics. Transient simulations have been used to analyze the dynamic operation of the circuit, while Monte Carlo have been used to obtain

an estimation about the circuit non-uniformity. The circuit design has targeted the optimization in terms of timing resolution and area occupation. The pulse width at the gating circuit output node 4 has been set to be approximately 300 ps, ensuring a good compromise between gating resolution and uniformity of the response among different pixels. The channel length of transistor M_{10} has been carefully designed in order to find a compromise between the voltage step size and pulse width uniformity along the whole discharge ramp.

In order to achieve a relatively wide dynamic range for photon counting, the step size should be kept low. On the other hand, this voltage step has to be large enough to be easily discriminated from the electronic noise background that is typically in order of hundreds of μV - 1 mV. The simulations have been performed for different sizes of length and width of transistor M_{10}. The simulation results for two different widths of transistor M_{10} 4.0 μm and 7.2 μm are represented in Figure 3.8.

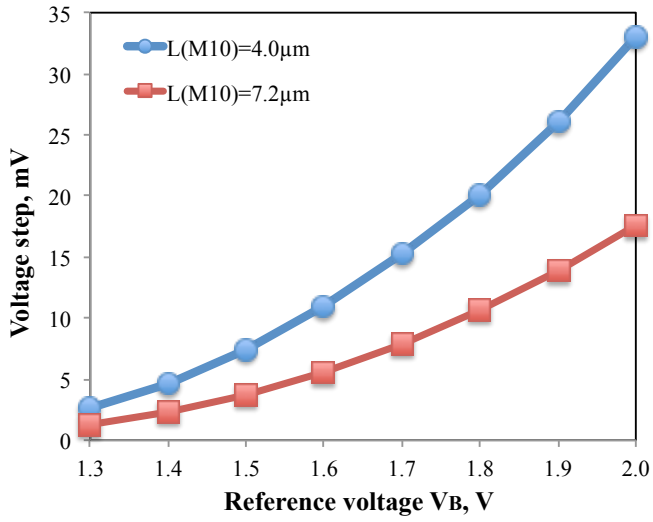

Figure 3.8: Average output step size as a function of reference voltage V_B. Data relevant to two gate lengths for transistor M_{10} are compared in the graph

3.2.2 Simulation results. Monte Carlo simulation

The mismatches between the different pixels of the array have been estimated with Monte Carlo simulation. The simulations have been performed for different sizes of length and width of transistor M_{10}. The simulation results for two different widths of transistor M_{10} 4.0 μm and 7.2 μm are represented in Figure 3.9 as these sizes are found to be a good trade-off between the step size and non-uniformity. The results show that uniformity among the pixels is below 10% for the whole range of V_B. The non-uniformity is lower at higher values of reference voltage V_B, since the threshold voltage mismatch of M_{10} becomes less relevant.

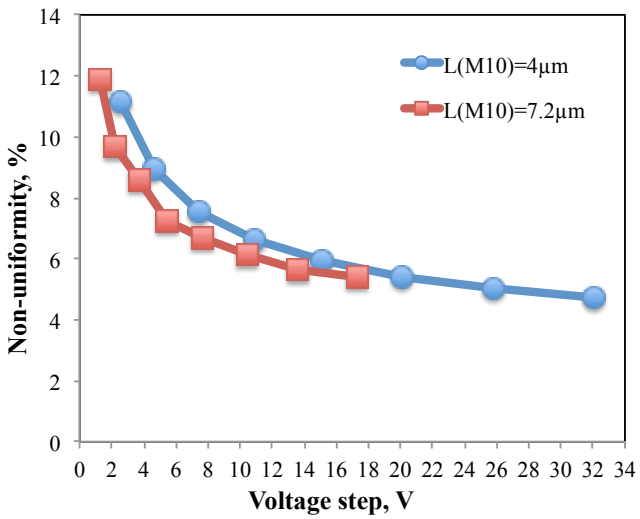

Figure 3.9: Voltage step non-uniformity as a function of voltage step. Data relevant to two gate lengths for transistor M_{10} are compared in the graph

3.2.3 Simulation results. Gated operation

Simulation results illustrating circuit operation in gated mode are reported in Figure 3.19. In this simulation, the SPAD generates an avalanche event every 50 μs, and a gating window signal WIN of 1 ns duration is applied in proximity of the avalanche discharge (Figure 3.18). At the beginning of the

simulation, signal WIN occurs 1 ns before the avalanche ignition. In this case, no discharge is observed in the circuits output. At each next cycle an additional delay of 50 ps is applied. After 20 cycles, which correspond to 1 ns additional delay, the gating window and the avalanche event of SPAD start overlapping, therefore, a voltage step appears at the output. The discharge continues for another 20 cycles, until the onset of avalanche events exits the gating window and the output capacitance discharge stops. The voltage step as a function of time delay is shown in Figure 3.12. The width of the curve is determined by the overlapping of two signals: of the width of the gating circuit output pulse at node 4 and the width of the gating window WIN. The steepness of the edges limits the minimum applicable gating window. For the present configuration, the minimum width is in the order of a few hundred ps, thus supporting the feasibility of sub-nanosecond time-gated operation.

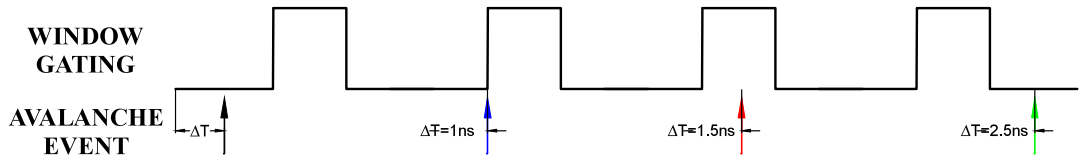

Figure 3.10: Timing diagram of gating window and avalanche events used in the simulation

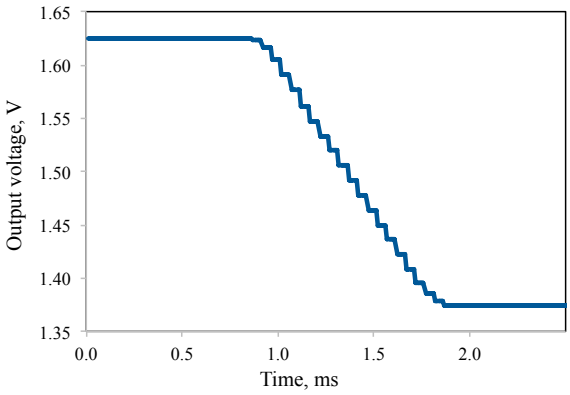

Figure 3.11: Output voltage of the circuit in gated operation

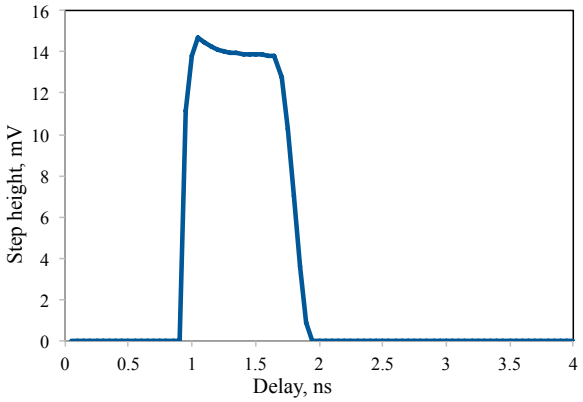

Figure 3.12: Voltage step as a function of time delay

3.3 Circuit III. Analog Readout Circuit Based on Charge Sharing

The circuit schematic is shown in Figure 3.13. The passive quenching circuit and the time gating circuit remain the same as in Circuit I (Figure 3.6), the analog counter based on charge sharing between a small parasitic capacitance C_P and NMOS capacitor C_{M12} connected in parallel. Table 3.3 contains dimensions of the MOS transistors in Circuit III.

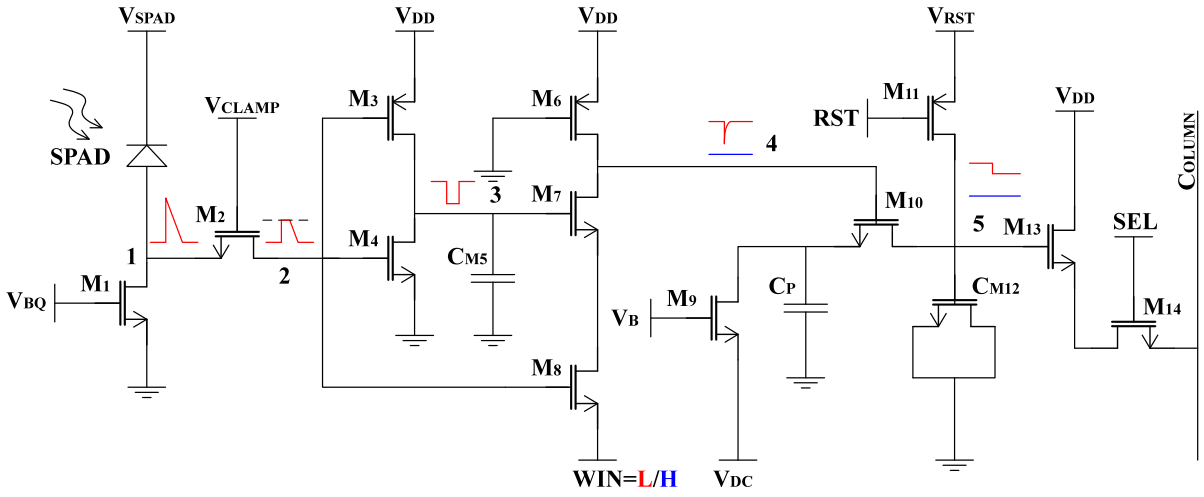

Figure 3.13: Schematic of the analog readout circuit based on charge sharing

The passive quenching circuit, the inverter and window gating circuit are realized similarly to Circuit II described in 3.2. At the beginning of an operation cycle, the capacitance C_{M12} is reset to V_{RST} voltage. Transistor M_9 provides a small current to charge C_P at the reference voltage V_B. The reference voltage V_B ensures a continuous reset of C_P. The current flowing through transistor M_9 can be adjusted so that capacitance C_P is fully discharged during the SPAD dead time, while the contribution of the current flowing through M_9 when M_{10} is closed is negligible. The MOS switch M_{10} is exploited to enable the charge transfer between C_{M12} and C_P, which takes approximately a few hundreds picoseconds. The pulse at

Transistor Name	W/L, μm	Transistor Name	W/L, μm
M_1	0.80/0;7	M_9	0.80/0.35
M_2	3.0/0.35	M_{10}	0.80/0.35
M_3	0.80/2.4	M_{11}	0.80/0.35
M_4	2.4/2.6	C_{M12}(1 version)	8.0/8.0
C_{M5}	2.0/1.2	C_{M12}(2 version)	8.0/4.0
M_6	0.80/0.80	C_{M12}(3 version)	4.0/4.0
M_7	1.6/0.70	M_{13}	2.0/0.80
M_8	3.5/0.35	M_{14}	2.0/0.35

Table 3.3: Dimensions of the MOS transistors in Circuit III

node D is wide enough to open transistor M_{10} for at the time required for a complete charge sharing. At each avalanche event, the switch M_{10} closes the circuit, and the voltage on the node B decreases by ΔV:

$$\Delta V = \frac{C_P}{C_P + C_{M12}} (V_{OUT} - V_B) \tag{3.3}$$

After reset phase $V_{OUT} = V_{RST}$, equation 3.3 can be used to calculate the initial step size. As in the previous circuit, a source follower (M_{13}) and a selection switch (M_{14}) complete the pixel.

3.3.1 Simulation results. Transient response

Transient simulations of the circuit output have been performed and are shown in Figure 3.14. Following the Equation 3.3, the amplitude of the following steps progressively reduces.

The ratio between capacitances C_P and C_{M12} determines the maximum number of counts that can be accumulated by the circuit. The capacitance C_P should be preferably much smaller than C_{M12} to obtain a significant number of steps (100-200) per acquisition before performing a read-out operation. A calibration is required to estimate the actual num-

ber of counts from the pixel output, due to the non-linear dependence of output voltage on count number. Despite the complexity of the calibration, the intrinsic signal compression may be exploited to expand the dynamic range.

A set of simulations was performed to evaluate the influence of the capacitance C_{M12} on the step height and the non-linearity of the circuit. Figure 3.14 shows the results of a transient simulation in the presence of an avalanche pulse train with 50 μs period. During this simulation the gating signal WIN was kept low, thus, all the avalanche events were counted. The simulation result represents the pixel output voltage at several different values of the capacitance C_{M12}. The value of parasitic capacitance C_P remained unchanged. As expected, a larger capacitance value of C_{M12} causes a smaller voltage step. This implies that a larger number of counts can be accumulated until the full discharge of the capacitance. The drawback of a larger capacitance is a large pixel area. To obtain an output voltage step in the range of 8 to 18 mV, the optimal capacitance of transistor C_{M12} lays between 200 and 400 fF.

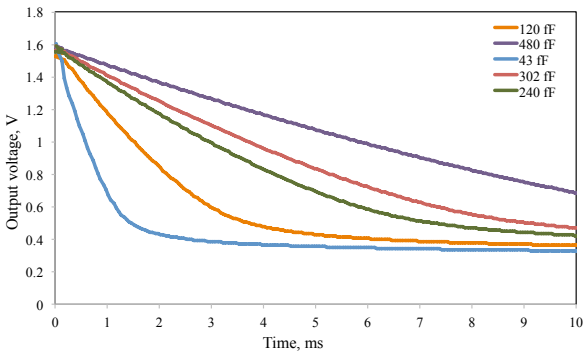

Figure 3.14: Simulated pixel output as a function of time for different values of MOS capacitance C_{M12}

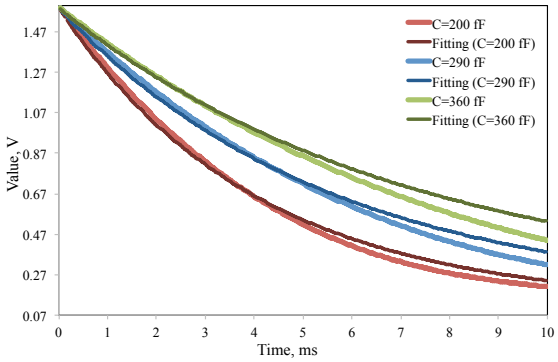

Figure 3.15: Simulated and theoretical fitting (Equation 3.3) curves representing the discharge of capacitance C_{M12}

The comparison of the obtained results with the exponential expected decay helps to predict and evaluate the measurement error. Figure 3.15

shows the deviation of the simulated curve from the theoretical fitting according to Equation 3.3. As it can be seen, the curves concur and thus the accuracy can be easily calibrated.

3.3.2 Simulation results. Monte Carlo simulation

The circuit non-uniformity mainly depends on the mismatch between capacitances C_1 and C_{M12} and might degrade if the value of C_P is too small. An optimized configuration can be found with simulations on the circuit parameters. Monte Carlo method was exploited to estimate the non-uniformity of output voltage step ΔV among all pixels in an array. Figure 3.16 displays the dependence of average voltage step height on the value of capacitance C_{M12}. Evidently, lower voltage step can be obtained with larger capacitance.

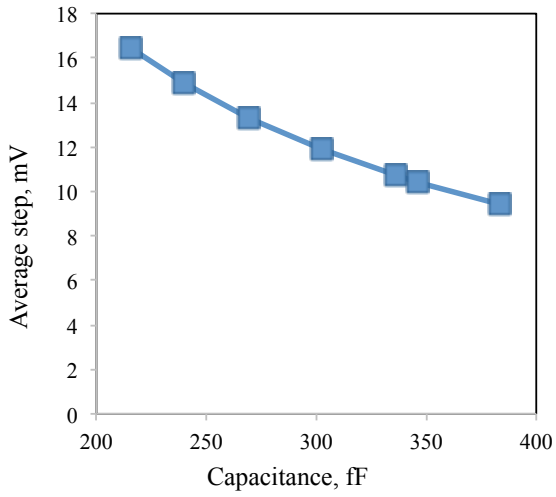

Figure 3.16: Dependence of the average step height ΔV on the value of capacitance C_{M12}

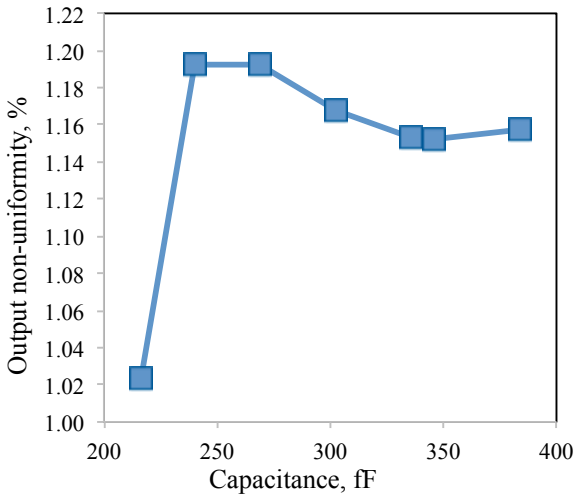

Figure 3.17: Dependence of output non-uniformity on the value of capacitance C_{M12}

Output step non-uniformity as a function of the value of capacitance C_{M12} is represented in Figure 3.17.

The simulation shows that the circuit can achieve a remarkable non-uniformity of approximately 1%. This value can be considered independent

on the value of capacitance C_{M12} value. According to design requirements, the choice of the capacitance size depends on the area available for the circuit design and the desirable number of counts per acquisition.

3.3.3 Simulation results. Gated operation

The circuit output voltage with gated operation is shown in Figure 3.18. Similarly to Circuit I, a 1-ns gating window with an additional delay of 50 ps at each step was applied. Thus, in the beginning of the simulation avalanche events are outside the observation window. After 20 steps, corresponding 1 ns delay, the avalanche event and time window start overlapping, thus, activating the counting circuit. An output discharge ramp is observed while the two pulses overlap. After another nanosecond, avalanche events fall again outside of the window and the discharge ramp is stopped.

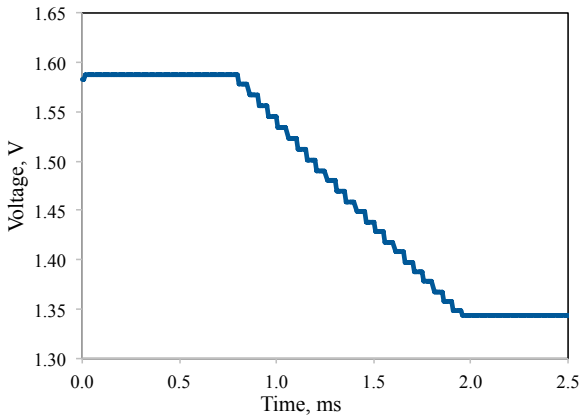

Figure 3.18: Simulated pixel output with gated operation: output voltage as a function of applied time delay

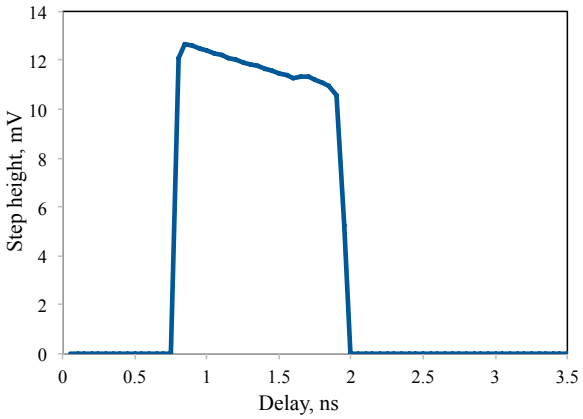

Figure 3.19: Simulated pixel output with gated operation: output voltage step as a function of applied time delay

The output voltage step as a function of applied time delay is shown in Figure 3.19. In comparison to Circuit I, the step size is not constant as it can be seen from the middle part of the curve. The non-linearity is due to the non-linear charge sharing process.

3.4 Circuit IV. Analog Readout Circuit with High-Pass Filter

The circuit described in this paragraph was designed in SOI, FBK and fabricated in a 0.15 μm technology on the same chip with the circuits presented in 3.2 and 3.3. I have been involved into the experimental characterization of the circuits reported hereafter.

3.4.1 Operating principle: First Version

The analog readout circuit is realized on only 9 NMOS transistors and consists of a passive quenching circuit, a gating circuit and an analog counter. The schematic of the analog circuit is represented in Figure 3.20. Table 3.4 contains dimensions of the transistors used in 1st structure.

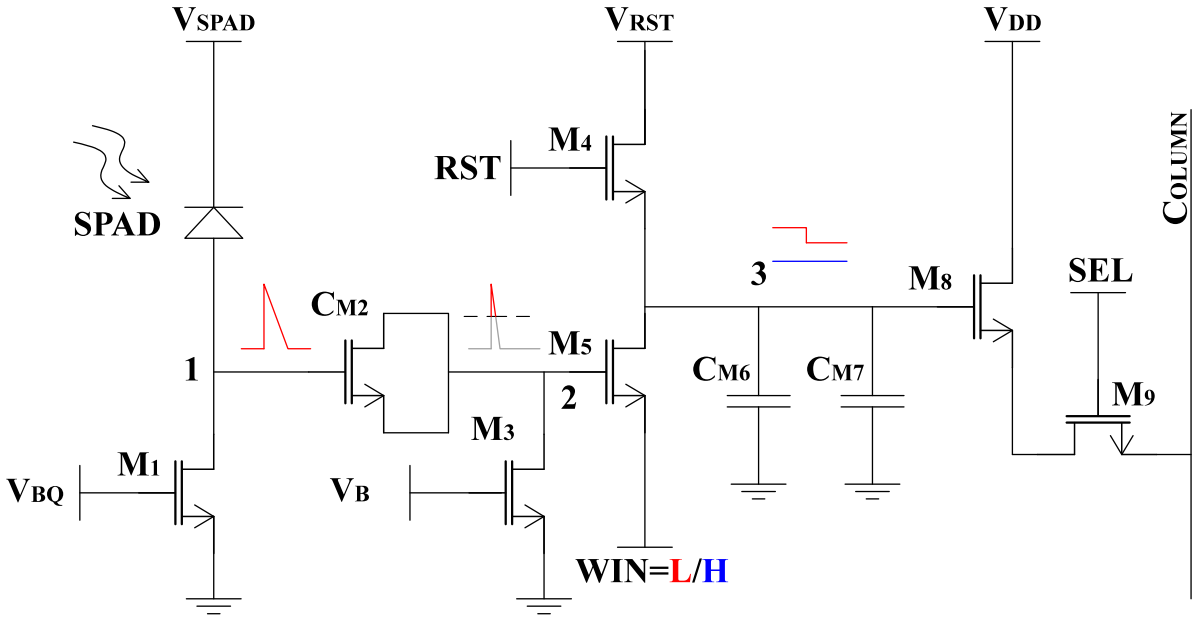

Figure 3.20: Circuit IV. Schematic of the first version

The operating principle is described in the following. To reset SPAD to its operating conditions after each detection event, a passive quenching

Transistor Name	W/L, μm	Transistor Name	W/L, μm
M_1	0.80/3.0	C_{M6}	2.0/1.0
M_2	1.0/2.0	C_{M7}	1.0/7.0
M_3	1.0/1.0	M_8	3.0/0.8
M_4	1.0/0.35	M_9	3.0/0.35
M_5	0.8/2.0		

Table 3.4: Dimensions of the MOS transistors. First version

circuit is realized on transistor M_1 connected to the anode of SPAD. Transistors M_2 and M_3 operate as a passive first-order high-pass filter, realized by RC circuit. The positive ignition pulse from SPAD at node 1 passes through this filter and, therefore, a reduced short positive pulse appears at node 2. The pulse width depends on the dimensions of transistor M_2 and M_3 and typically is designed to be of a few hundreds of picoseconds. The gating signal WIN is applied at the source of M_5 and defines the time window when the avalanche event can be counted. The circuit is capable of counting photons only when the gating signal WIN is in low state. The pulse at node 2 is delivered to the gate of transistor M_5 and turns it on for a few hundreds of picoseconds, so that a small charge packet is extracted from the MOS capacitances C_{M6} and C_{M7}. As a result, a voltage step ΔV appears at the circuit output. This voltage step can be adjusted by changing the reference voltage V_B, thus, changing R constant in RC circuit. If an avalanche event is triggered outside the gating window (signal WIN is high), no voltage drop is observed in the output. Transistor M_4 is used to reset the capacitances C_{M6} and C_{M7}. As a consequence the capacitance is recharged to the mean between $V_{RST} - V_{THM4}$ and V_{DD} as the chip has been designed so that V_{DD} is the reset voltage. Transistors M_8 and M_9 realize a source follower and select switch, respectively.

The timing diagram of the main meaningful signals at the nodes is

represented in Figure 3.21.

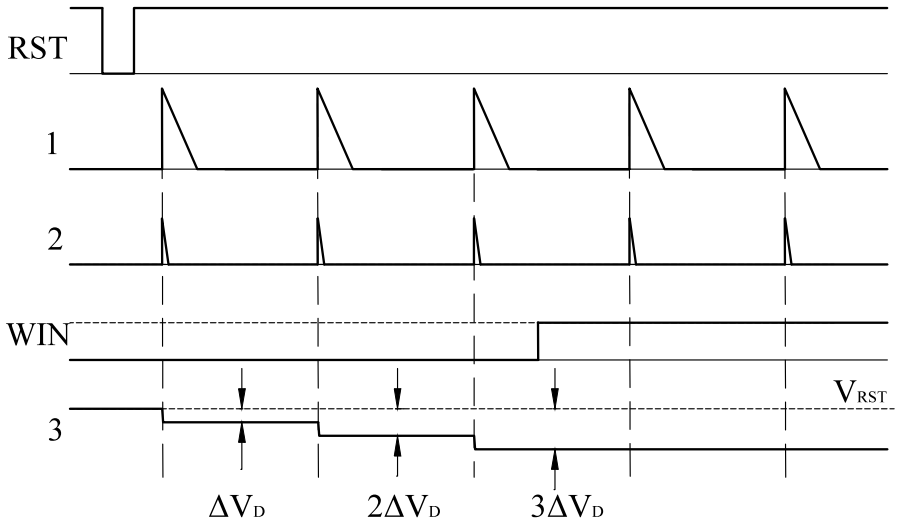

Figure 3.21: Timing diagram of the first structure

3.4.2 Simulation results. Transient response

A set of simulations has been performed to analyse the circuit behaviour and set the operating range. To estimate the dynamic range of the circuit, transient simulations have been performed. The key parameter assuring a wide dynamic range is the value of reference voltage V_B. Applied to the gate, voltage V_B changes its conductivity of transistor M_3, thus, RC constant in high-pass filter formed by C_{M2} and M_3. In order to estimate the step size linearity and dynamic range of the circuit as a function of V_B, the simulations have been performed for different V_B values. The transient response at different values V_B are shown in Figure 3.22. Figure 3.23 shows the output voltage step size in dependence on V_B. According to this data, the dynamic range and non-linearity has also been estimated.

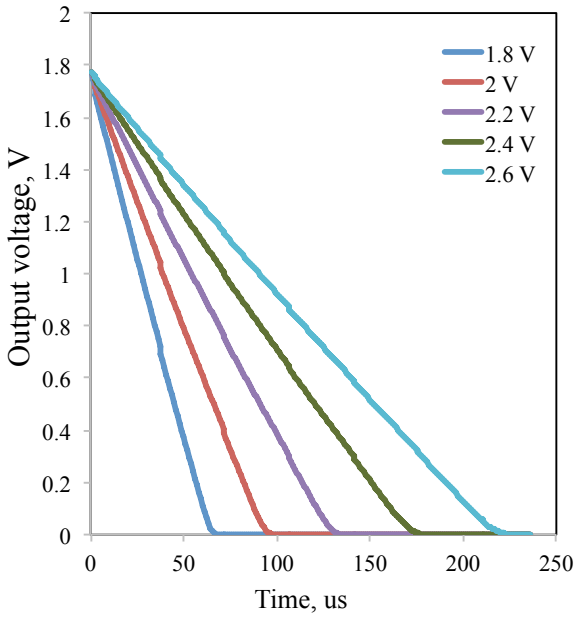

Figure 3.22: Circuit IV: first version. Transient response at different values V_B

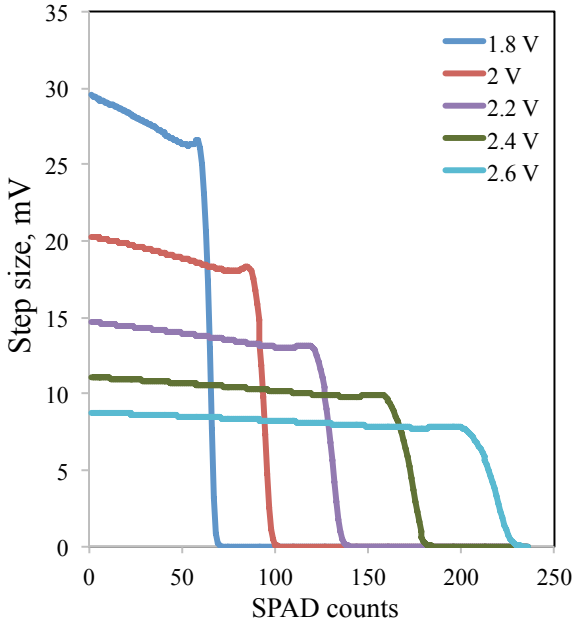

Figure 3.23: Circuit IV: first version. Output voltage step size as a function of SPAD counts

3.4.3 Simulation results. Monte Carlo simulation

Non-uniformity between the different pixels has been calculated with Monte Carlo simulation. The simulations have been performed for different reference voltage values V_B and are shown in Figure 3.24. A 7% non-uniformity among the pixels was achieved for the range of V_B from 1.8 to 2.6 V. As at higher voltages of V_B nMOS transistor M_3 exits from ohmic region into saturation, the step size stops increasing. The non-uniformity is slightly larger for smaller steps (8.7%). Average circuit non-linearity in dependence on voltage V_B is shown in Figure 3.25.

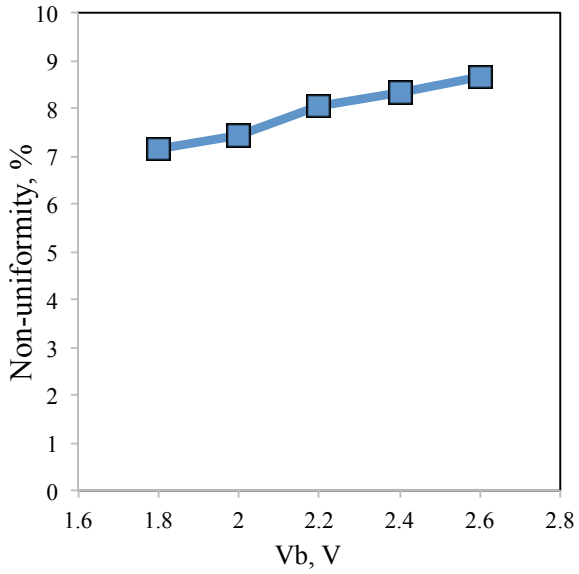

Figure 3.24: Circuit IV: first version. Output step non-uniformity as a function of reference voltage V_B

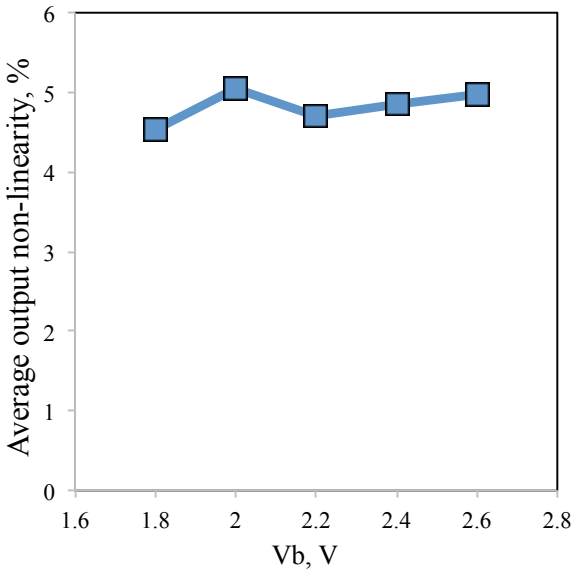

Figure 3.25: Circuit IV: first version. Average output step non-linearity as a function of reference voltage V_B

3.4.4 Operating principle: Second version

Similarly to the structure described in 3.4.1, this circuit of analog readout comprises a passive quenching circuit, a gating circuit and an analog counter. The circuit is composed by 10 NMOS transistors. Circuit schematic is represented in Figure 3.26.

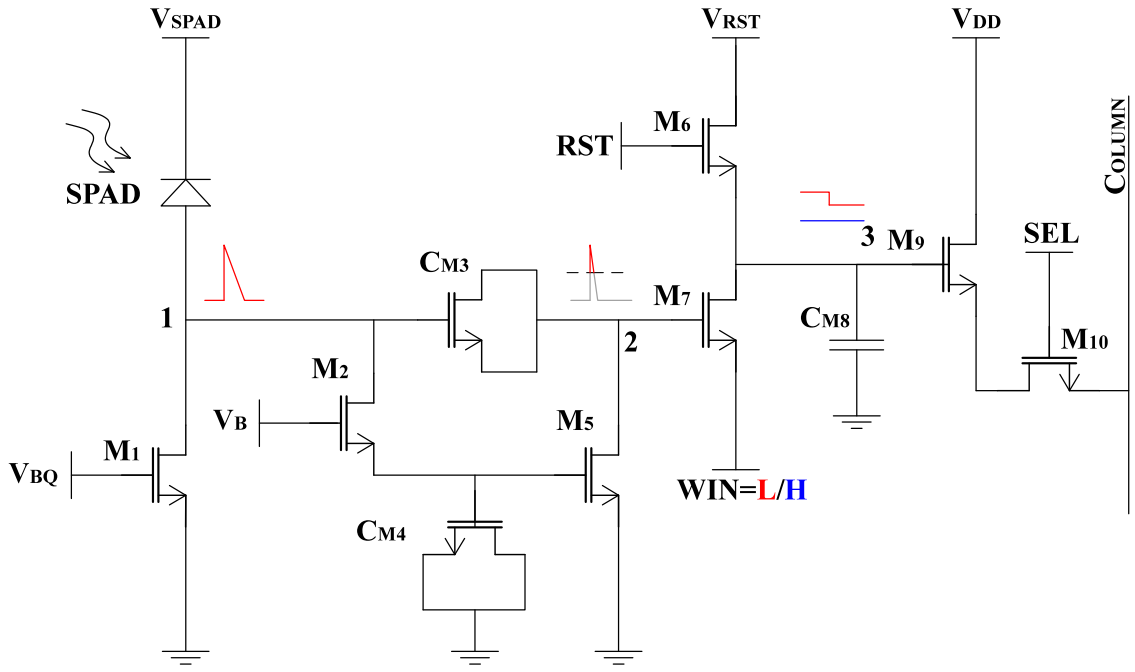

Figure 3.26: Circuit IV. Schematic of the second version

Table 3.5 contains dimensions of the transistors used in 2nd structure.

Transistor Name	W/L, μm	Transistor Name	W/L, μm
M_1	0.80/7.0	M_6	1.5/0.35
M_2	5.0/1.0	M_7	1.5/6.0
M_3	5.6/4.5	C_{M8}	5.0/5.0
M_4	2.5/2.0	M_9	3.0/0.8
M_5	5.0/0.7	M_{10}	3.0/0.35

Table 3.5: Dimensions of the MOS transistors. Second version

The operating principle is described in the following. A passive quenching circuit restoring SPAD after photon detection is realized on transistor M_1 that is connected to the anode of SPAD. Transistors M_2, M_3 and MOS capacitances C_{M3} and C_{M4} form a high-pass filter. The positive ignition pulse from SPAD at node 1 passes through this filter and, therefore, a reduced short positive pulse is appears at node 2. The pulse width depends on the dimensions of transistor M_2, C_{M3}, C_{M4} and M_5.

The main difference from the structure reported in 3.4.1 is that the circuit implements a sort of "dynamic" RC circuit, as V_g in M_5 (thus, the R in the RC circuit) varies during the event. The goal was to generated at node 2 a pulse which is higher but shorter in time compared to the previous configuration. The circuit works as following: before the avalanche, resistor M_5 is off, as node 1 is tied to ground through transistor M_1. When a photon is detected, the pulse in node 1 appears in node 2. As the R is almost 0 at the very beginning of the event, the pulse in node 2 is higher than in the previous circuit 3.4.1. Few tens of picoseconds after the rising edge of the event, the pulse is transferred to the gate of M_5 through transistor M_2, thus increasing the R in the RC circuit. In this way, the pulse is node 2 is clamped.

The gating circuitry is enabled with WIN signal applied at the source of M_7. WIN defines the time window when the avalanche event can be counted. Thus, photons can be counted only when the gating signal WIN is in low state. The SPAD pulse at node 2 is delivered to the gate of transistor M_7 and turns it on for a few hundreds picoseconds, and a small charge packet is extracted from the MOS capacitance C_{M8}. As a result, a voltage step ΔV is observed at the circuit output. This voltage step can be adjusted by changing the reference voltage V_B, thus adjusting the reaction time of the RC circuit. A higher V_B generates shorter but lower pulses at node 2. If an avalanche event is triggered outside the gating window (signal

WIN is high), no voltage drop is observed in the output. Transistor M_6 is used to restore the capacitance C_{M8} to the initial value V_{RST}. Transistors M_9 and M_{10} function as a source follower and select switch, respectively.

The timing diagram of the main meaningful signals at the nodes is represented in Figure 3.27.

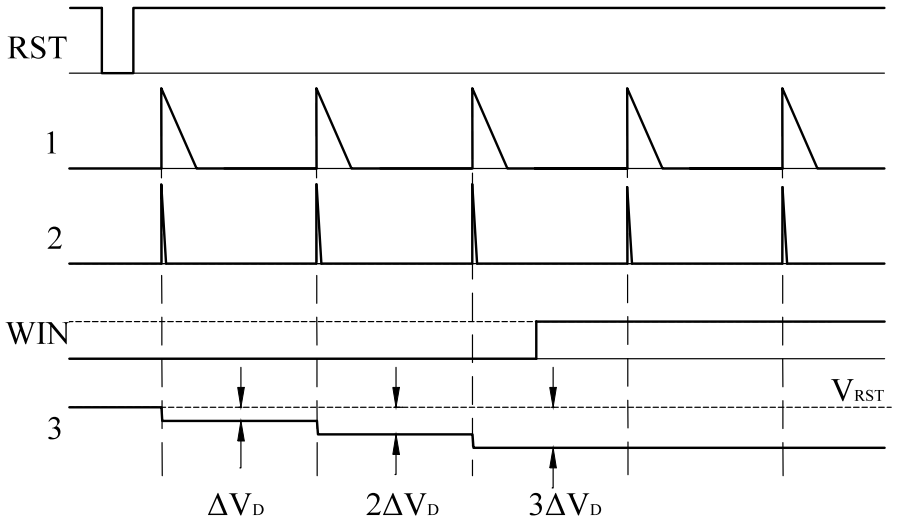

Figure 3.27: Timing diagram of the second structure

3.4.5 Simulation results. Transient response

Simulations on transient response have been carried out to evaluate the circuit performance and adjust parameters. Dynamic range depends on the voltage step that was calculated in dependence on the value of reference voltage V_B. Similarly to the circuit 3.4.1, V_B changes R parameter in high-pass filter formed by C_{M3}, C_{M4}, M_2 and M_5. The transient response at different values V_B are shown in Figure 3.28.

Figure 3.29 shows the output voltage step size in dependence on V_B. According to this data, the dynamic range and non-linearity has also been estimated.

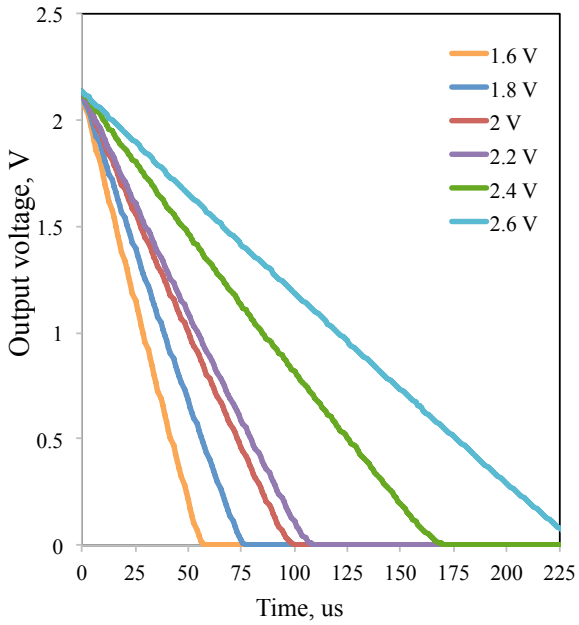

Figure 3.28: Circuit IV: second version. Transient response at different values V_B

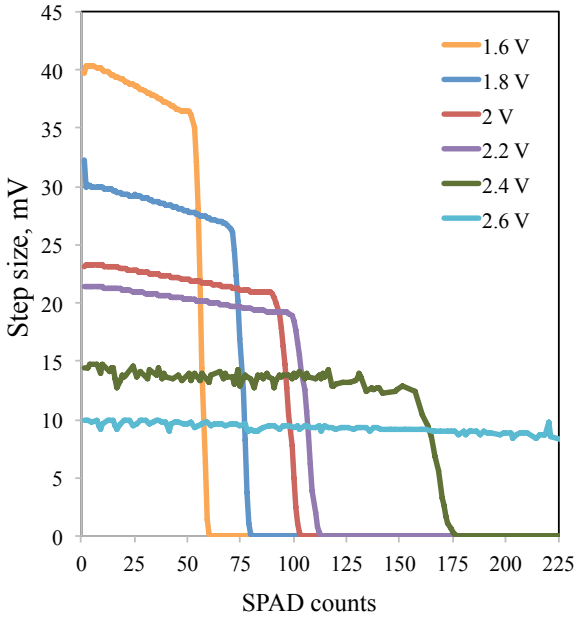

Figure 3.29: Circuit IV: second version. Output voltage step size as a function of SPAD counts

3.4.6 Simulation results. Monte Carlo simulation

Non-uniformity between the different pixels has been calculated with Monte Carlo simulation. The simulations have been performed for different reference voltage values V_B and are shown in Figure 3.30. A 7% non-uniformity among the pixels was achieved for the range of V_B from 1.8 to 2.6 V. As at higher voltages of V_B nMOS transistor M_3 exits from ohmic region into saturation, the step size stops increasing. The non-uniformity is slightly larger for smaller steps (8.7%). Average circuit non-linearity in dependence on voltage V_B is shown in Figure 3.31.

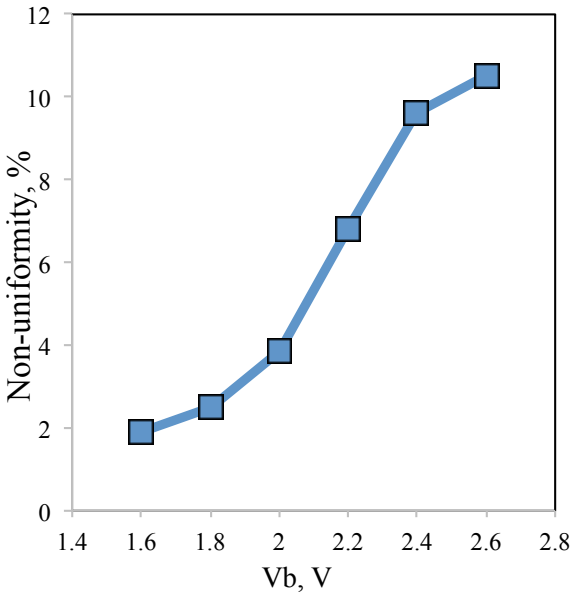

Figure 3.30: Circuit IV: second version. Output step non-uniformity as a function of reference voltage V_B

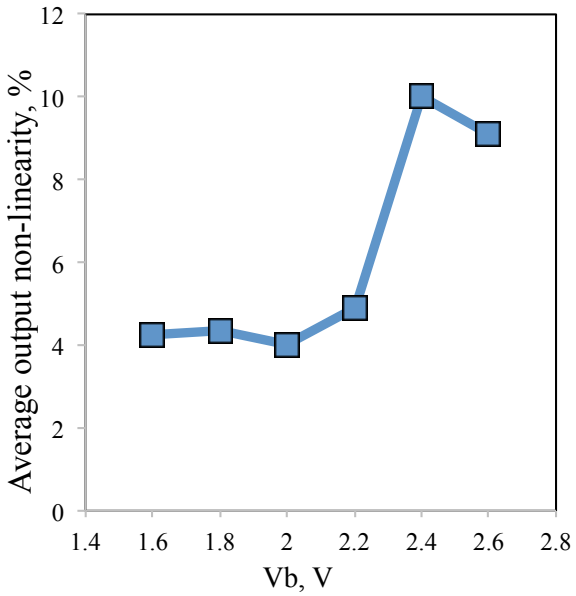

Figure 3.31: Circuit IV: second version. Average output non-linearity as a function of reference voltage V_B

Chapter 4

Chip Design and Experimental Setup

In this Chapter the architecture and the layout of the chip comprising Circuit II, Circuit III and Circuit IV are presented. In addition, the setup of the experimental bench used for the pixel optical characterization and time-gated operation is described.

4.1 SPAD Structure Implemented in Pixel

The SPAD structure presented in [133] has been chosen for integration into these arrays. This photodetector was designed in a 0.15 μm CMOS technology. Its cross-section is depicted in Figure 4.1. The structure is based on a p+/n-well active area junction, surrounded by a guard ring formed by a low-doped region where both p-well and n-well implantations were blocked. This low-doped guard ring formed around the junction prevents premature edge breakdown [85]. A metal shield created with the upper metal layers is used to stop the photons incident in non-active areas of the device.

The SPAD has an active area diameter of 10 μm and a breakdown voltage of 16.1 V. The SPAD has a high timing resolution of 60 ps and low dark count rate of 160 cps. This structure also possesses a low afterpulsing probability of 1.3% at 30 ns dead time and a photon detection probability

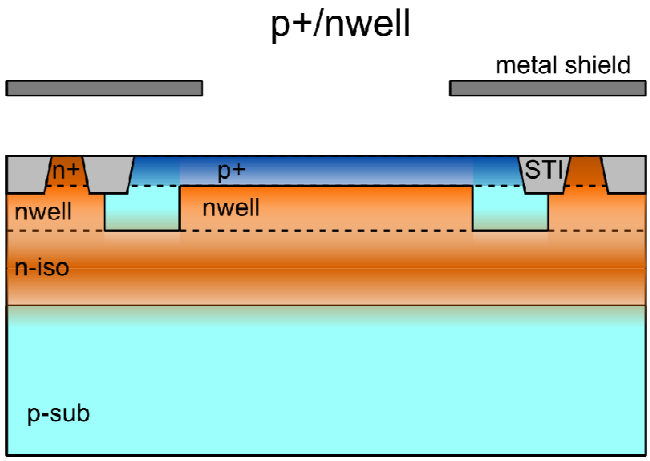

Figure 4.1: Cross-section of the SPAD included in the pixels [133]

of 26% at λ=470nm.

4.2 Chip Architecture

The readout circuits presented in 3.2, 3.3 and 3.4 have been assembled with SPADs into pixels and integrated into linear arrays. The sample layout of one of the pixels is shown in Figure 4.2. The layout of the pixels was not

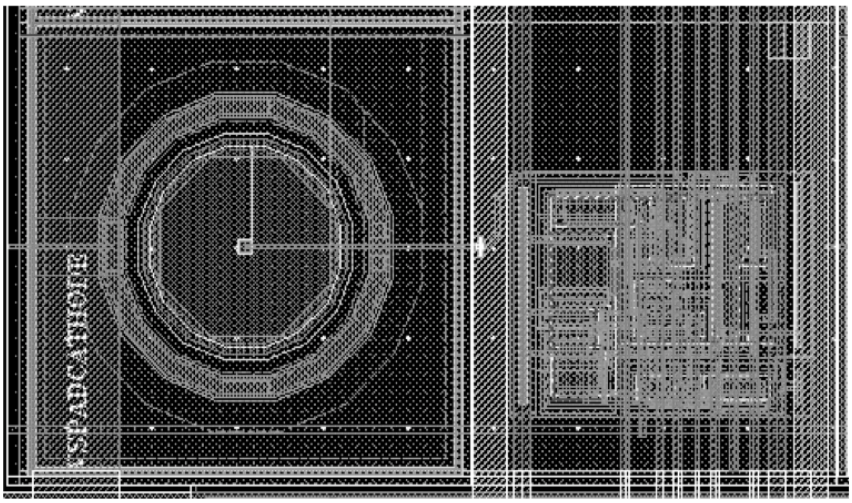

Figure 4.2: Pixel layout of Circuit II

optimized for high fill factor because information about the minimum guard ring size and device distance was still missing. Therefore, this design was mainly focused on the analysis of circuit functionality. In parallel, SPAD arrays with different distances and guard ring sizes have been implemented to independently optimize the detectors.

Several linear arrays of 40 pixels each have been fabricated in the same chip in 0.15 μm CMOS technology. The chip also includes peripheral electronics needed for proper array operation. The chip block diagram is depicted in Figure 4.3. The chip consists of the pixel linear arrays, row and

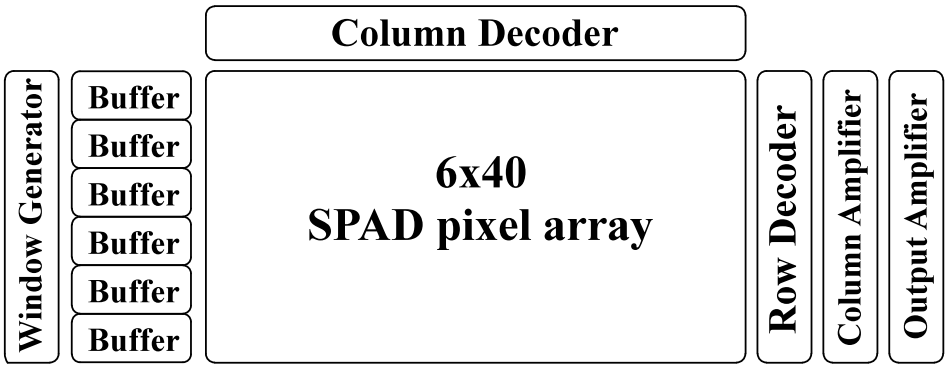

Figure 4.3: Block diagram of the chip

column decoders, column and output amplifiers, window generator and a buffer for each row. 6×40 array of pixels includes two rows with Circuit II in two different configurations, while Circuit III was implemented in three versions, each one in a different row. Circuit IV was included in the last row, with 15 pixels for each version.

Row and column decoders select one single row or column connecting the pixel outputs to the column amplifiers for readout. The decoders were implemented as shift registers with D-type flip-flops connected in series. While $RESET$ signal is shared with the row decoder, clock signals CLK are independent. Column and output amplifiers are composed of source followers.

The window generator has the function to combine two edges of the START and STOP signal, externally provided, and create an internal gating signal. This signal is then distributed to the pixel arrays through several digital buffers. The simulated timing diagram of the window generator is shown in Figure 4.4. The time window is generated according to $START$ and $STOP$ signals provided externally. The signals $START$ and $STOP$ are combined through a $NAND$ gate. In this way, a time window WIN as short as a few tens of picoseconds can be generated internally. This WIN signal is buffered and then delivered to the arrays. As it can be noted from the simulations in Figure 4.4 for a single pixel, $WINbuffered$ signal maintains the sharpness of the edges of WIN.

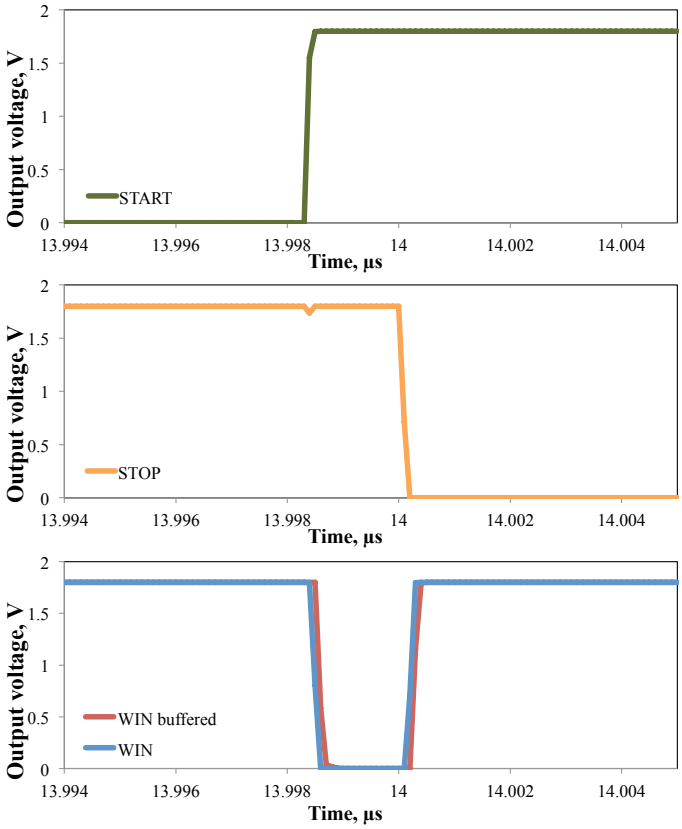

Figure 4.4: Simulations of the window generator operation

All these parts have been integrated in the same chip together with

other test circuits. The layout of the chip is is depicted in Figure 4.5 and a micrograph of the chip is shown in Figure 4.6.

Table 4.1 describes the input/output analog/digital signals required for pixel array operation.

A summary of the different pixels implemented in the array is presented in Table 4.2

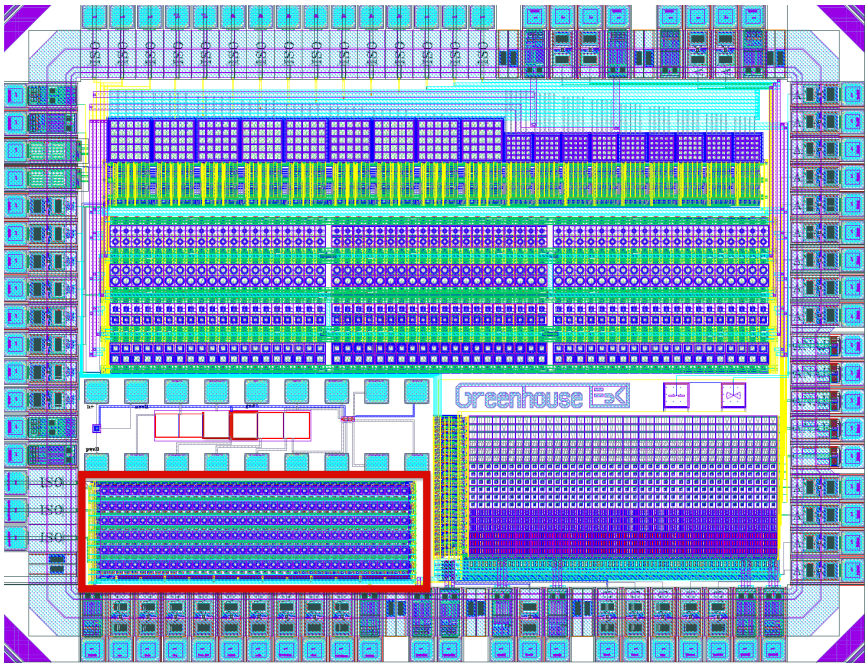

Figure 4.5: Chip layout. The SPAD pixel arrays are highlighted in red

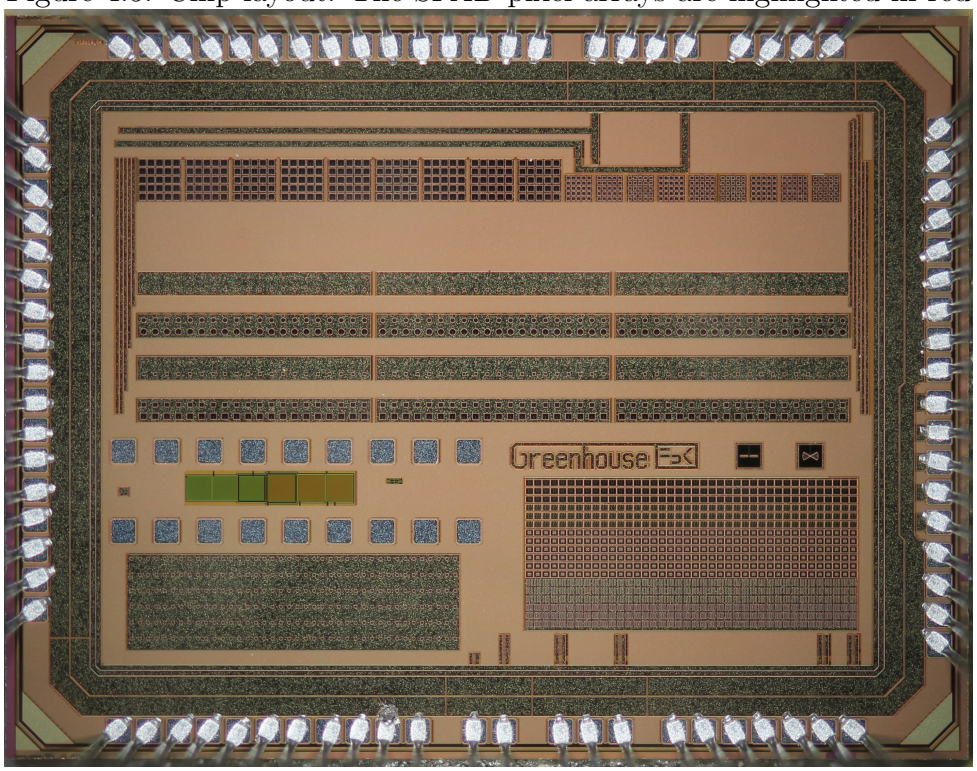

Figure 4.6: Chip micrograph

Signal Name	Value	Function	Circuit
Power supply			
$V_{SPAD.II}$	$\geqslant$19 V	SPAD bias voltage	
$V_{SPAD.III}$	$\geqslant$19 V	SPAD bias voltage	
$V_{SPAD.IV}$	$\geqslant$19 V	SPAD bias voltage	
$V_{DD(1.8)}$	1.8 V	Pixel supply voltage	
$V_{DD(3.3)}$	3.3 V	Pixel supply voltage	
$V_{SS(1.8)}$	1.8 V	Digital supply voltage	
$V_{SS(3.3)}$	3.3 V	Digital supply voltage	
Analog signals			
V_{BQ}	2 V	Gate voltage of the quenching transistor M_1	
V_{CLAMP}	3 V	Voltage on the clamping transistor M_2	C.II, C.III
V_{RST}	2.6...3.3 V	Reset voltage value	
V_B	1.4...2.6 V	M_{10} gate voltage	C.II
V_B	1.65 V	M_9 gate voltage	C.III
V_B	1.8...2.6 V	M_2 gate voltage	C.IV (1v)
V_B	1.6...2.6 V	M_3 gate voltage	C.IV (2v)
V_{DC}	1 V	M_9 source bias voltage	C.III
Digital signals			
START	0...3.3 V	Gating window START	
STOP	0...3.3 V	Gating window STOP	
RST	0...3.3 V	Pixel reset	
SEL	0...3.3 V	Pixel select	
RST DEC	0...3.3 V	Column and row decoder reset	
CLK ROW	0...3.3 V	Column and row decoder clock	
CLK COL	0...3.3 V	Column and row decoder clock	
Reference currents			
Col.Amp	9 μA	Bias current of column amplifier	
Out.Amp	100 μA	Bias current of output amplifier	
Output voltage			
V_{OUT}		Output analog voltage	

Table 4.1: Supply, analog and digital I/O required for chip operation

Counter type	Configuration		Linear array
Resistive switch	Different switch M_{10} dimensions		
	1	W=0.8 μm; L=4.2 μm	40 pixels, 1st row
	2	W=0.8 μm; L=7.0 μm	40 pixels, 2nd row
Charge sharing	Different MOS capacitor M_{12} dimensions		
	1	W=8.0 μm; L=8.0 μm	40 pixels, 3rd row
	2	W=8.0 μm; L=4.0 μm	40 pixels, 4th row
	3	W=4.0 μm; L=4.0 μm	40 pixels, 5th row
High-pass filter	Different HPF structures		
	1	first version of HPF	15 pixels, 6th row
	2	second version of HPF	15 pixels, 6th row

Table 4.2: Circuit configurations implemented in the chip

4.3 Experimental Setups

In order to characterize the circuit performance several types of measurements have been carried out:

- counter characterization, to extract voltage step, electronic noise, linearity and non-uniformity;
- pixel optical characterization, to estimate both pixel output signal and noise as a function of incident light intensity;
- time-gated operation, to extract minimum observation window width at gated operation.

LabView software was used for signal control and for data analysis.

4.3.1 Counter characterization

Characterization of counter performance has been conducted using the setup shown in Figure 4.8. This setup was used for Circuits, II, III and IV, while for Circuit I the counter was characterized using electrical pulses. All analog and digital signals were generated with general purpose PXI-Analog/Digital test board PCI-6542 by National Instruments. During the measurements the window signal WIN was maintained in low state so that all the impinging photons could be detected. The chip was illuminated using a variable intensity wide-spectrum halogen light source. To generate a uniform light distribution, the sensor was exposed to the light through a diffuser. During the measurements the light intensity was varied to cover the whole dynamic range of the sensor from the dark to the saturation region. The output signal from the sensor board was acquired with the analog board. The sensor board is shown in Figure 4.7

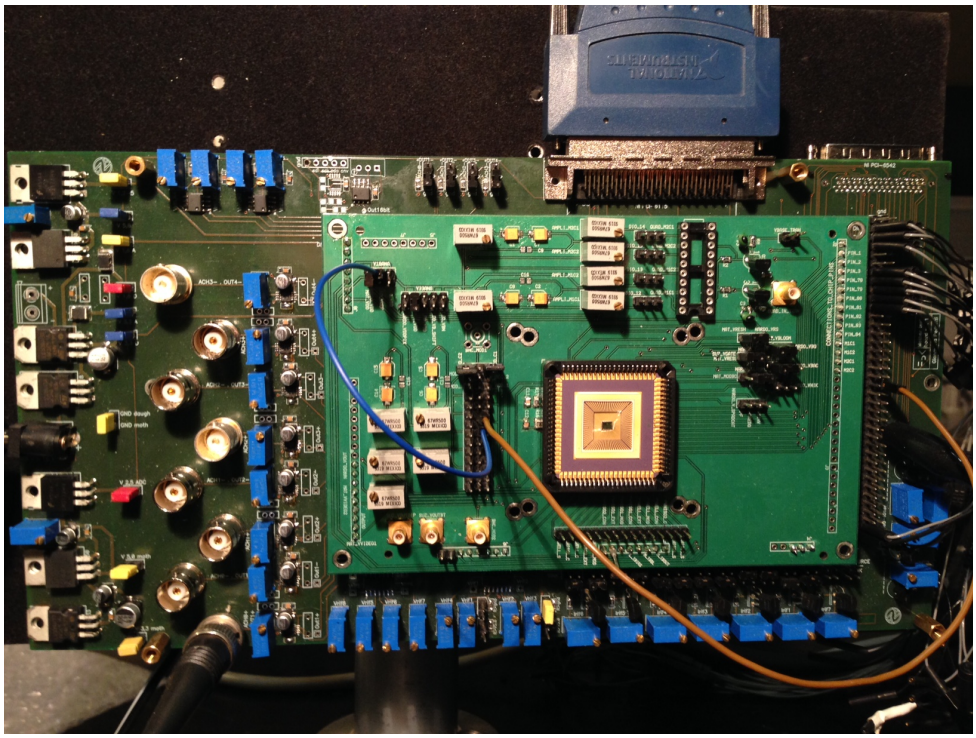

Figure 4.7: Sensor board

Through data analysis, the main counter performance parameters were obtained: dynamic range, linearity of the circuit, non-uniformity of the pixel response, and the electronic noise of the circuit.

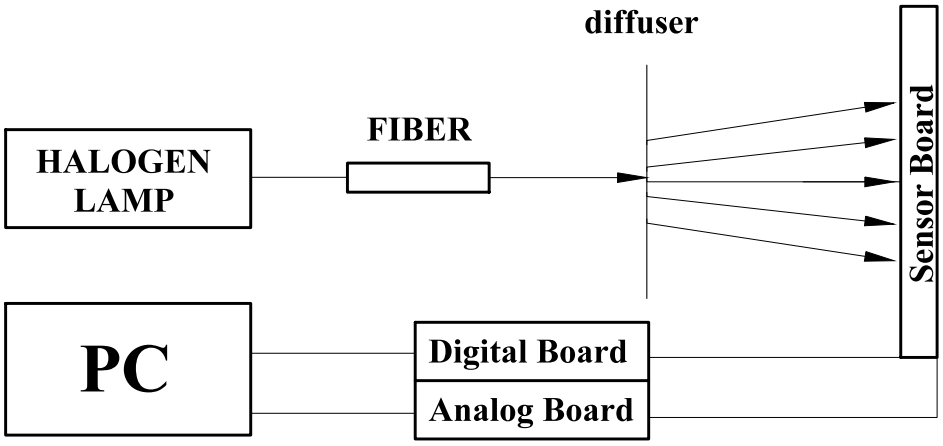

Figure 4.8: Test setup used for counter characterization measurements

A histogram of the output voltage calculated at 1 million of acquisitions has been acquired from each pixel. An example of a histogram of a single pixel is represented in Figure 4.9. Each peak of the histogram represents a number of detected photons. The right-most peak position is equal to the reset value, which includes the cases when after integration time no photons have been detected. The second peak corresponds to one photon detected and each additional peak represents an additional detected photon.

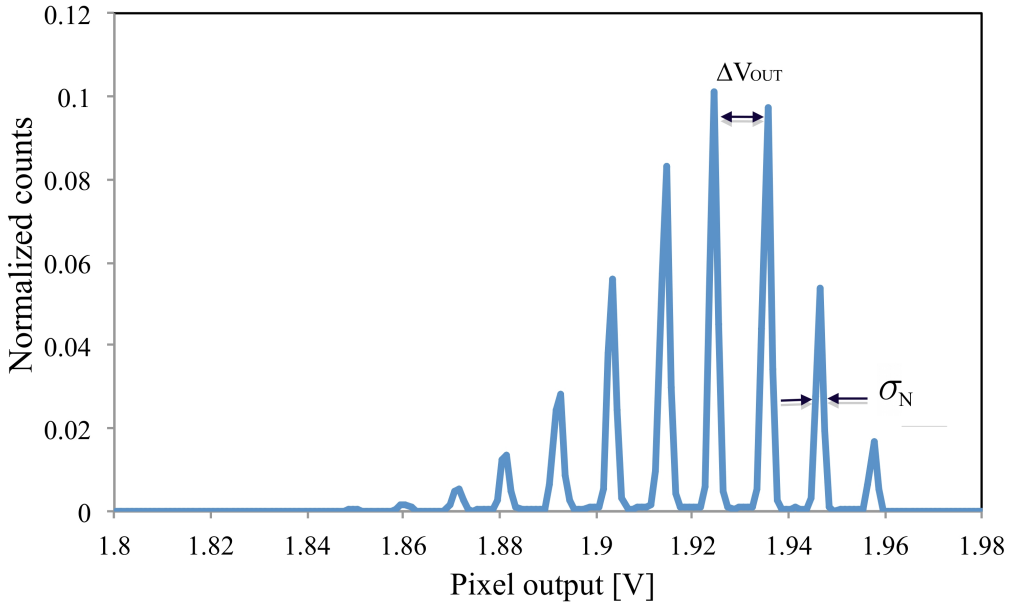

Figure 4.9: Pixel output voltage histogram

From the output voltage histogram the step size ΔV_{OUT} can be extracted for each pixel. The standard deviation of ΔV_{OUT} is related to pixel electronic noise. If the histogram covers the entire dynamic range, statistics on integral (INL) and differential (DNL) non-linearities can be extracted. INL was calculated as the deviation from the pixel output voltage to a linear fitting line. DNL represents the maximum deviation of an actual analog output step from the average step value calculated from the fitting line.

In order to ensure a high dynamic range, the step size should be set as small as possible. On another hand, the peak width, i.e. electronic noise, affects the minimum detectable step size. The standard deviation of each peak for each pixel can be estimated from the histogram assuming that the peaks follow a Gaussian distribution. Electronic noise is composed of a constant term, representing pixel readout noise, and a term proportional to the number of counts N:

$$\sigma_N = \sqrt{\sigma_0^2 + N\sigma_P^2} \tag{4.1}$$

where σ_N is the noise at N counts, σ_0 is the reset noise calculated at 0 counts, and σ_P is the noise introduced by each count.

The mismatch bentween transistors and capacitors in the counter circuits causes a non-uniformity of the average output voltage step delivered by different pixels. The non-uniformity of the output voltage step was extracted analyzing the output histograms of all the pixels in an array.

4.3.2 Pixel optical characterization

The pixel optical characterization has been carried out to measure the pixel overall response in the presence of light with variable intensities. The setup is shown in Figure 4.10

The pixel output signal was measured as a function of incident light power. The same wide-spectrum lamp used for counter characterization was used here. In these measurements a set of neutral-density filters (an optical filter wheel) were used to ensure a wide range of light intensities. The optical power density was measured with an optical power meter.

This setup was used to measure both pixel output signal and noise as a function of incident light intensity. In addition, Photo Response Non-Uniformity (PRNU) could also be characterized by analyzing the response of different pixels. In this measurement it is highly important to sup-

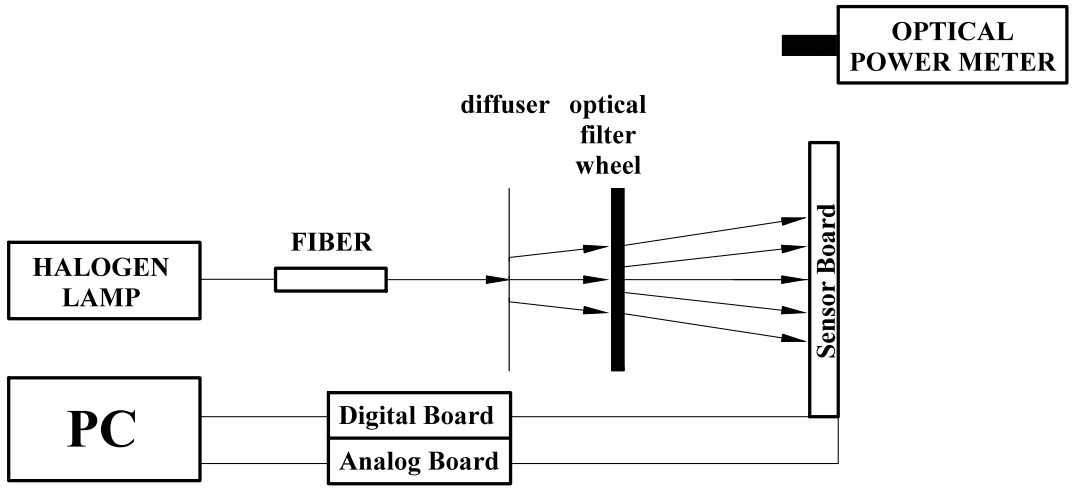

Figure 4.10: Test setup used for pixel optical characterization

press the non-uniformity of the light source. Therefore, special attention is needed to create a uniform illumination that was obtained by meeting the following conditions:

- large distance between the light source and the sensor, ensuring that the light intensity is sufficient to cover the whole dynamic range of the sensor.

- use of a diffuser in front of the image sensor.

4.3.3 Time-gated operation

An analysis of the pixels in time-gated operation was conducted in order to extract the minimum observation window that could be obtained. The measurement setup used for time-gated measurements is shown in Figure 4.11.

In this measurement campaign, a picosecond pulsed laser (Picoquant, $\lambda = 470$nm, pulse width 70ps FWHM) was used. The sensor was exposed to the laser emission through a diffuser. A pulse generator (HP8110) was

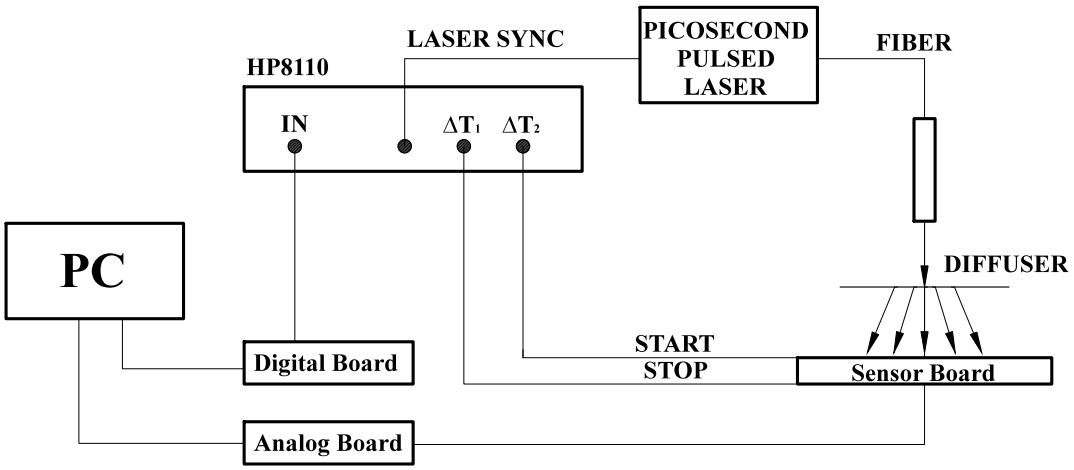

Figure 4.11: Test setup used for time-gated measurements

exploited to trigger the laser at 50 MHz repetition rate. The same instrument was used to generate START and STOP signals with different time delays $\Delta T1$ and $\Delta T2$. In this way, an observation window with programmable width $W = \Delta T_1 - \Delta T_2$ was obtained. The timing diagram of the signals used to generate the window is shown in Figure 4.12.

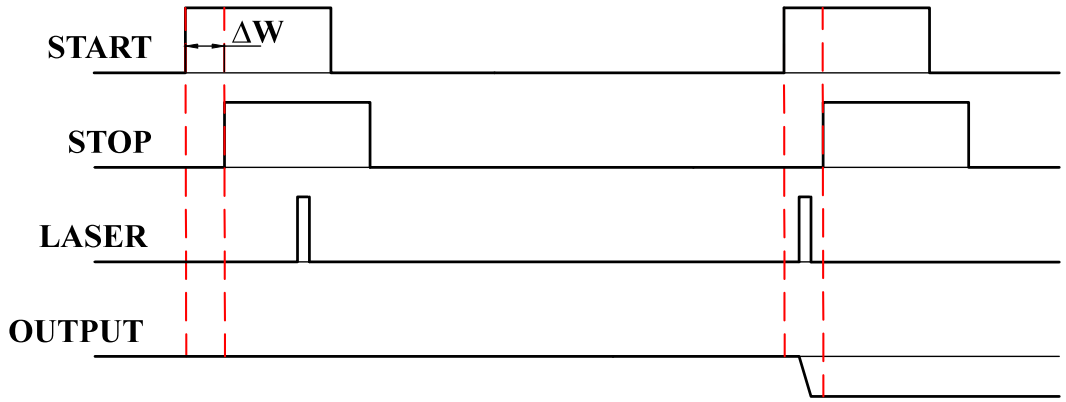

Figure 4.12: Timing diagram of the signals for time-gated measurements

Chapter 5

Experimental results

This chapter covers experimental results obtained on the different test arrays of pixels. The main target of the characterization was the validation of the proposed pixels designs and their comparison. If their performance were demonstrated to be comparable with the digital standard implementation, analog counting circuits would improve spatial resolution of sensors.

Experimental results on counter characterization are presented in this chapter.

5.1 Circuit I.

This section presents the experimental characterization of Circuit I, which was also published in [150].

Circuit I, whose design is discussed in section 3.1, was implemented in a 20×20 array and fabricated in a standard 0.35 μm CMOS technology. An input signal emulating SPAD ignitions was externally provided through by digital board.

5.1.1 Reference voltage dependence

An experimental characterization was carried out in order to evaluate the circuit performance. All the measurements presented hereafter were conducted on all the analog counters in the array. The mean output voltage step of the array is dependent on the different reference values of V_{REF1} and V_{REF2} and displayed in Figure 5.1. During the measurement, the ref-

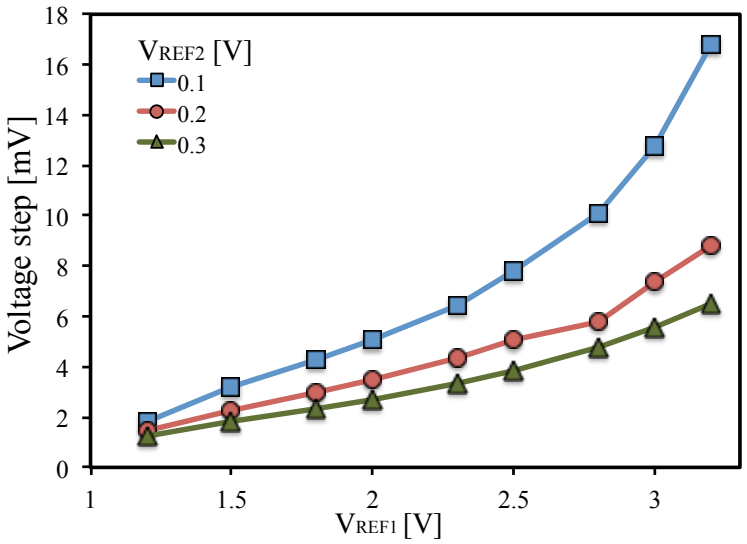

Figure 5.1: Output voltage step as a function of V_{REF1} and V_{REF2}

erence voltage V_{REF1} was varied from 1.2 to 3.2 V and V_{REF2} was varied from 0.1 to 0.3 V. The experimental value of parasitic capacitance C_P is estimated to be 0.8 fF, lower than the preliminary simulation results, as in the actual layout implementation the source diffusion of M_4 was shared with the drain diffusion of M_5. This estimated value is in good agreement with the post-layout simulations.

From Figure 5.1 the average voltage output step shows a linear dependency only for values of V_{REF1} lower than 2.6 V while a non-linearity appears for higher values. For a better explanation of this behavior, an analysis of the circuit depicted in Figure 3.1 during the falling edge of

node IN has been performed. During this transient the delay introduced by inverter $X2$ keeps transistor M_4 on for a short time before M_3 is closed and M_5 is opened, causing a direct current path from node D to V_{REF2}. This extra charge packet causes a non-linear increase of the voltage step of the counter with V_{REF1}. In a first approximation, the error introduced during this transient depends on the width of the temporal interval ΔT in which M_5 starts conducting and M_4 is still open. A possible way to reduce ΔT, as shown in Figure 5.1, is to increase V_{REF2} delaying the opening of M_5, or decrease V_{REF1}, turning off M_4 earlier.

A secondary effect of this current is also the discharge of parasitic capacitance at node B towards V_{REF2}. As a result, an additional charge packet, caused by the charge sharing between the node B and the output, is introduced into equation 3.1, turning into a voltage step modification.

The reference voltages V_{REF1} and V_{REF2} also affect the voltage step non-uniformity, measured as the standard deviation of ΔV_D over the whole array (see Figure 5.2). As it is seen in the graph, the measurements show a non-uniformity below 4% for V_{REF1} ranging from 1.5 to 3 V and V_{REF2} voltages exceeding 0.2 V.

The main advantage of the proposed circuit is its low output non-uniformity by comparison with the implementation in [143, 144]. These two circuits are based on completely different principles. The proposed approach is based on charge transfer between two capacitances. As it follows from equation 3.2, the step non-uniformity is mostly caused by the mismatches of capacitances C_P and C_{M6} and the threshold voltage of transistor M_4. In order to minimize the overall mismatch, the value of C_{M6} was chosen as large as possible, taking into consideration the available area. In the previous work [143, 144] the SPAD pulse is shortened before feeding a resistive switch in its core. The non-uniformity was then caused not only by threshold voltage mismatches, but also by the shortened pulse

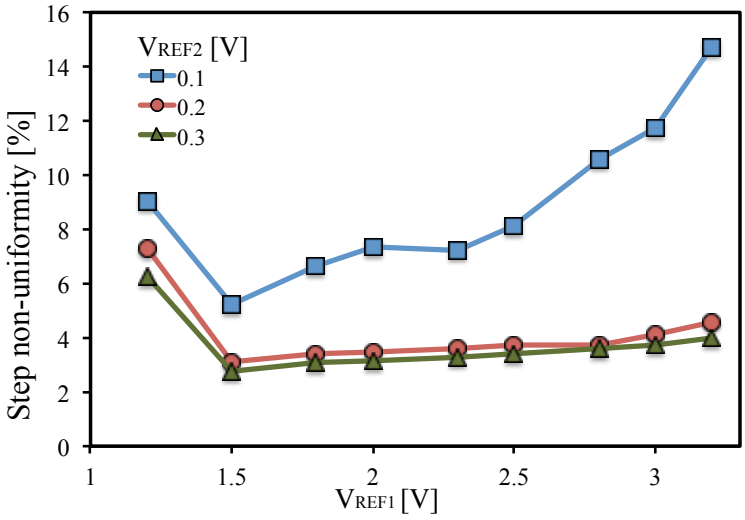

Figure 5.2: Voltage step non-uniformity in dependence on reference voltages V_{REF1} and V_{REF2}

width non-uniformity.

It should be noted that the storage capacitor C_{M6} might discharge with time by leakage currents. In order to estimate the impact of a possible leakage, the array was read out after an integration time of a few tens of milliseconds in dark conditions (i.e., with no pulses applied), and only a slight change in the output voltage (lower than 1 mV) was observed. This effect might be neglected as the circuit is expected to operate in low light level conditions in real time (20 frames per second).

The readout output noise of each counter has also been measured at room temperature. Across the whole reference voltages range the noise does not exceed s=1.2 mV. This value is in good agreement with expectations and determines the minimum voltage step for shot-noise limited operation.

The circuit power consumption estimation was carried out at 1 MHz repetition rate of the input signal and power supply voltage V_{DD}=3.3 V. A power consumption of 190 nW was measured for each pixel.

5.1.2 Non-linearity estimation

One of the advantages of the present circuit is its programmable resolution that can be adjusted accordingly to the application demands.

The circuit provides a programmable resolution that can be tuned precisely for application requirements. Two sets of reference voltage values were identified providing a number of steps at the output corresponding to 7- and 8-bit resolution. Taking into account the step size (Figure 5.1) and step non-uniformity (Figure 5.2) results, two sets of reference voltages were chosen (Table 5.1):

	Ref.voltages values, V		Step Size	Step Non-uniformity,%	$\sigma_{\bar{e}}$
Set 1	V_{REF1}	2.0	4.1	≈ 3.8	0.3
	V_{REF2}	0.15			
Set 2	V_{REF1}	3.1	8.1	≈ 4.2	0.15
	V_{REF2}	0.2			

Table 5.1: Circuit I characteristics

As a figure of merit for the single-event discrimination capability of the circuit, we can use the ratio between the readout noise to the step size and refer to it as an equivalent noise in electrons. (Equation 5.1)

$$\sigma[\bar{e}] = \frac{\sigma_0}{\Delta V}, \tag{5.1}$$

where σ_0 — electronic noise of the circuit, ΔV — voltage step size, $\sigma[\bar{e}]$ — electronic noise of the circuit expressed in electrons.

Thus, the readout noise for a single voltage step is 0.15 and 0.3 electrons for the two sets, respectively. The expected non-linearity for the both setting is approximately 4%. A characterization of the output voltage linearity was carried out on all the analog counters. The output voltage values of each counter in the array were acquired for all the possible

numbers of input pulses spanning the ranges 0-128 and from 0 to 256 to assure 7 and 8-bit resolution settings, respectively. From these data, integral (INL) and differential (DNL) non-linearity were extracted. The envelope of INL and DNL curves for all the pixels for 8-bit resolution setting are depicted in Figures 5.3. INL slightly exceeds ±1 LSB error, DNL is in order of ±0.6 LSB error.

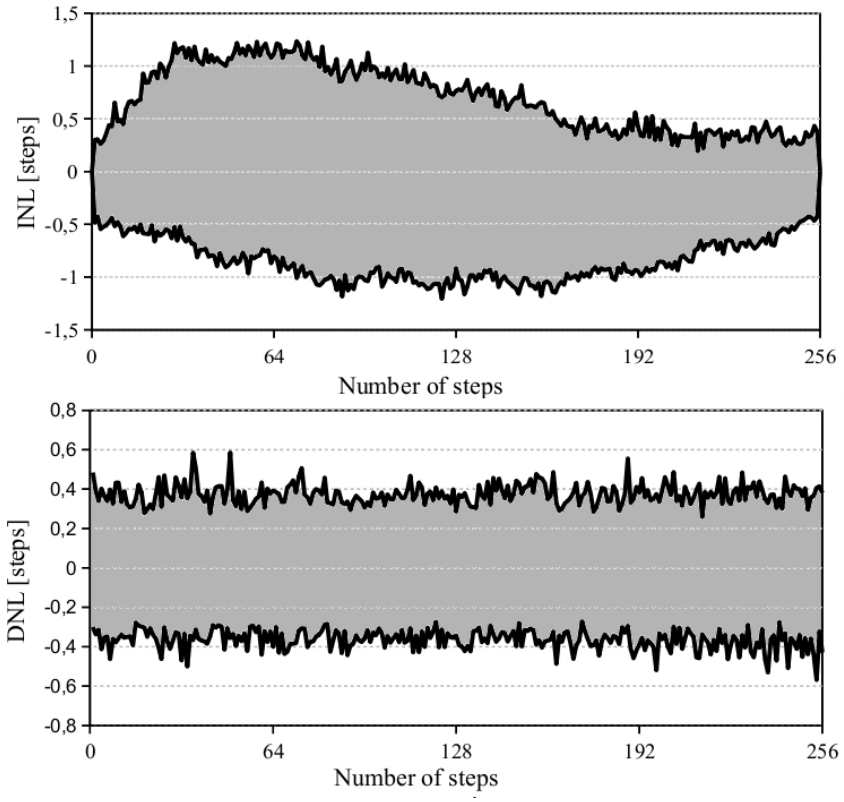

Figure 5.3: Integral (INL) and differential (DNL) non-linearity for 8-bit resolution (Set 1)

Figures 5.4 shows the INL and DNL envelopes for 7-bit resolution setting. For 7-bit the INL remains within ±0.6 LSB range. At the same time, DNL is considerably smaller than ±1 LSB error, its values are within ±0.3 LSB.

Generally speaking, a DNL value greater than 0.5 LSB would not be acceptable in a Digital-to-Analog Converter. Despite this fact, a DNL value

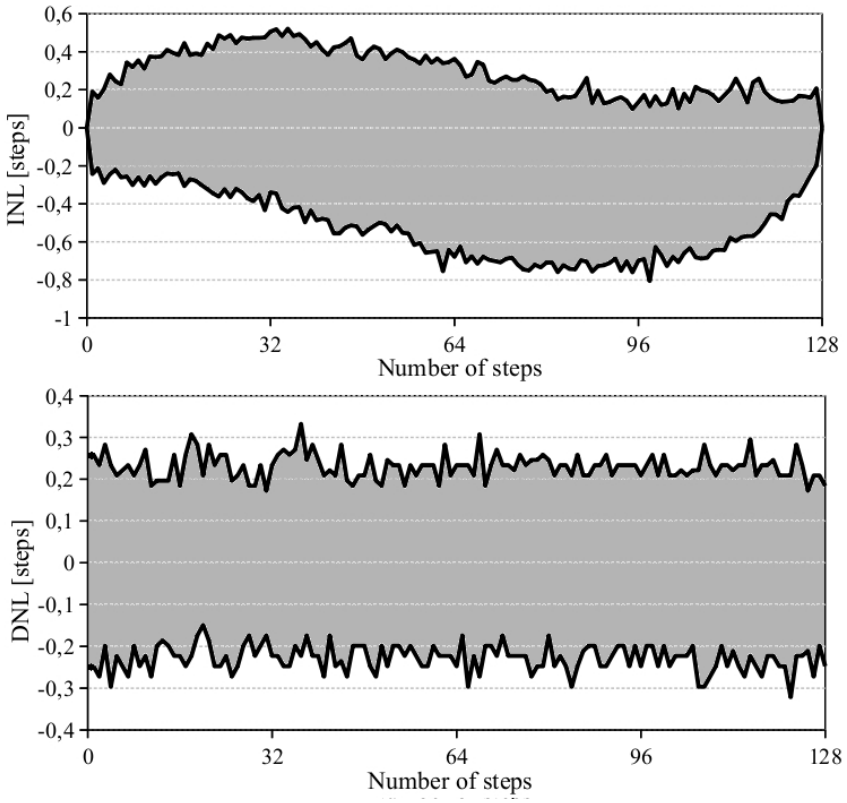

Figure 5.4: Integral (INL) and differential (DNL) non-linearity for 7-bit resolution (Set 2)

of 0.6 LSB can still be suitable for such application, where the uncertainty of the shot noise related to photon counting is typically larger than 1 LSB. Moreover, Figure 5.3 shows that there are only a few occurrences in the whole array with a DNL higher than 0.5 LSB, so that only a very limited number of codes might be missed. Hence, 8-bit resolution ensures higher dynamic range, while 7-bit resolution might be used in such applications where good uniformity and sensitivity are more important features.

5.1.3 Period and pulse width dependence

The output voltage step can be affected by the frequency of the SPAD pulse events. In order to estimate this influence, the frequency of the IN signal was changed from 1 to 500 kHz while keeping a constant pulse width

of 200 ns. The reference voltages were set to the values providing 7- and 8-bit resolution. The mean step size, calculated as an average on the whole array of analog counters, is shown in Figure 5.5 as a function of pulse period. Over the whole time range the step size increases by approximately 6.3% for 7-bit resolution setting and 7.6% for 8-bit resolution setting. The observed increase in step size values at high pulse period values could be explained by a leakage current of transistor M_4. SPAD dead time typically

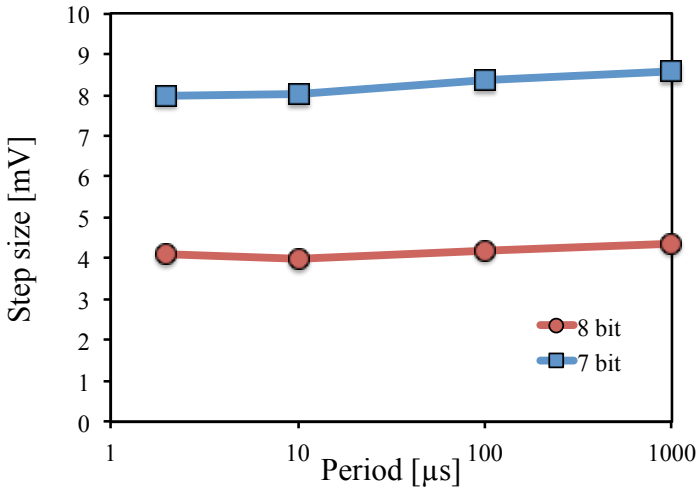

Figure 5.5: Output step size as a function of the pulse period

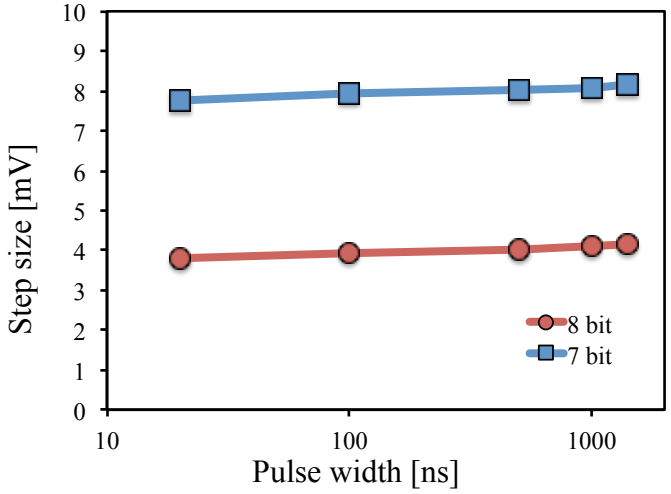

Figure 5.6: Output step size as a function of pulse width

lasts from a few tens to a few hundreds of nanoseconds. Thus, the impact

of the pulse width upon the voltage step has been also estimated. The measurement was performed with different values of pulse width between 20 ns to 1200 ns while keeping a constant pulse period of 2 μs.

The reference voltages were set as in the previous case, to obtain 7 and 8-bit resolution. Figure 5.6 shows a mean value increase by approximately 4.9% for 7-bit and 9.4% for 8-bit resolution. In this case the voltage step size increases because the charge transfer is affected by sub-threshold operation of transistor M_4.

5.2 Circuit II.

This section presents the characterization results of the resistive-switch pixel, which was described in section 3.2. The analog counter circuit has been fabricated in two configurations with different length for transistor M_{10} in order to estimate the influence of transistor size on the pixel non-uniformity. The area occupied by the circuit is slightly larger with respect to the previous implementation in 0.35 μm process [143, 144] (238 μm^2 versus 200 μm^2).

5.2.1 Counter characterization

A first experimental campaign was performed to measure the electrical characteristics of the counter, independently from the features of the SPAD. Since an electrical test input was not included in the pixels, the SPAD itself was used to stimulate the counter. For this reason the arrays have been exposed to a light of tunable intensity and reference voltage V_B was varied in order to obtain a voltage step in the range 5...50 mV. Values of V_B and resulting output voltage steps are displayed in Table 5.2.

During the measurements the window signal WIN was maintained in low state so that all the impinging photons could be detected. An example of pixel circuit output signal has been acquired with oscilloscope. The output trace is presented in Figure 5.7. The initial voltage corresponds to the reset value V_{RST}. With each pulse coming from SPAD it can be observed a voltage step in the output (determined by the length of transistor M_4 and bias voltage V_B).

A histogram of the output voltage calculated at 1 million of acquisitions has been acquired for each pixel. The light conditions were varied from a low light intensity level (a few photons) to the detector saturation. A short integration time was used to reduce count non-uniformity

Transistor M_{10} Dimensions	Reference voltage V_B	Output Step Size
W=0.8 μm, L=4 μm	1.51 V	5.33 mV
	1.68 V	10.27 mV
	1.80 V	16.3 mV
	2.0 V	29.99 mV
	2.28 V	48.95 mV
W=0.8 μm, L=7.2 μm	1.68 V	4.79 mV
	1.88 V	9.45 mV
	1.98 V	12.75 mV
	2.32 V	28.9 mV
	2.79 V	58.42 mV

Table 5.2: Dimensions of the MOS transistors in Circuit II

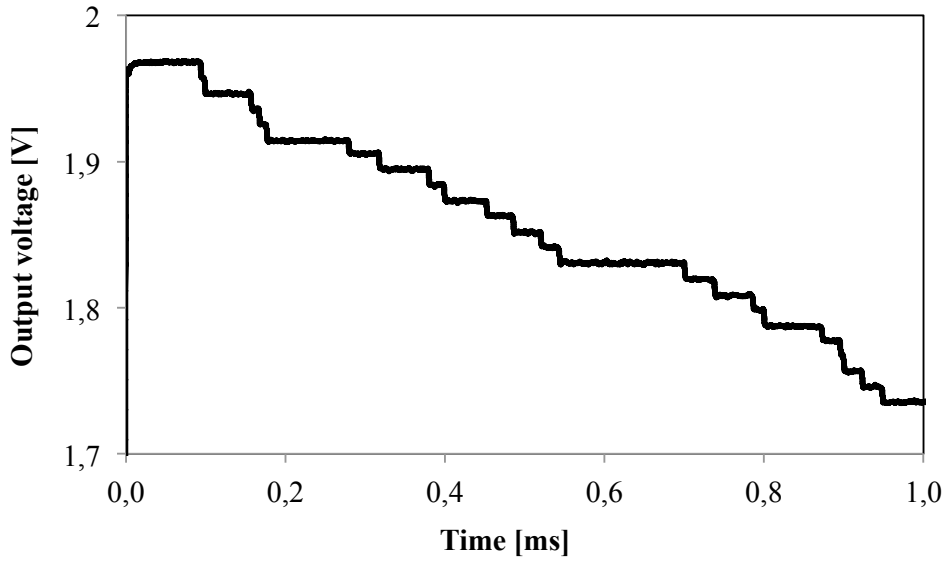

Figure 5.7: Oscilloscope trace of pixel output: each voltage step represents a detected photon

due to the distribution of Dark Count Rates. A great advantage of this circuit is its output programmability. The step size was adjusted by varying reference voltage V_B. The step was set at values close to 5, 15, 30 and 50 mV, and circuit electronic noise and non-linearity were evaluated at the different settings. Figure 5.8 shows a histogram of a single pixel. In this

example, the distance between two peaks, and therefore the step size, is close to 10mV. The peaks positions in the histogram were calculated for

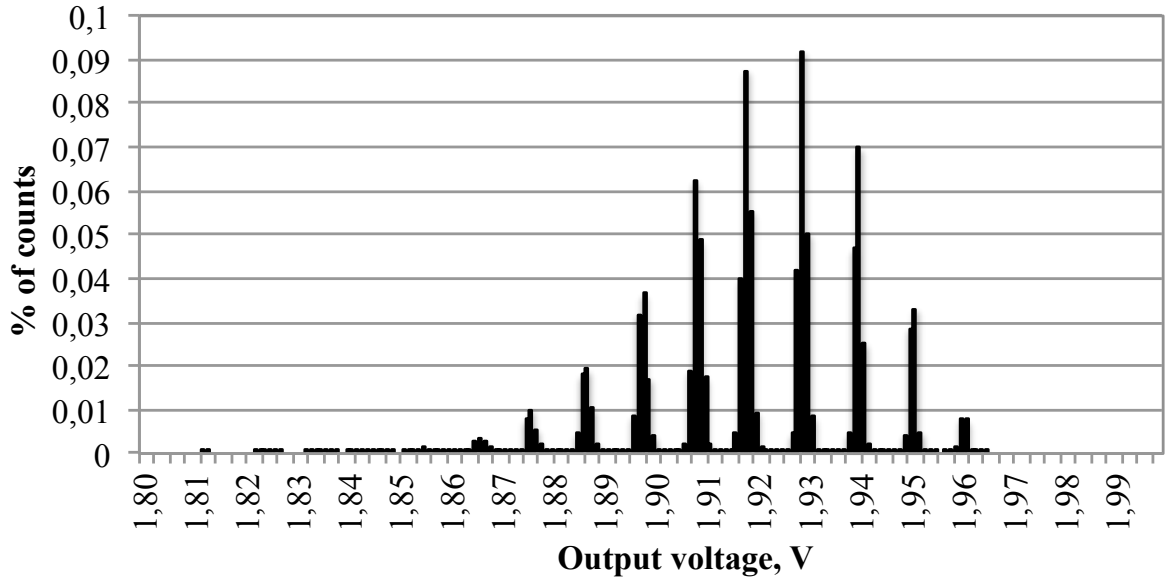

Figure 5.8: Pixel output voltage histogram

each pixel. Figure 5.9 and Figure 5.10 show the average peak position as a function of number of counts at three different settings for V_B.

The width of each peak is related to the electronic noise. The standard deviation of each peak has been extracted for each pixel. Figure 5.11 and Figure 5.12 show the average standard deviation as a function of pixel count for two different sizes of transistor M_{10}. Electronic noise increases with the number of counts due to the additional noise introduced by each count described in Equation 4.1

The reset noise is the same for both configurations of Circuit II. As it can be observed in the graphs, a smaller noise contribution is related to a smaller step. At high count numbers, a smaller noise is present in the second circuit configuration having a longer channel of transistor M_{10}.

In Figure 5.13 a comparison between simulated and experimental output voltage step as a function of reference voltage V_B is presented. The

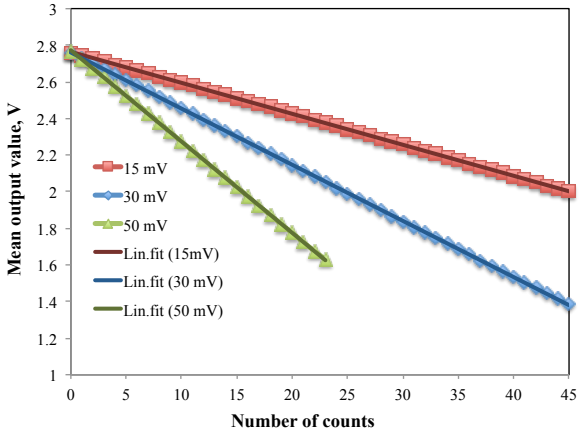

Figure 5.9: Average pixel output voltage as a function of pixel counts for transistor M_{10} (W=0.8 μm, L=4.0 μm). Data relevant to three values of reference voltage V_B are compared

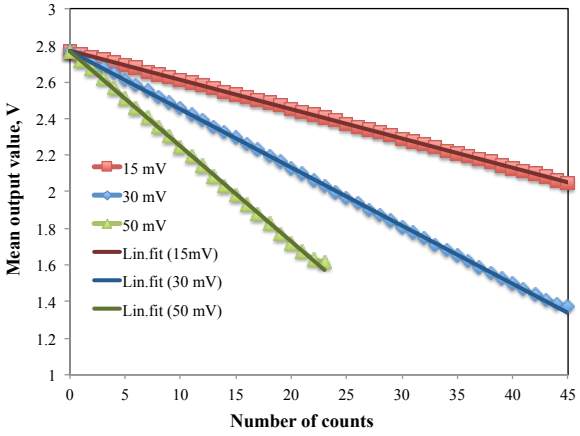

Figure 5.10: Average pixel output voltage as a function of pixel counts for transistor M_{10} (W=0.8 μm, L=7.2 μm). Data relevant to three values of reference voltage V_B are compared

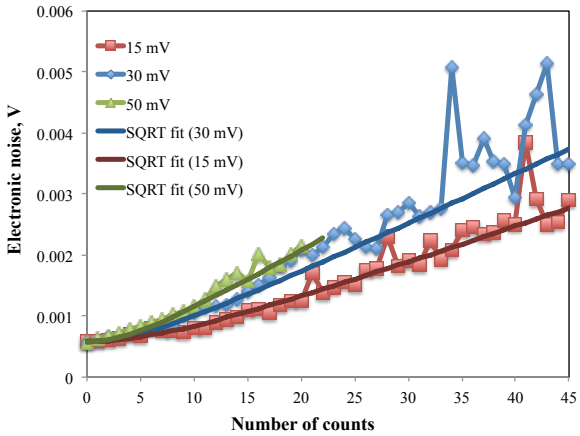

Figure 5.11: Histogram peak standard deviation as a function of pixel counts, for two different sizes of transistor M_{10}: (W=0.8 μm, L=4.0 μm). Data acquired with three values of reference voltage V_B

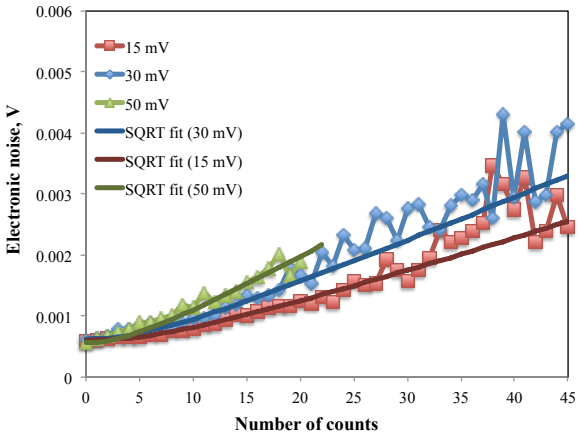

Figure 5.12: Histogram peak standard deviation as a function of pixel counts, for two different sizes of transistor M_{10}: (W=0.8 μm, L=7.2 μm). Data acquired with three values of reference voltage V_B

measurements are in good agreement with the simulations.

The step linearity and non-uniformity among the pixels in the array were calculated from the experimental data. A comparison between

the simulated and experimental output voltage step non-uniformity as a function of reference voltage V_B is presented in Figure 5.14.

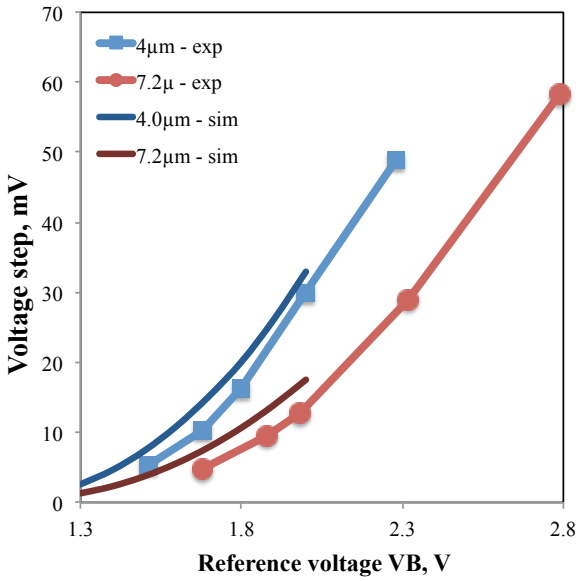

Figure 5.13: Experimental and simulated average pixel output voltage as a function of reference voltage V_B for both configurations of transistor M_{10}

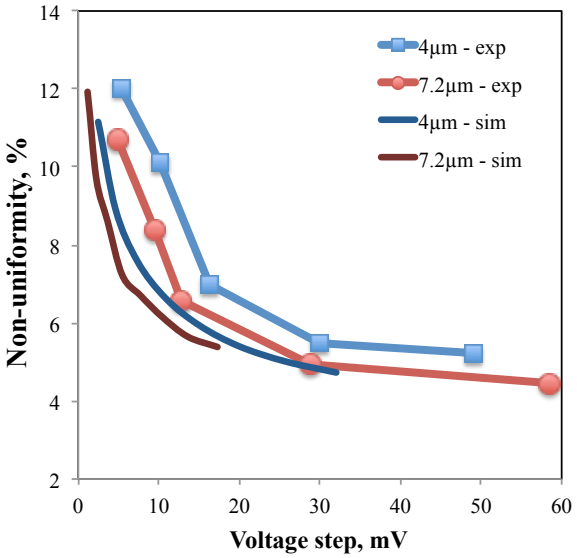

Figure 5.14: Experimental and simulated average pixel non-uniformity as a function of output voltage step for both configurations of transistor M_{10}

A summary of the characterization results is presented in Table 5.3. The pixels with longer transistor M_{10} gate have shown a 10% improvement of the pixel non-uniformity. However, transistor M_{10} is approximately two times larger. Non-uniformity is also dependent on the set step size and is larger at smaller step values. The number of steps used for the counter characterization does not represent the maximum output range, but the number of steps that could be easily discriminated without any additional calibration of the gaussian distribution calculation. Due to the additional noise contributed with each count, at higher number of counts the "finger" in the pixel output histogram (Figure 5.8) can have a few peaks. This effect should be further taken into account in the signal processing.

Transistor M_{10} Dimensions	Step Size	N. steps	σ_0	σ_P	Pixel Non-uniformity	INL
W=0.8 μm; L=4.0 μm	5.33 mV	35	0.620 mV	0.054 mV	11.8%	3.55%
	10.27 mV	40	0.612 mV	0.062 mV	10.1%	3.39%
	16.30 mV	45	0.578 mV	0.066 mV	6.96%	3.16%
	29.99 mV	45	0.583 mV	0.094 mV	5.47%	2.73%
	48.95 mV	25	0.589 mV	0.078 mV	5.23%	2.58%
W=0.8 μm; L=7.2 μm	4.79 mV	35	0.721 mV	0.025 mV	10.7%	3.61%
	9.452 mV	45	0.721 mV	0.027 mV	8.4%	3.41%
	12.75 mV	50	0.633 mV	0.045 mV	5.96%	3.15%
	28.92 mV	45	0.596 mV	0.067 mV	4.86%	2.77%
	58.42 mV	20	0.623 mV	0.076 mV	4.37%	2.69%

Table 5.3: Circuit II characteristics. V_{RST} is set to 3.0 V

At high values of V_{RST} in range of 3...3.3 V, an effect of non-linearity of the first steps have been observed. In these conditions, voltage of SELECT switch V_{DD}=3.3 V is not high enough, thus, the transistor works in sub-threshold regime. This effect reduces the size of the first few steps. The output voltage step for a few pixels with L_{M10}=7.2μm and with V_{RST} set to 3.3 V is shown in Figure 5.15. The linearity of the circuit can be further improved by decreasing reference voltage V_{RST}. Figure 5.16 shows the output voltage step of the same pixels when measured with a reset voltage V_{RST}=2.7 V.

Preliminary experimental results for V_{RST} set to 2.7 V are presented in Table 5.4. A remarkable linearity of 1.1% can be achieved at the price of a narrower dynamic range.

Integral and differential non-linearities of the counters have also been calculated. Figure 5.17 presents INL and DNL calculated over 45 steps at

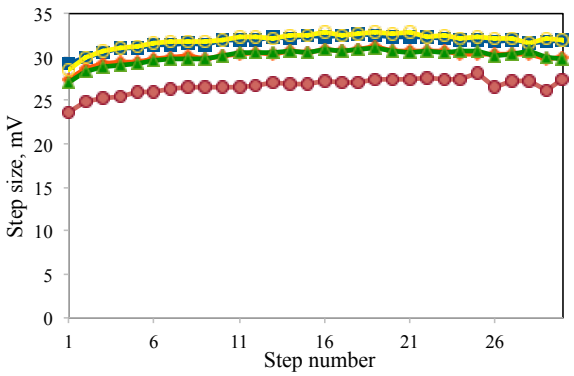

Figure 5.15: Pixel step size as a function of the number of counts. Configuration with transistor M_{10} (W=0.8 μm; L=7.2 μm) and V_{RST}=3.0 V

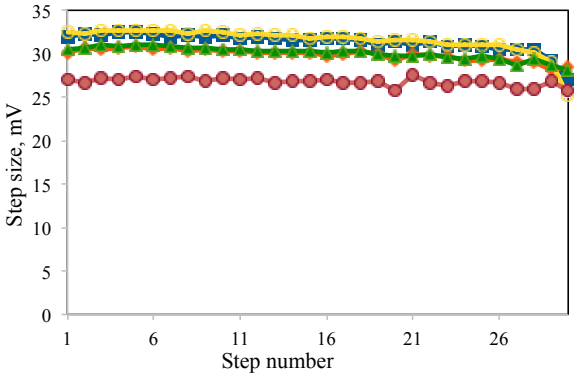

Figure 5.16: Pixel step size as a function of the number of counts. Configuration with transistor M_{10} (W=0.8 μm; L=7.2 μm) and V_{RST}=2.7 V

Transistor M_{10} Dimensions	Step Size	N.steps	σ_0	σ_P	Pixel Non-uniformity	INL
W=0.8 μm; L=4.0 μm	4.48 mV	30	0.711 mV	0.025 mV	12.06%	1.4%
	9.96 mV	10	0.694 mV	0.048 mV	10.10%	1.14%
W=0.8 μm; L=7.2 μm	4.629 mV	30	0.720 mV	0.039 mV	10.7%	1.39%
	9.45 mV	10	0.711 mV	0.026 mV	8.66%	1.23%

Table 5.4: Circuit II characteristics at V_{RST} set to 2.7 V. Configuration with transistor M_{10} (W=0.8 μm; L=7.2 μm)

15 mV step size. INL does not exceed ± 0.5 LSB for both structures. DNL is lower than ±0.1 for both pixels for the output range. The higher values of INL and DNL are explained by non-linearities of the first steps at high values of V_{RST}.

The pixel current consumption has been simulated to be 280 nA at 100 kHz repetition rate.

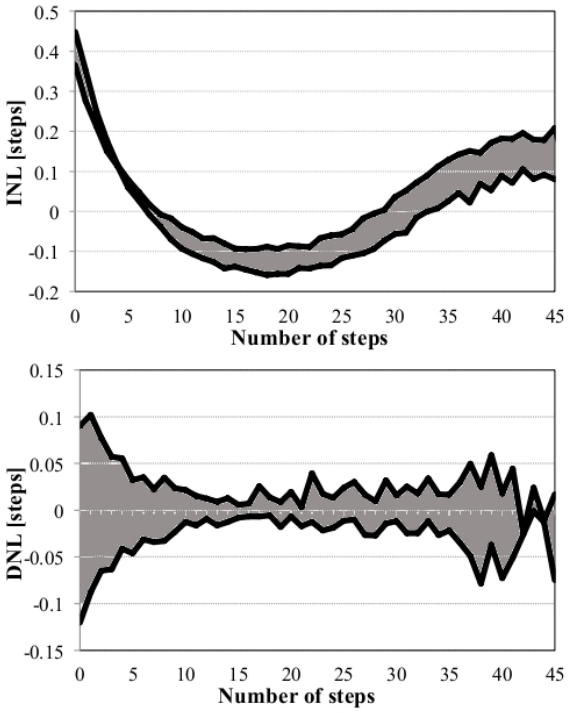

Figure 5.17: INL and DNL of the circuit at 15 mV step size. Configuration with transistor M_{10} (W=0.8 μm; L=4.0 μm). V_{RST}=3 V

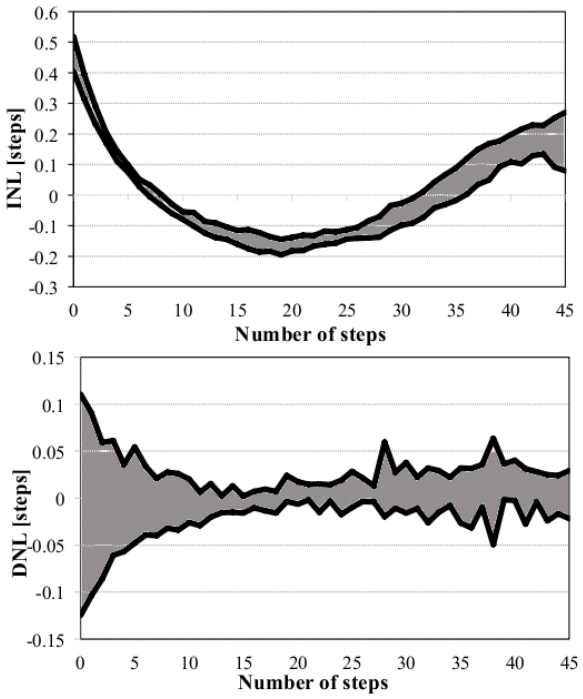

Figure 5.18: INL and DNL at 15 mV step size. Configuration with transistor M_{10} (W=0.8 μm; L=7.2 μm). V_{RST}=3 V

5.2.2 Pixel optical characterization

Pixel output characteristics have been measured as a function of incident light power. In the measurements the chip was illuminated with a wide spectrum halogen lamp. Light intensity was varied using a set of neutral-density filters. In order to measure the optical power density a calibrated photodiode was used. Figure 5.19 and Figure 5.20 depict the pixel output voltage signal and noise as a function of incident optical power density for the first and the second pixel structure, respectively.

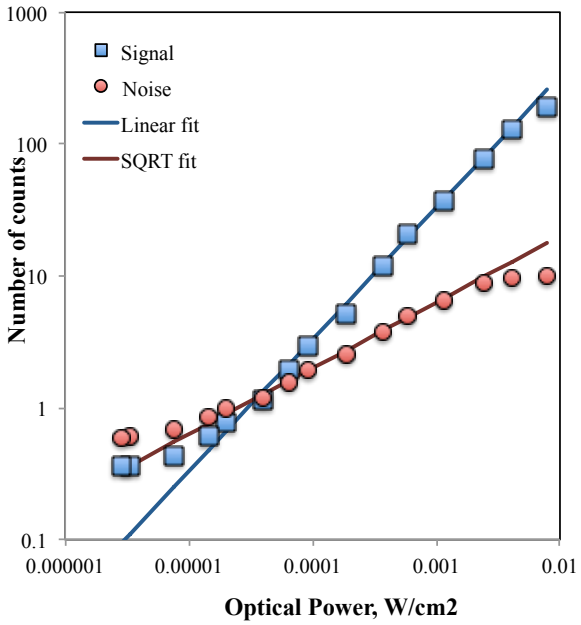

Figure 5.19: Pixel output signal and noise as a function of optical power density. Configuration with transistor M_{10} (W=0.8 μm; 4.0 μm)

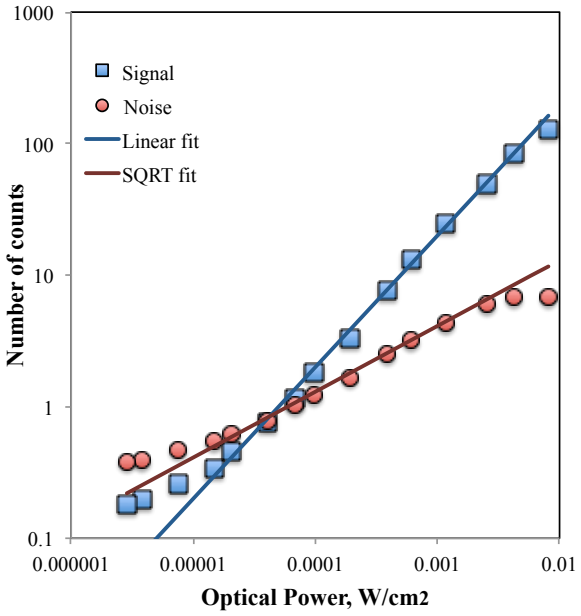

Figure 5.20: Pixel output signal and noise as a function of optical power density. Configuration with transistor M_{10} (W=0.8 μm; L=7.2 μm)

The integration time was set to 10 μs. The output signal is linearly proportional to the incident power until the upper bound of the dynamic range is reached. The noise is proportional to the square root of the optical power. This behavior proves shot-noise limited operation of the pixel. In Figure 5.21 and 5.22, these two curves cross at a voltage value of 15 mV,

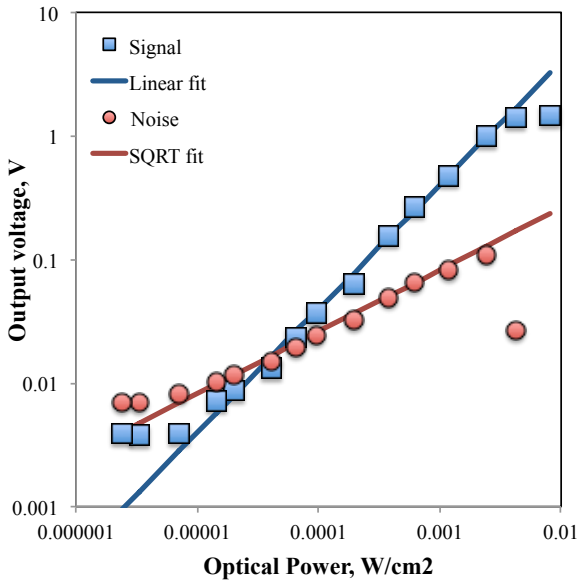

Figure 5.21: Pixel output signal and noise in voltage as a function of optical power density. Configuration with transistor M_{10} (W=0.8 μm; 4.0 μm)

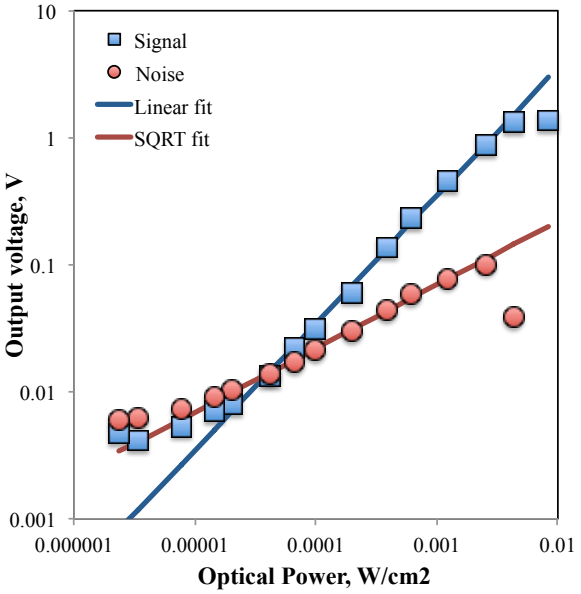

Figure 5.22: Pixel output signal and noise in voltage as a function of optical power density. Configuration with transistor M_{10} (W=0.8 μm; L=7.2 μm)

which for this pixel setting is the output voltage corresponding to the detection of one single photon.

5.2.3 Time-gated operation

A characterization of pixel output in time-gated operation was conducted using the setup described in Chapter 4. The average output voltage for two different gate widths as a function of time delay is presented in Figure 5.23, showing that a minimum gate width lower than 1ns can be obtained. The time window could be reduced to a minimum 0.9 ns. Below this value, the output signal level strongly decreases.

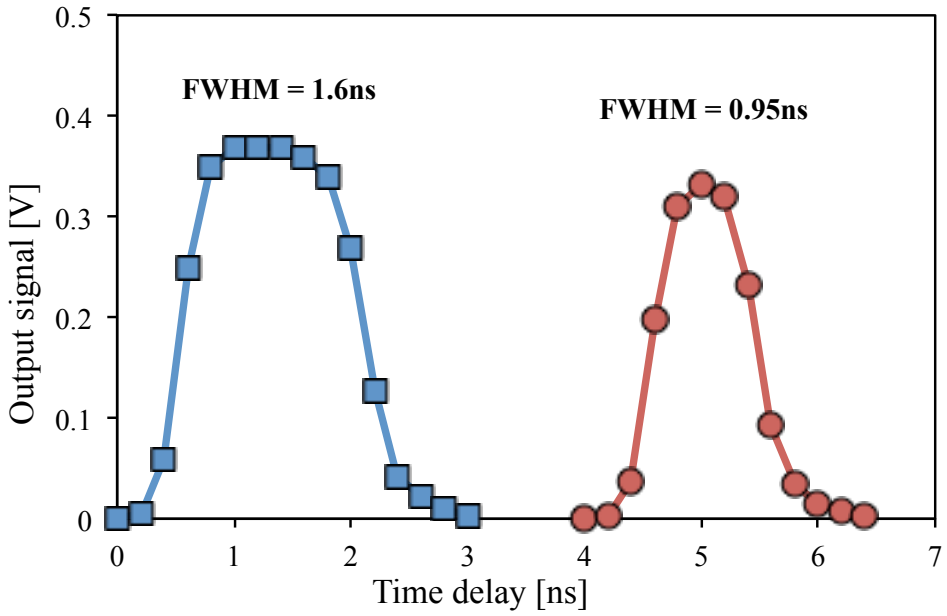

Figure 5.23: Average pixel output signal as a function of time delay for two different gate width settings

5.3 Circuit III

5.3.1 Pixel design and circuit configuration

Three linear arrays of pixels based on Circuit III were included in the test chip fabricated in 0.15 μm CMOS technology. The analog counter circuit has been fabricated in three different configurations with different sizes of storage MOS capacitor C_{M12}. The capacitor sizes included in the chip are shown in Table 5.5. The capacitor size affects the output step size and, therefore, the circuit dynamic range.

The area occupied by the circuit is 306 μm^2 and is the same for all three configurations.

5.3.2 Counter characterization

As was done for the other pixels, an experimental campaign was performed to measure the electrical characteristics of the counter. During the measurements, the pixels have been exposed to light with variable intensity and the observation window was kept always open, with signal WIN maintained in low state. The circuit output signal has been observed with oscilloscope and two output traces are shown in Figure 5.24. The initial voltage corresponds to the reset value V_{RST}. Each pulse coming from SPAD corresponds to a voltage step in the output voltage. Variability in the photons arrival times causes the difference between these two traces.

The output voltage as a function of number of counts is shown in Figure 5.25. As shown in the simulations discussed in 3.3.2, the amplitude of the following steps progressively reduces.

As for the pixels previously presented, a large number of acquisitions of the pixel output signals and its distribution analysis is used to evaluate the pixel performance. Thus, the histograms, one of a few of which are depicted in Figure 5.26, have been acquired for each pixel in the three

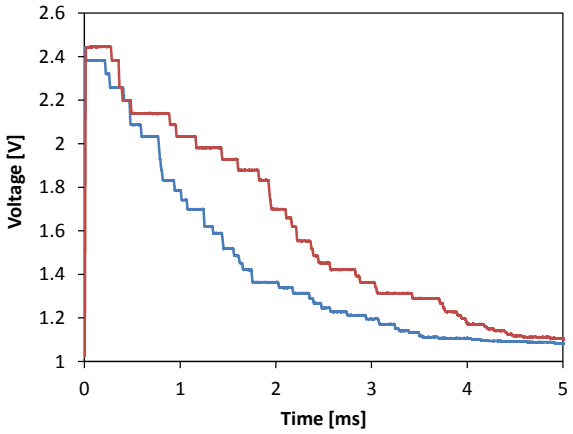

Figure 5.24: Pixel output oscilloscope traces

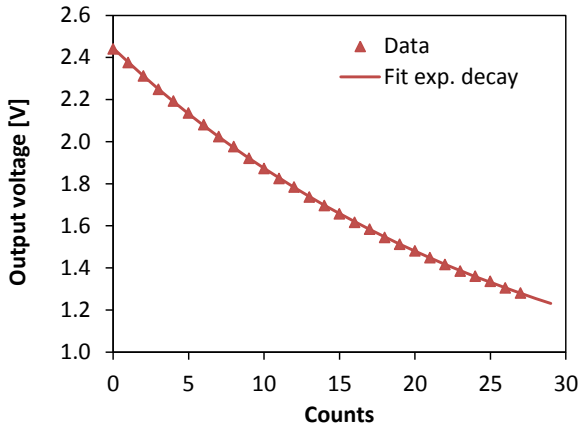

Figure 5.25: Circuit output as a function of count number

versions. The histogram acquisition was carried out under different light conditions in order to estimate the circuit dynamic range. Figure 5.26 shows that, the single photons can be easily discriminated for all three structures, as in all cases the peaks appear well separated.

The width of the histogram peaks is related to the electronic noise. Assuming a gaussian distribution for each peak, electronic noise at each photon detection event has been calculated. Figure 5.27 represents the circuit electronic noise at different voltage steps. This noise is lower than 1mV and approximately independent from the number of pixel counts for the

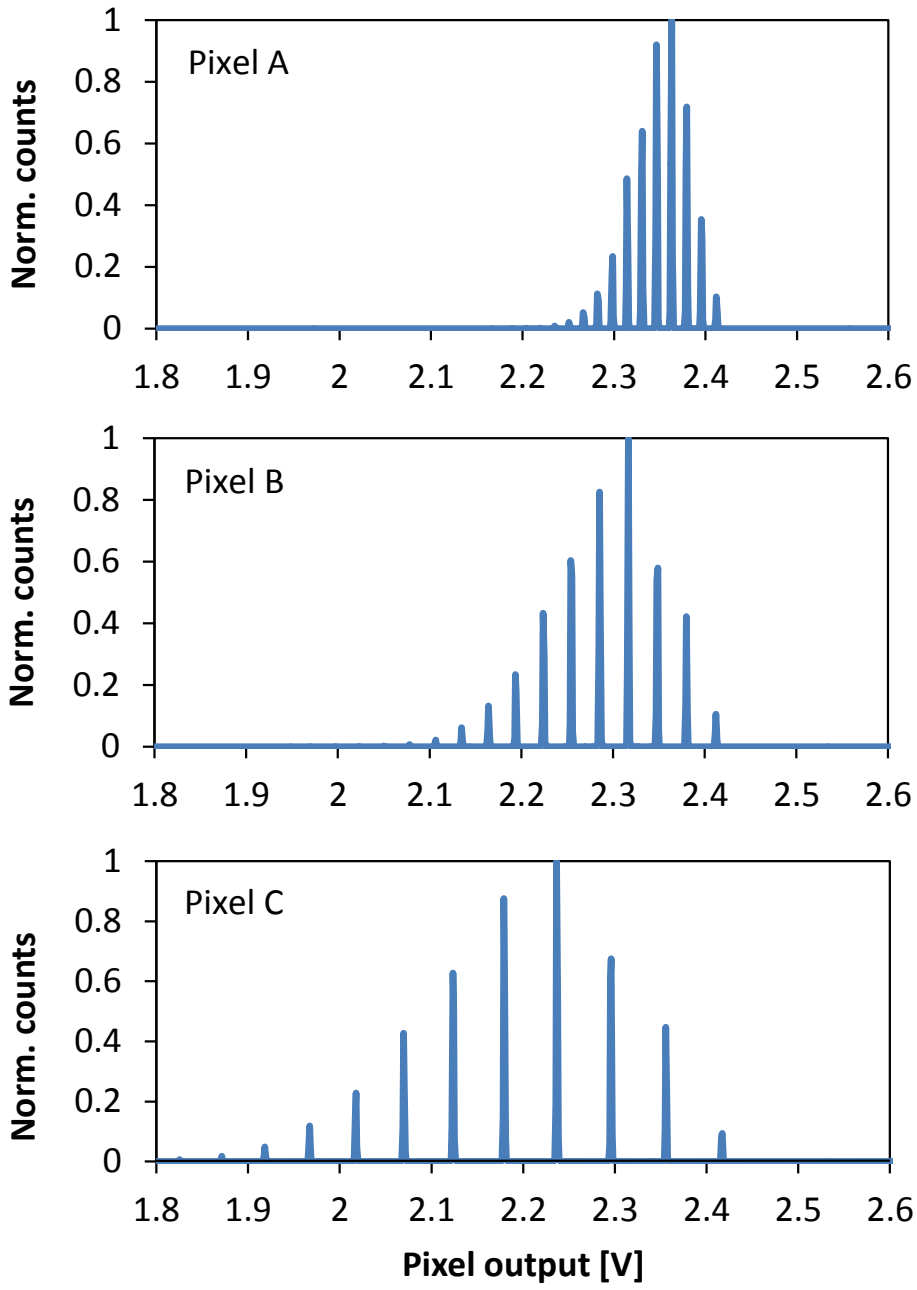

Figure 5.26: Output voltage histogram at low light intensity for the three different pixel structures

entire dynamic range. This means that the noise contribution introduced by the single steps is negligible.

Pixel step non-uniformities among pixels have been estimated and

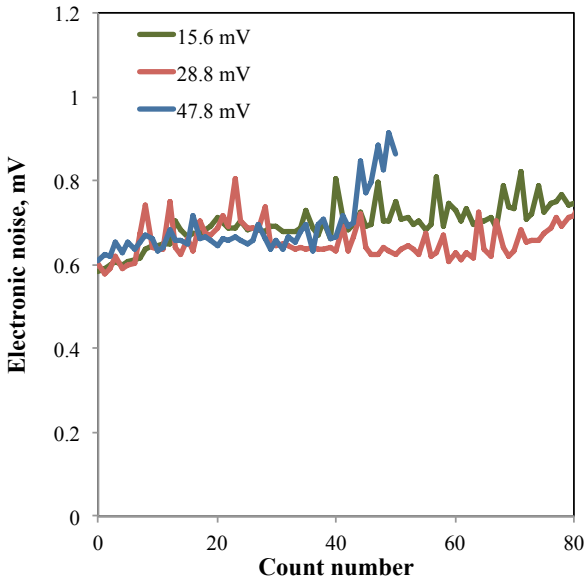

Figure 5.27: Electronic noise for the three different structures

C_{M10} Dimensions	Step Size	Pixel Non-uniformity	σ_0	σ_P
8×8 μm^2 (290 fF)	15.6 mV	1.1%	0.695 mV	≈0
4×8 μm^2 (145 fF)	28.8 mV	0.75%	0.654 mV	≈0
4×4 μm^2 (72 fF)	47.8 mV	1.1 %	0.675 mV	≈0

Table 5.5: Circuit III characteristics

reported in Table 5.5 for the three structures. A non-uniformity of 1.1% was observed that is in good agreement with the Monte-Carlo simulations, described in 3.3.2.

5.3.3 Pixel optical characterization

The pixel output signal was measured as a function of incident light power. A wide-spectrum halogen lamp was the source of the illumination. An optical filter wheel was used for light intensity attenuation. The optical power density was measured with a calibrated photodiode. Pixel output voltage and noise as a function of the optical power density are represented in Figure 5.29 for the third structure at 10 μs integration time.

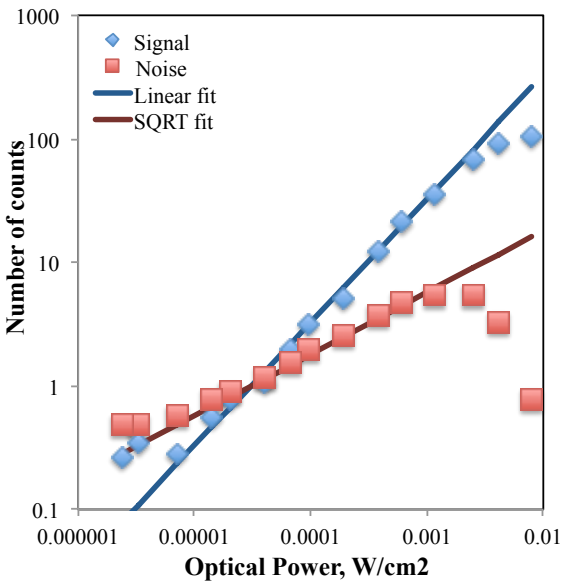

Figure 5.28: Pixel output signal and noise as a function of optical power density

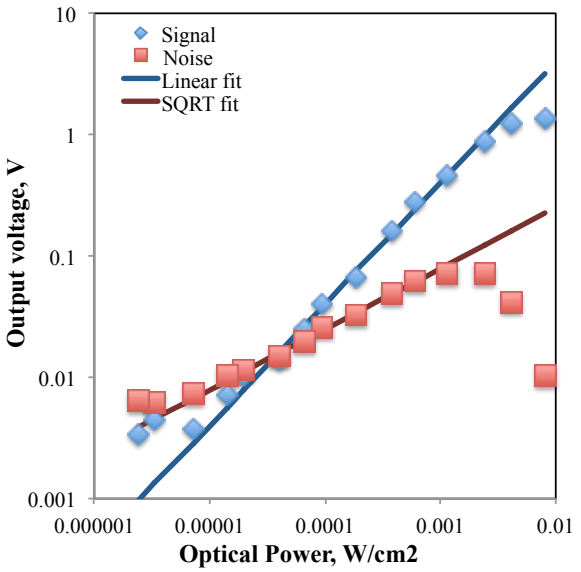

Figure 5.29: Pixel output signal and noise as a function of optical power density

The output voltage range of the circuit is 1.4 V. At low light intensity, the output signal is linearly proportional to the incident power, while the noise is proportional to the square root of the optical power. In addition, the intersection of these two curves is at a voltage value of 15mV. This output voltage corresponds to the detection of one single photon and is an additional confirmation that the pixel works in shot-noise limited operation.

The pixel response non-uniformity (PRNU) was estimated at white light illumination. A PRNU = 1.9% was measured in the linear region for the first pixel structure. This value is partly due to the 1.1% counter non-uniformity and partly to the photodetector response non-uniformity.

5.3.4 Time-gated operation

A picosecond pulsed laser source (Picoquant, $\lambda = 470$nm, pulse width 70ps FWHM) was used to characterize time-gated operation of the pixel arrays. The test setup used in this measurement has been described in section 4.3.3 (Figure 4.11).

The average output voltage for two different gate window widths as a function of time delay is presented in Figure 5.30.

The window repetition frequency was set at 50 MHz. The circuit is capable of sub-nanosecond time-gated operation. A minimum gate width of 0.53 ns can be achieved.

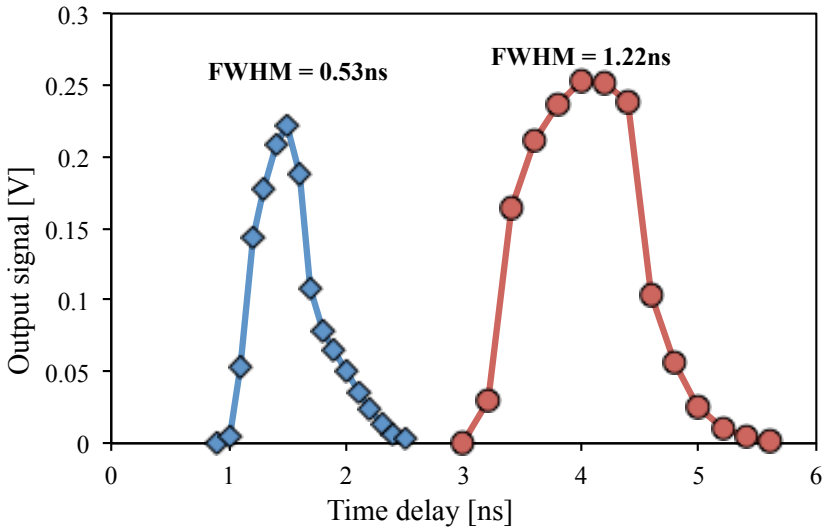

Figure 5.30: Pixel output as a function of time delay for two different gating window widths

5.4 Circuit IV.

5.4.1 Optical pixel characterization: First version

The area occupied by the counter circuit is 171 μm^2. The pixel output voltage histogram was acquired at low illumination levels. The gating signal WIN was maintained low during the acquisition. Figures 5.31 shows one of the histograms of the output voltage that were calculated with 1 million of acquisitions for each pixel.

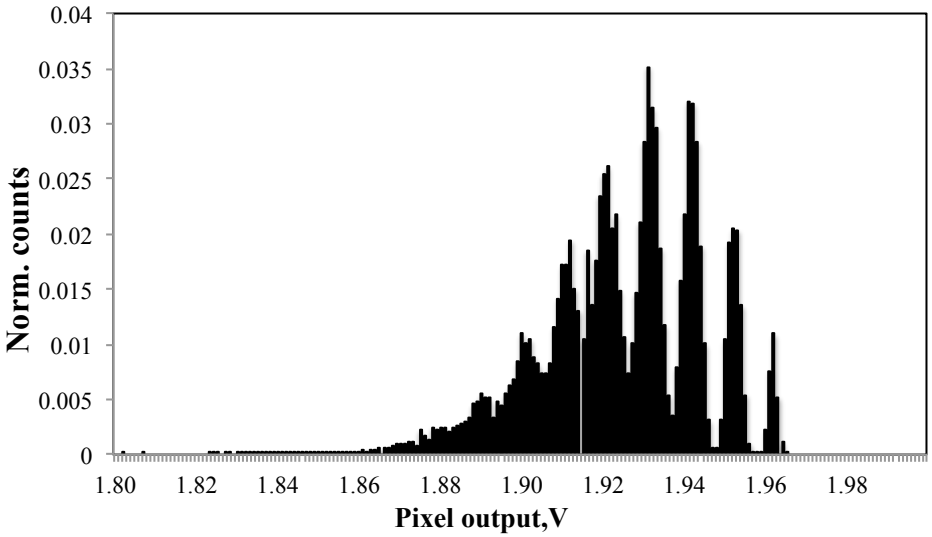

Figure 5.31: Histogram of photon counts. First structure

The step size was set to be about 10 mV by adjusting reference voltage V_B. With this setting, a non-uniformity of 3.3% has been calculated.

The peaks positions in the histogram and the average standard deviation were calculated for each pixel. The average output signal and electronic noise are shown in Figure 5.32 and Figure 5.33 as a function of number of counts, respectively.

As it can be noted, the standard deviation increases with the number of counts. Equation 4.1 describes the dependence of standard deviation on the number of counts N. Based on the histograms, the voltage step size

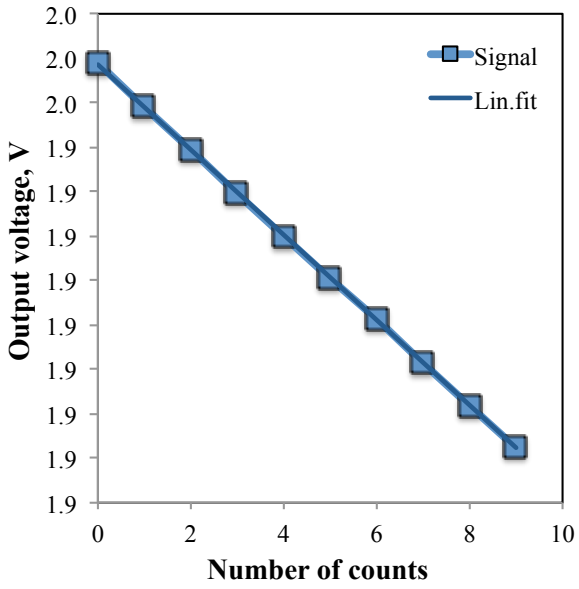

Figure 5.32: Pixel output signal as a function of optical power density

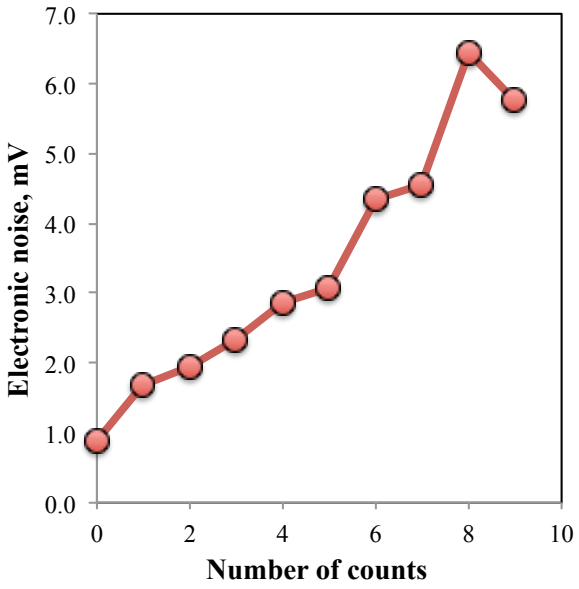

Figure 5.33: Electronic noise as a function of optical power density

and standard deviation across the whole array were calculated. The reset noise is σ_0=0.888 mV, while σ_P≈0.543 mV. Such a high level of additional noise limits the least discriminable voltage step and shrinks the circuit dynamic range. Observing the histogram depicted in Figure 5.31 it is clear that at 10 mV step size maximum 5 counts could be distinguished. Since it was clear that this problem severely impairs the usefulness of this circuit, no further characterization was held.

5.4.2 Optical pixel characterization: Second version

The area occupied by the counter circuit is 263 μm^2. Figures 5.34 shows the output voltage histogram of one pixel tuned at 10 mV step size.

The step size was varied in range from 15 to 50 mV by adjusting reference voltage V_B. At average step size of 10 mV, the non-uniformity of 3.7% has been calculated.

The pixel output voltage as a function of counts is represented in

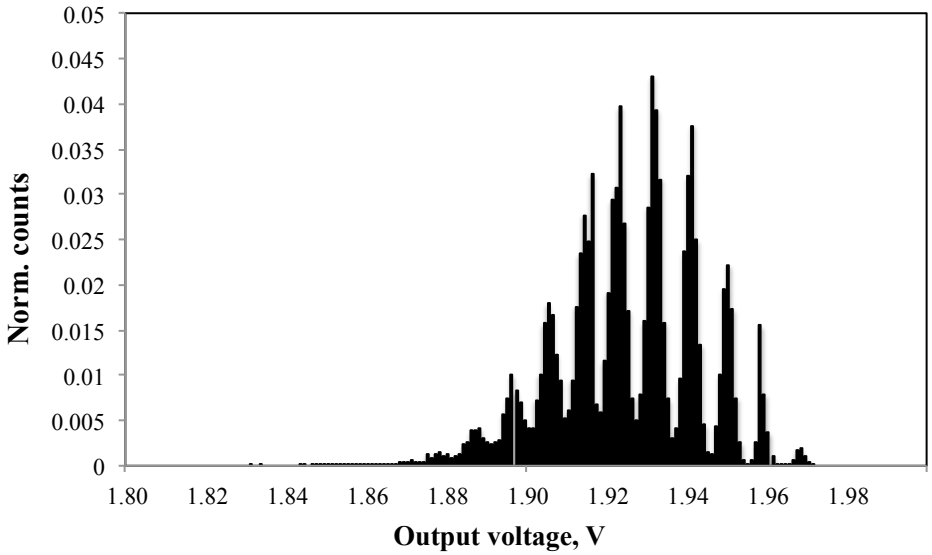

Figure 5.34: Histogram of photon counts. Second version

Figure 5.35. An analysis of the measurements shows that a non-linearity of 3% can be achieved.

The average standard deviation was calculated for each pixel and represented in Figure 5.36 as a function of number of counts.

As it can be noted, the standard deviation increases with the number of counts, but the increment is a bit smaller than in the first version. Based on the histograms, the voltage step size and standard deviation across the whole array were calculated. The reset noise of the present circuit is σ_0=0.6 mV, while $\sigma_P \approx$0.2 mV. Similarly to the circuit presented in 5.4.1, high electronic noise limits the least discriminable voltage step and shrinks the circuit dynamic range.

Table 5.6 summarizes the characteristics of both high-pass filter circuit versions.

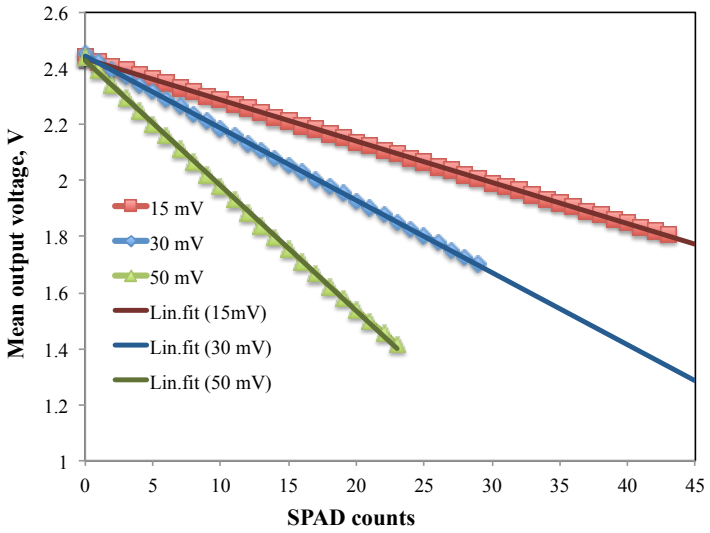

Figure 5.35: Second structure: output voltage as a function of counts

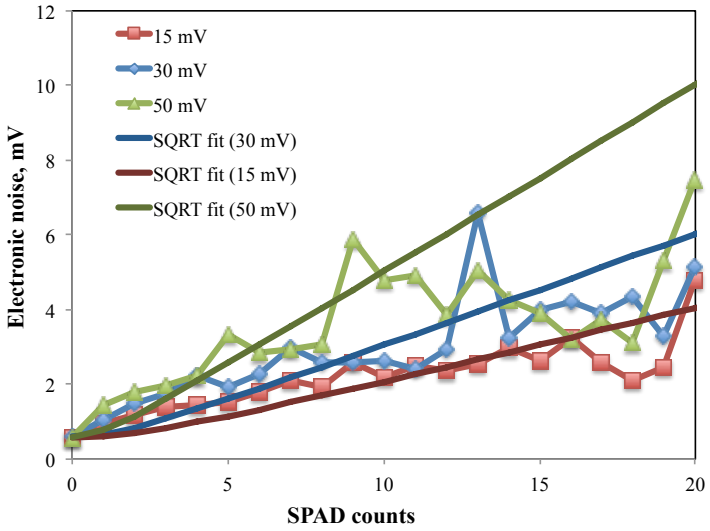

Figure 5.36: Electronic noise. Second structure

Structure	Step Size	N. steps	Step Non-uniformity%	σ_0	$\sigma_{\bar{e}}$	Non-linearity
I	10 mV	10	3.5%	0.88 mV	≈ 0.54	—
II	15.74 mV	25	3.70%	0.58 mV	0.2 mV	3.54%
	28.16 mV	20	3.14%	0.6 mV	0.3 mV	3.67%
	50 mV	17	2.37%	0.59 mV	0.5 mV	3.61%

Table 5.6: Circuit IV. Summary of preliminary output characteristics

Chapter 6

Conclusions and Future Work

The goal of this thesis has been the design and characterization of several readout circuits to be implemented in SPAD-based pixels for photon counting applications. The main design goals were compactness, good uniformity, low power consumption and sub-nanosecond timing resolution. A few linear test arrays have been fabricated in different CMOS technologies. The performance of four circuits based on different operating principles has been investigated.

First of all, the compact design of all four structures has been achieved due to the analog implementation of the readout. The area occupied by each of the circuits is not greater than 300 μm^2 that is a factor 10 improvement in comparison to a digital implementation [73].

The performance of Circuit I based on charge transfer principle has been evaluated (see section 5.1). An array of these counters, not including SPAD and gating electronics, was fabricated in a 0.35 μm CMOS process and has been experimentally characterized. The area occupied by the circuit is 230 μm^2 and the power consumption is 190 nW per pixel at 1MHz repetition rate. The circuit has a programmable resolution with a 4% non-uniformity of the output voltage step. An INL of 0.6 and 1 LSB error and a DNL of 0.3 and 0.6 LSB have been measured at 7- and 8-bit

resolution, respectively. These characteristics are acceptable for photon-counting applications and the circuit is suitable as in-pixel counter in SPAD based image sensors.

The circuit non-uniformity worsened by the parasitic current path through transistor M_4 and the clock feedthrough. However, this effect is significantly reduced within a range of reference values V_{REF1} and V_{REF2} assuring non-linearity of approximately 4%. As the pixel does not contain a detector, for the future work it would be interesting to implement a SPAD array based on this concept, including also a gating circuit.

Circuit II (section 3.2), based on resistive switch principle, is a refinement of the design presented in [143, 144]. The design in [143, 144], which has the shortcomings of high power consumption in inverter and high non-uniformity of 11%. In order to improve the circuit performance, pMOS transistors were introduced, thus sacrificing the circuit compactness. Two linear test arrays of pixels with two different switch dimensions have been fabricated in a 0.15 μm CMOS technology and an electro-optical characterization has been performed. In comparison to [143], the area occupied by the circuit is slightly larger (230 μm^2 versus 200 μm^2 in [143]) due to pMOS transistors exploitation. On another hand, the circuit non-uniformity has been improved by 10%. The pixel current consumption has been measured to be 280 nA at 100 kHz repetition rate which is almost two times lower than the value presented in [143] (500 nA at 100 kHz). Also, time-gated measurements have shown that a sub-nanosecond time window of 0.95 ns at FWHM can be achieved (1.1 ns in [143]). A great advantage of the present circuit is its programmable voltage step which can be tuned taking into account application requirements and, therefore, providing a trade-off between the resolution and output non-uniformity. In addition, due to the low INL and DNL no additional calibration is needed.

The measurement results also suggest that a better non-uniformity

can be obtained at a larger gate of the nMOS switch M_{10}, thus making technological mismatch less significant. However, larger M_{10} leads to the increase of the occupied area on the substrate, the layout can still be improved in the future designs. The present work was focused on the analysis of the circuit performance, therefore, the layout was not optimized for the compactness and its design can still be improved.

The third readout circuit is based on charge sharing principle. The circuit includes only 14 transistors and occupies an area of 255 μm^2. Three structures with different capacitor sizes have been chosen for a test implementation. The pixels, comprising also a SPAD, have been assembled into a linear array of 40 pixels. Characterization measurements have demonstrated that the present circuit type benefits an excellent non-uniformity of approximately 1% among the pixels. This number represents a factor 10 improvement over the value obtained in [143]. Low PRNU of 1.9% assures a uniformity of the outputs among different pixels, therefore, additional non-uniformity adjustment is not necessary. Moreover, a remarkable feature of the circuit is its constant in time electronic noise equal to the reset noise. Thus, even very small step could be still discriminated with applied noise subtraction. A sub-nanosecond time window of 0.53 ns FWHM has been obtained in the time-gated measurements. This value is two times lower compared to Circuit II. The pixel current consumption has been measured to be 350 nA at 100 kHz repetition rate that is 30% lower than the current consumption value presented in [143].

The dynamic range of Circuit III depends on the charge capacitance value. That is, larger dimensions of transistor M_{10} assures smaller the step size and, hence, a wider dynamic range. On another hand, a large capacitance would increase the pixel size. A pixel array based on this design should therefore take into account the particular application demands in terms of dynamic range. As the output voltage step size is gradually

decreasing with each SPAD count due to the output voltage non-linear dependence, an additional non-linear calibration is needed. Despite the complexity of this adjustment, the intrinsic signal compression may be exploited to expand the dynamic range. Low electronic noise and low PRNU suggest that this circuit is the better solution for a large array assembling.

Two versions of the circuit presented in section 3.4.1, which includes a high-pass filter and a resistive switch, were realized and manufactured in a 0.15 μm CMOS technology. A preliminary optical characterization of the first configuration (section 5.4.1) has been conducted. The reset noise for the present type of circuit is σ_0=1.3 mV, while the additional noise at each step is $\sigma_P \approx 0.288$ mV. Such a high level of noise limits the least discriminable voltage step and reduces the circuit dynamic range. For this reason, no further characterization of this HPF type was conducted. The second circuit configuration, described in section 3.4.4, has shown an output non-linearity of 3.7% and an electrical non-uniformity among the pixel of 3.5%. The reset noise of σ_0=0.6 mV, while $\sigma_P \approx 0.2$ mV. Similarly to the circuit presented in 3.4.1, high electronic noise limits the least discriminable voltage step and reduces the circuit dynamic range. Therefore, also for this configuration no time-gated measurement have been performed.

The counter in these circuits operates on a resistive switch principle. Therefore, deviation of the pulse width at the gate of transistor M_7 is the main reason of the high electronic noise and high non-linearity of these structures. Sacrificing the circuit area, an inverter could be introduced to stabilize the pulse width duration. For future work it could be interesting to implement this type of circuit with the counter described in 3.3. Being less sensitive to the pulse duration, the circuit could show better results.

Along with the circuit refinement in the future design, the array should be assembled with high resolution and improved peripheral electronics. Pixel fill factor and pixel pitch could be further improved not only

with circuit layout design, but also with a new geometry of SPAD and a reduced guard ring.

The summary Table 6.1 compares the related works discussed in the state-of-the-art (Chapter 2) with the circuits presented in this dissertation.

Ref.number	[126]	[144]	[146]	Circuit I	Circuit II (1str)	Circuit II (2 str)	Circuit III (1 str)	Circuit III (2 str)	Circuit III (3 str)
Technology, μm	0.13	0.35	0.13	0.35	0.15	0.15	0.15	0.15	0.15
Counter type	ANLG	ANLG	ANLG	ANLG	ANLG	ANLG	ANLG	ANLG	ANLG
Area, μm^2	1300	200	83	230	230	230	255	255	255
Step size, mV			Progr.	Progr.	Progr.	Progr.	15.6	28.8	47.8
Resolution, bit	7	7		7 | 8					
INL, LSB	0.7	n.m.		0.6 | 1.0	0.15	0.15	non-linear calibration needed		
DNL, LSB	1.9	n.m.		0.3 | 0.6	0.1	0.09			
PRNU, %		11	2	4	10	8	1.9	1.9	1.9
Electronic reset noise, mV			0.4	1.2	0.7	0.7	0.6	0.6	0.6
Noise contribution at each step, mV				n.m.	0.05	0.05	$\approx$0	$\approx$0	$\approx$0
Minimum gating window					0.95 ns	0.95 ns	0.53 ns	0.53 ns	0.53 ns
Power per pixel	200μW @500kHz	500nW @1MHz		190nW @1MHz	0.9μW @100kHz	0.9μW @100kHz	1.1μW @100kHz	1.1μW @100kHz	0.9μW @100kHz

Table 6.1: Summary table on in-pixel analog counters for SPAD based arrays

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