



UNIVERSITÀ
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DEPARTMENT OF INFORMATION ENGINEERING AND COMPUTER SCIENCE

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FONDAZIONE BRUNO KESSLER

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OPTIMIZED SINGLE ELECTRON BIPOLAR AVALANCHE
TRANSISTORS FOR INNOVATIVE THZ/IR IMAGING SYSTEMS

Abderrezak Boughedda

Advisor

Dr Leonardo Gasparini

Fondazione Bruno Kessler

Industrial Tutor

Mr Daniele Perenzoni

Sony Semiconductor Solutions Europe

Co-Advisor

Prof Lucio Pancheri

Università degli Studi di Trento

Abstract

This thesis presents the design, test and characterization of optimized Single-Electron Bipolar Avalanche Transistors (SEBAT) for use in fully-integrated antenna-coupled Field-Effect Transistor (FET) detector arrays. Targeting the TeraHertz (THz) and Long-Wavelength Infra-Red (LWIR) spectra, these detectors offer the advantage of room-temperature, vacuum-free operation and compatibility with standard Complementary Metal-Oxide Semiconductor (CMOS) fabrication technology, but they are limited by poor Signal-to-Noise Ratios (SNR) due to weak optical input power and large low-frequency noise.

Traditional readout architectures address this challenge through a multi-stage amplification chain that can operate even in presence of faint signals limiting the impact of flicker noise. However, these schemes necessitate complex, area-consuming and power-intensive circuitry that hinders the scalability of high-resolution, real-time imaging systems.

SEBAT-based architectures have emerged as a promising alternative that exploits the device's intrinsic avalanche multiplication to convert the signal generated by the detector directly into a train of digital pulses, thereby eliminating the need for external analog amplification.

Unfortunately, early experimental implementations in deep sub-micron technology exhibited poor efficiency, with electron-to-pulse conversion rates of only 0.001%, four orders of magnitude below theoretical predictions and state-of-the-art devices.

This research work addresses the challenge of optimizing the SEBAT device for THz and IR imagers based on antenna-coupled FET-detectors through:

- Problem analysis – Identifying the physical mechanism limiting existing implementations using Technology Computer-Assisted Design (TCAD) simulations and matching the results with experimental data.
- Modeling – Developing a comprehensive SPICE model for the SEBAT characterized by low complexity to facilitate the design of fully-integrated large-scale antenna-coupled FET detector arrays.
- Optimization and fabrication – Designing, testing and characterizing optimized SEBAT devices in 110 nm CMOS standard technology, overcoming the limitations of previous implementations.
- Image sensor development – Integrating the optimized devices in detector arrays targeting 0.9 THz, 1.5 THz and 21-38 THz (corresponding to the spectral LWIR range of 8-14 μm).

Experimental results demonstrate that the optimized SEBAT implementations achieve efficiencies compatible with single-electron detection. This achievement enables compact, power-efficient detector arrays through standard 110 nm CMOS fabrication for applications in security screening, biomedical diagnostics, and industrial inspection.

Keywords

CMOS integration, FET detectors, SEBAT, Single-electron detection

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Chapter 1

1. Introduction and theoretical background

This thesis explores the optimization of Single Electron Bipolar Avalanche Transistors (SEBAT) targeting the readout of TeraHertz (THz) and InfraRed (IR) detection systems based on antenna-coupled Field-Effect Transistor (FET) detectors. More in details, this work focuses on analyzing the limitations and improving electron conversion efficiency through TCAD modeling and parameter optimization. This detection approach has been applied across different spectral bands through dedicated test arrays, demonstrating the versatility of the integration of a SEBAT readout for FET detectors for both THz and IR wavelengths. This chapter provides the motivations behind this thesis by first introducing THz imaging applications, then presenting the theoretical background on IR and THz detection technologies, followed by an overview of detector technologies and readout architectures. The chapter concludes by outlining the specific research objectives and contributions of this work.

1.1. Background and Motivation

Medical diagnostics, security screening, industrial quality control, and materials characterization require sensing technologies that can safely penetrate materials while providing information about surface properties. Within this framework, electromagnetic radiation serves as a versatile tool as it provides material-specific responses and absorption depths according to the wavelength, while the maturity of modern fabrication enables the seamless integration of compact sources and detectors into complex imaging systems.

The electromagnetic spectrum spans from radio waves through visible light to gamma rays, with each region characterized by distinct wavelengths and photon energies and this work specifically addresses challenges related to the IR and THz bandwidths. The IR region occupies wavelengths from approximately 700 nm to 1 mm, subdivided into near-infrared (NIR, 0.7-1.4 μm), short-wave infrared (SWIR, 1.4-3 μm), mid-wave infrared (MWIR, 3-8 μm), long-wave infrared (LWIR, 8-15 μm), and far-infrared (FIR, 15-1000 μm). The THz region, sometimes called the "terahertz gap," occupies frequencies from 0.1 to 10 THz (wavelengths from 3 mm to 30 μm), bridging the

gap between microwave electronics and infrared photonics. Fig. 1-1 shows the location of the IR and THz regions in the electromagnetic spectrum.

Conventional IR sensors use mature technologies to detect temperature differences, identify materials from their heat signatures, and provide detailed surface images. While standalone IR sensing systems are commercially available, practical integration requires detectors compatible with standard CMOS fabrication processes and capable of room-temperature operation without vacuum packaging. This compatibility enables seamless system integration and reduces production costs compared to hybrid assembly approaches.[1].

THz imaging complements IR detection by penetrating non-polar materials opaque to IR, providing spectroscopic fingerprints of molecular rotations and vibrations, and enabling safe biological imaging due to non-ionizing photon energies ($\sim 0.4\text{-}40$ meV) [2]. These unique properties allow THz systems to probe material composition and internal structure in applications where IR and visible light cannot penetrate [2]. However, achieving CMOS-compatible IR detection that can be monolithically integrated with THz sensing in a single chip remains an open challenge, limiting the development of compact dual-band detection systems.

While combining IR and THz detection could theoretically provide complementary surface and subsurface information in a unified multispectral platform [3],[4] achieving such integration requires first establishing efficient, CMOS-compatible detection mechanisms for each spectral band independently. This thesis builds upon the premise that both infrared (IR) and terahertz (THz) radiation can be detected using antenna-coupled FET detectors in standard CMOS technology, where the operational frequency is primarily determined by the scaling of the antenna geometry. These antennas are realized utilizing the intrinsic metal layers of the CMOS process—structures conventionally reserved for power distribution and signal routing—thereby enabling monolithic integration without post-processing. In this context, a readout scheme based on SEBAT has recently been proposed as a promising solution, but suffering for poor electron detection efficiency, not justified by theoretical predictions. This work therefore focuses on validating the SEBAT-based readout approach for antenna-coupled FET detectors separately for IR and THz wavelengths, demonstrating the versatility of this readout architecture across different spectral regions without attempting to integrate them into a multispectral imaging system. The work explores fundamental detection mechanisms, optimization strategies, and performance limits for each band, providing the foundation necessary for potential future integration efforts.

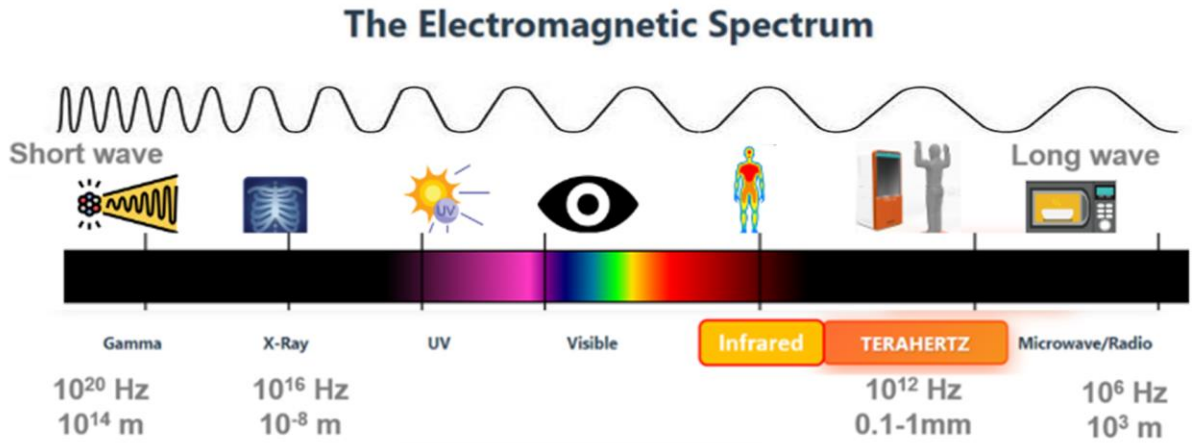


Fig. 1-1. The electromagnetic spectrum.

While IR detection is commercially established, THz detection faces persistent sensitivity challenges. Current THz detection methods exhibit limited sensitivity, with state-of-the-art FET-based detector arrays achieving Noise Equivalent Power (NEP) values of several nW/ $\sqrt{\text{Hz}}$ [5]. Recent advances have improved THz detector performance through optimized antenna designs and CMOS integration [6], yet significant gaps remain. Complex integration requirements including precise antenna-detector matching, low-noise readout circuits, and source modulation schemes increase system cost and complexity [5].

Traditional detector readout architectures implement separate signal processing chains for each spectral band, with customized amplification and digitization circuits matched to specific detector characteristics [7]. This approach multiplies system complexity as additional spectral bands are added, since each detector type requires its own optimized readout architecture.

SEBAT-based readout offers architectural simplification by providing avalanche amplification applicable across different detector types. Individual frequency-specific detectors (THz or IR) connect to SEBAT amplifiers that convert detection events into digital pulses through avalanche multiplication, enabling a unified processing backend for multiple spectral bands. However, existing SEBAT implementations for THz detection achieve electron-to-pulse conversion efficiency of only 10^{-4} [8], substantially below the 70% measured by Lany et al. [9]. This performance gap prevents practical adoption of SEBAT technology for detection applications. This thesis addresses this efficiency gap by investigating the fundamental mechanisms limiting SEBAT performance and developing optimization strategies to enable SEBAT-based readout for antenna-coupled FET detection systems for both THz and IR wavelengths.

1.2. THz Applications

THz radiation exhibits characteristic propagation behaviour and material interaction properties that determine its utility for sensing applications. THz waves penetrate many non-conducting materials including clothing, paper, wood, and plastics, but experience strong absorption in liquid water and complete reflection from metals. The interaction with water occurs through dipolar absorption mechanisms, where wave amplitude decreases proportionally to water content in the propagation path. This water sensitivity, combined with non-ionizing photon energies and sub-millimeter wavelengths, defines the fundamental physics underlying THz detection requirements. The non-contact, non-destructive nature of THz measurements derives from these material interaction properties rather than from measurement methodology.

1.2.1 Biomedical applications cancer detection

THz imaging has demonstrated promise as a non-invasive diagnostic method, particularly for the early diagnosis of cancer. The technology helps differentiate between healthy and cancerous tissues by capturing detailed images of the tissue and thus recognizing molecular signatures as shown in Fig. 1-2.

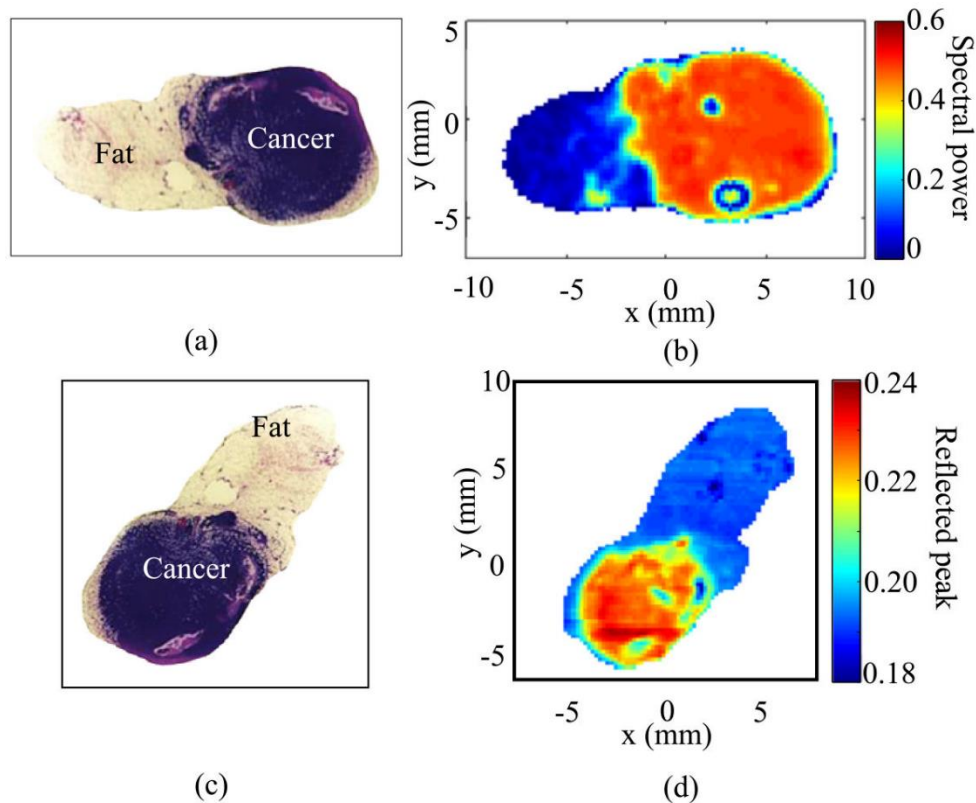


Fig. 1-2. THz images of xenograft mice tumor sample 2. (a) Pathology image, (b) THz image of freshly excised tissue, (c) pathology image (same as in (a)), (d) THz image of FFPE block tissue [10].

This is particularly valuable for mapping tumor margins accurately. Getting precise tumor boundaries during surgery is critical - it can significantly improve surgical outcomes and reduce the chances of cancer recurrence [11],[12]. These types of examinations are intended to avoid invasive procedures in future medical applications.

1.2.2 Pharmaceutical Industry Quality Control

THz imaging provides non-destructive quality control in pharmaceutical manufacturing, detecting voids, cracks, and content non-uniformity in tablets through contrast in dielectric properties [13]. THz time-domain spectroscopy characterizes polymorphic forms and quantifies active ingredient concentration without sample contact [14].

1.2.3 Security Screening Concealed Weapons Detection

THz imaging enables non-invasive detection of concealed weapons, explosives, and contraband through clothing, packaging, and non-metallic barriers due to selective material penetration properties [15],[16]. THz spectroscopy identifies explosives through characteristic molecular absorption signatures in the 500 GHz to 2.5 THz range [17] as demonstrated in postal screening and body scanning applications (Fig. 1-3).



Fig. 1-3. Imaging results showing body-borne concealed threats, a belt with explosives and a gun, obtained by the new sub-THz security body scanner at 3 μ m range [18].

1.2.4 Food and Agriculture Quality Inspection

THz imaging detects contaminants, voids, and packaging defects in sealed food products [19]. In agriculture, THz transmission measurements enable moisture content mapping and structural analysis for crop quality assessment (Fig. 1-4).

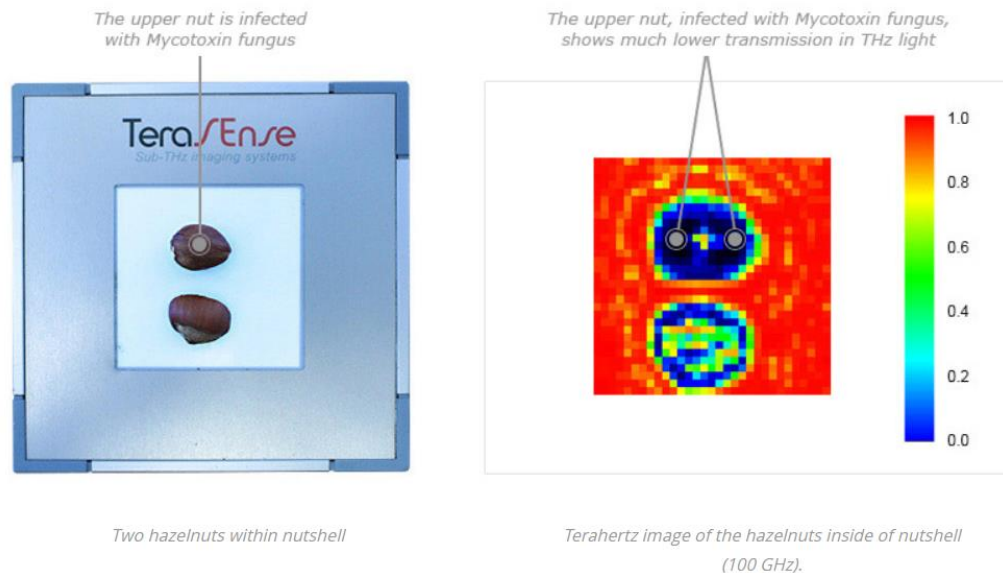


Fig. 1-4 Terahertz imaging demonstrates non-destructive detection of fungal infection in hazelnuts. (a) Experimental setup showing healthy and infected samples. (b) THz transmission image at 100 GHz reveals internal structure, with infected regions showing reduced transmission (blue areas) [19].

1.2.5 Industrial Non-Destructive Testing (NDT) Material Evaluation

Nowadays, manufacturers offer a robust non-destructive evaluation method that use THz imaging to identify inclusions or defects in non-metallic materials and to measure density and humidity fluctuations in materials like ceramics. This method improves manufacturing productivity and product durability by offering high-resolution images of interior features without causing material damage. When compared to other techniques like microwaves and millimeter waves, THz imaging is especially useful because it can see embedded objects with higher spatial resolution and penetrate non-metallic, optically opaque media [20].

1.2.6 Wireless Communication and Science Future Wireless Systems

THz frequencies offer potential for future wireless systems due to available bandwidth in the hundreds of GHz range, enabling data rates from 100 Gbps to several Tbps. However, atmospheric attenuation and limited transmission distance constrain practical deployment [21].

1.3. THz Detection Approaches

The diverse applications described above rely primarily on active THz imaging, where targets are illuminated with controlled THz sources and the reflected or transmitted radiation is measured. Passive THz systems that rely on natural thermal emission are rarely deployed due to extremely low room-temperature THz radiation levels, requiring long integration times (seconds to minutes) and cryogenic detector cooling for adequate sensitivity [22]. In contrast, active systems achieve video-rate imaging (tens of milliseconds per frame) through high-power THz sources, enabling real-time inspection and screening applications. Active illumination also enables precise material characterization through spectroscopic analysis and controlled measurement geometries, making it the dominant approach for practical THz imaging systems [22].

1.4. Terahertz Radiation Sources

THz source generation faces the "terahertz gap" challenge: frequencies exceed conventional electronic oscillator limits (~ 300 GHz) while THz photon energies (0.004-0.04 eV) fall below semiconductor laser requirements (>1 eV). This necessitates specialized approaches including frequency multiplication, quantum cascade lasers, and photoconductive antennas [23].

1.4.1 Fundamental Source Generation Approaches

THz generation employs six primary approaches, each addressing specific operational requirements and frequency ranges.

Laser-Based Direct Generation

Laser systems have emerged as powerful platforms for THz generation, leveraging decades of optical technology development. These approaches exploit the precision and controllability that have made lasers indispensable across countless applications. Far-infrared gas lasers represent one of the earliest successful approaches, utilizing specialized gas mixtures as optical gain media to directly produce coherent THz radiation [24],[25]. These systems, while somewhat bulky, can deliver excellent beam quality and spectral purity. Electrically pumped solid-state lasers have

evolved to provide more stable and predictable output characteristics through precise electrical control, offering researchers better reproducibility and long-term stability [26]. However, the real breakthrough came with Quantum Cascade Lasers (QCLs), which represents a fundamental shift in laser design philosophy [27], [28]. Rather than relying on traditional electronic transitions between atomic energy levels, QCLs exploit quantum mechanical intersubband transitions within carefully engineered semiconductor heterostructures [27]. This approach enables unprecedented control over the output frequency, allowing researchers to essentially "design" the wavelength by adjusting the quantum well dimensions. The tunability and precision offered by QCLs have made them particularly valuable for spectroscopic applications where specific frequencies are required [29],[30].

Frequency Multiplication Sources

Frequency multiplication extends microwave sources to THz frequencies through nonlinear harmonic generation. Microwave synthesizers (10-100 GHz) drive multiplier chains consisting of Schottky diodes or varactor devices, achieving multiplication factors of $3\times$ to $36\times$ to reach the THz range [31], [32]. These systems typically employ chains of frequency doublers, triplers, and higher-order multipliers to step up from easily generated microwave frequencies to the desired THz range. While this approach can be somewhat inefficient due to the multiple conversion stages, it offers excellent frequency stability and precise control. Schottky Barrier Diode (SBD) arrays have proven particularly effective in this role, capitalizing on the fast switching characteristics and nonlinear behavior of these devices [33], [34]. The ability to fabricate arrays of these diodes allows for power combining and improved efficiency, making this approach practical for many applications [35].

Nonlinear Optical Conversion

Nonlinear optical processes generate THz radiation through difference frequency generation, optical rectification, and parametric oscillation in nonlinear crystals. Diode-pumped fiber lasers serve as ideal platforms for these approaches because they provide stable, high-quality optical sources with excellent beam characteristics [28]. Fiber geometry naturally supports efficient nonlinear interactions while maintaining good beam quality. Various nonlinear optical conversion mechanisms, including difference frequency generation, optical rectification, and parametric processes, enable precise manipulation of optical frequencies to generate THz radiation [36]. The ability to generate pulsed THz radiation through these optical techniques has opened up entirely new application areas, particularly in time-domain spectroscopy and imaging [37], [38]. The

coherent nature of the generated radiation, combined with the temporal precision achievable with femtosecond laser systems, allows for time-resolved studies of material properties that would be impossible with other generation methods.

Electron Beam Manipulation

Using the basic connection between accelerating charges and electromagnetic radiation, this technique is arguably the most physically straightforward way to generate THz. Through precise manipulation of electron paths and acceleration, THz radiation can be generated. Backward Wave Oscillators (BWOs) and gyrotrons exemplify this approach, utilizing complex interactions between electron beams and electromagnetic fields [36]. BWOs operate by sending an electron beam through a slow-wave structure where the beam interacts with a backward-propagating electromagnetic wave, creating sustained oscillation [39]. Gyrotrons, on the other hand, exploit the cyclotron motion of electrons in strong magnetic fields to generate radiation [40]. These systems can achieve remarkably high-power levels, making them attractive for applications requiring strong THz sources [41]. The magnetic field configurations used in gyrotrons create unique radiation characteristics that can be tailored through careful design of the magnetic field geometry [42]. The periodic acceleration of electrons in these systems creates radiation patterns that can be quite different from other generation methods, offering unique capabilities for specific applications [43].

Photoconductive Switch Mechanisms

This approach represents one of the most compact and versatile methods for THz generation, combining semiconductor physics with optical excitation in an elegant and practical package. The underlying principle exploits the rapid generation and acceleration of charge carriers in specially designed semiconductor structures. The typical implementation involves metal strip-line configurations fabricated on semiconductor substrates, often GaAs or similar materials with favorable electronic properties [44]. When femtosecond laser pulses illuminate the gap between these metal electrodes, they rapidly generate electron-hole pairs in the semiconductor. An applied bias voltage accelerates these carriers, creating transient current pulses that radiate THz electromagnetic waves [45]. Due to their small size, photoconductive switches are especially appealing for portable and lab-scale uses [46]. Optimizing particular performance attributes, such as bandwidth, power, or pulse duration, is made possible by the versatility of substrate materials and electrode geometries. Recent advances in antenna design and substrate engineering have significantly improved the efficiency and bandwidth of these devices [47].

Photomixers

Photomixers use two independent tunable laser sources to generate difference frequencies in the THz range. Two laser beams at different frequencies illuminate a photoconductive antenna, where the THz difference frequency excites the semiconductor material, creating coherent THz wave emission [48].

1.4.2 Comparative Performance Characteristics

Each THz source type presents distinct performance parameters, listed in Table 1-1.

Table 1-1. THz Radiation Source Types and Performance Parameters

Source Type	Frequency Range	Power Output	Coherence	Complexity	Typical Applications
Direct Laser	0.1-10 THz	Low- Moderate	High	Moderate	Spectroscopy
Electronic Devices	0.3-3 THz	Low	Moderate	High	Communication
Electron-Based	0.1-3 THz	High	Moderate	Very High	Industrial
Nonlinear Optical	0.1-3 THz	Pulsed	High	Moderate	Research
Photoconductive	0.1-3 THz	Pulsed	Moderate	Low	Imaging
Photomixer	0.1-3 THz	Low	High	Moderate	Sensing

1.5. THz detectors

THz detectors can be classified into two primary categories based on their detection mechanisms: **coherent (heterodyne) and incoherent (direct) detection systems.**

Coherent detectors employ heterodyne mixing, combining the received THz signal with a local oscillator to produce a beat frequency output that preserves phase and amplitude information. Schottky diode mixers can operate up to 25 THz with high conversion efficiency and fast response times, but require complex waveguide integration [49]. Superconductor-Insulator-Superconductor (SIS) mixers operate in the 300-700 GHz range with exceptional sensitivity but require cryogenic cooling [17]. Hot electron bolometers (HEB) provide picosecond response times suitable for THz mixing applications but necessitate cryogenic operation [50].

Incoherent detectors directly convert THz radiation to electrical signals without requiring local oscillators. Pyroelectric detectors are based on polar crystals that exhibit temperature-dependent electrical polarization, providing broadband response but limited sensitivity [51]. Microbolometers are thermal detectors that measure radiation-induced temperature changes through resistance variations, offering room-temperature operation [52]. Golay cells are opto-acoustic detectors providing higher sensitivity than pyroelectric detectors but with slower response times [53]. Field-Effect Transistor (FET) detectors convert THz radiation to DC voltage through plasma wave rectification in the transistor channel, offering room-temperature operation and direct compatibility with standard CMOS fabrication processes [44-46]. Due to their relevance for SEBAT-integrated multispectral systems, FET detectors are analyzed in detail in Section 0.

1.6. Figures of merit for THz detectors

The performance evaluation of THz detectors relies on several key figures of merit that characterize the device's sensitivity and noise behavior. These metrics enable quantitative assessment of the detector's ability to convert incident radiation into measurable electrical signals while accounting for intrinsic noise contributions [54]. The two fundamental figures of merit are responsivity (R) and Noise-Equivalent Power (NEP).

1.6.1 Responsivity

The responsivity characterizes the detector's signal generation efficiency, defined as the ratio between the measured electrical output and the incident electromagnetic power. This parameter can be expressed in terms of voltage or current, depending on whether the readout measures voltage or current signals:

$$R_v = \frac{V_s}{P_{in}} \left[\frac{V}{W} \right], \quad R_i = \frac{I_s}{P_{in}} \left[\frac{A}{W} \right] \quad 1-1$$

where V_s and I_s denote the detector output voltage and current signals, respectively, while P_{in} represents the incident THz power impinging on the detector active area.

1.6.2 Noise-Equivalent Power (NEP)

The noise-equivalent power quantifies the minimum detectable signal level of the detector. Specifically, NEP corresponds to the incident power level that produces an output signal equal to the

noise level, resulting in unity signal-to-noise ratio within a 1 Hz measurement bandwidth. This figure of merit is obtained by dividing the detector noise spectral density by its responsivity [54]:

$$NEP_v = \frac{V_n}{R_v} \left[\frac{W}{\sqrt{Hz}} \right], \quad NEP_i = \frac{I_n}{R_i} \left[\frac{W}{\sqrt{Hz}} \right] \quad 1-2$$

where V_n and I_n correspond to the voltage and current noise spectral densities of the detector, respectively. A lower NEP indicates enhanced sensitivity, with the detection threshold scaling as $P_{min} = NEP \times \sqrt{\Delta f}$ for a given measurement bandwidth Δf .

1.6.3 Comparative performance

Room-temperature THz imaging applications require careful selection among available detector technologies, each presenting distinct trade-offs in response time, sensitivity, and imaging capability. Time-domain spectroscopy (THz-TDS) systems [55] employ ultrafast laser pulse sampling with electro optical switching, achieving exceptional sensitivity and broad spectral coverage through temporal waveform acquisition and Fourier transform analysis [37]. However, THz-TDS implementations require expensive femtosecond laser sources, optical delay stages for temporal waveform sampling, and raster scanning for spatial imaging, limiting practical imaging applications despite their superior spectral resolution capabilities. Antenna-coupled microbolometer arrays [56] provide high sensitivity through thermal detection mechanisms, achieving noise-equivalent power values competitive with cryogenic detectors while operating at room temperature.

These detectors enable real-time imaging when coupled with high-power sources such as quantum cascade lasers [57], though their fabrication requires complex post-processing including suspended membrane structures and vacuum encapsulation [58], resulting in significant manufacturing costs. Pyroelectric detectors [59] offer broadband response across the THz spectrum by detecting radiation-induced polarization changes in ferroelectric crystals. Their inherent AC coupling characteristic requires source modulation or chopping, and they exhibit relatively low sensitivity compared to bolometric or THz-TDS approaches, though commercial pyroelectric camera systems provide adequate imaging capability for high-power illumination scenarios [60]. FET-based detectors achieve the most favorable balance for integrated imaging systems, providing moderate sensitivity with fast electronic response times and excellent scalability to large-format focal plane

arrays. Their direct CMOS fabrication compatibility eliminates specialized processing steps, significantly reducing manufacturing complexity and cost while enabling monolithic integration with readout electronics.

The optimal detector choice depends on specific application requirements: THz-TDS suits spectroscopic analysis demanding high spectral resolution, microbolometers serves applications requiring maximum sensitivity with modest frame rates, pyroelectric systems provide cost-effective solutions for high-power active imaging, and FET arrays enable practical real-time THz imaging through scalable CMOS integration [61].

1.7. Infrared detection

This thesis addresses detection across both THz and infrared spectral bands. The complementary capabilities of these regions (THz penetration through non-polar materials revealing subsurface structures, and IR thermal emission enabling surface characterization) motivate the development of a unified detection platform compatible with standard CMOS fabrication. Traditional infrared detection employs two distinct technological approaches. Quantum detectors utilize narrow-bandgap semiconductors such as indium-gallium-arsenide (InGaAs) or mercury-cadmium-telluride (MCT) to convert absorbed photons directly into electron-hole pairs, achieving high sensitivity but requiring cryogenic cooling and specialized non-CMOS-compatible fabrication processes [49]. Thermal detectors measure radiation-induced temperature changes through microbolometer resistance variations [62] or pyroelectric polarization effects, operating at room temperature but with slow millisecond-scale response times and complex post-processing requirements including suspended membrane structures and vacuum encapsulation [63].

Recent theoretical work has proposed extending the plasma wave rectification mechanism used in THz FET detectors to infrared wavelengths through appropriate antenna scaling [64]. This approach would enable a unified detection mechanism across THz and IR bands using standard CMOS fabrication.

1.8. Field-Effect Transistor Detectors

Among the THz detector types described in Section 1.5, FET-based detectors are particularly relevant for this research due to their compatibility with standard CMOS fabrication processes and room-temperature operation [65]. These characteristics enable monolithic integration with readout circuits and large-scale array implementations for imaging applications.

FET detectors operate through plasma wave rectification in the transistor channel. When THz radiation couples to the gate-source terminals of the transistor, it induces electron density oscillations in the channel as shown in Fig. 1-5. These oscillations generate a measurable DC voltage between the drain and source terminals [66]. The detection mechanism can be described through two complementary theoretical frameworks. Plasma wave theory describes collective electron oscillations in the confined two-dimensional electron gas of the transistor channel, where the plasma wave velocity and resonant frequency depend on the carrier density and channel dimensions, analogous to acoustic wave propagation in confined media. Self-mixing detection treats the FET as a nonlinear mixing element that down-converts the high-frequency THz signal through the quadratic nonlinearity of the transistor I-V characteristics, producing a DC component proportional to the incident THz power [67].

FET detectors produce DC voltage output proportional to incident THz power. The integration of these detectors with appropriate readout architectures enables signal processing and large-scale imaging array implementations [11].

FET-based THz detectors offer several advantages for practical imaging system implementation. Direct fabrication in standard CMOS processes eliminates specialized processing steps, reducing cost and enabling co-integration with readout electronics. Planar fabrication enables implementation of large-format focal plane arrays with thousands of detector elements. Passive detection mode with minimal DC bias current enables low-power operation suitable for portable and battery-powered applications. Unlike cryogenic detectors, FET-based detection functions at ambient temperature, significantly reducing system complexity and cost [7], [61].

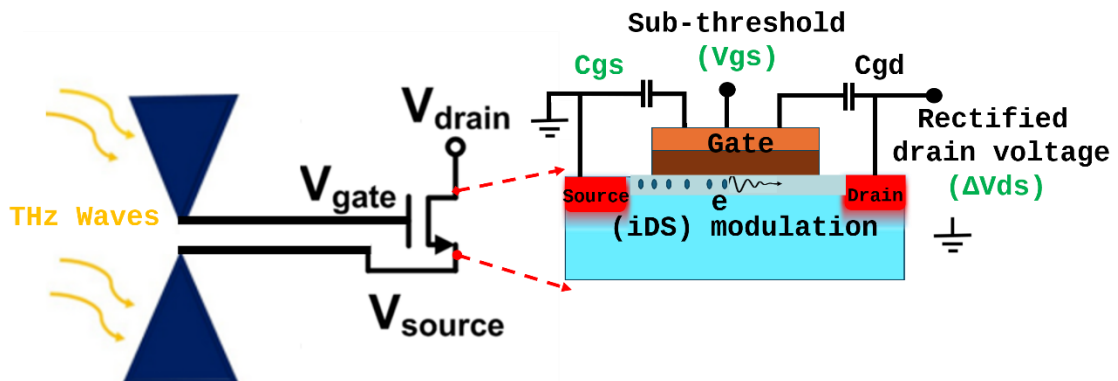


Fig. 1-5. Simplified detector schematic: FET detector on the left, and device cross section on the right.

1.9. Readout Architectures for FET Detectors

As described in Section 1.8, FET detectors generate a DC voltage ΔV_d s between drain and source terminals in response to THz radiation. The practical implementation of FET detector arrays requires readout circuits capable of measuring these signals with sufficient sensitivity while maintaining compatibility with large-format array architectures. The readout channel is a fundamental block in THz imaging systems, and its proper design enables better performance in terms of sensor resolution, occupied area, complexity, and power consumption [68].

1.9.1 Traditional Voltage-Mode Readout

THz detection with Field-Effect Transistor-based detectors requires low-noise amplification, which typically involves trade-offs in terms of complexity, power, and area, resulting in severe scalability constraints for pixel integration into imaging arrays. The low amplitude (tens of μV to several mV) combined with source modulation requirements (DC to 1 kHz for lock-in detection) present significant challenges for readout design [7].

Various interface architectures have been demonstrated to address these challenges. Switched capacitor structures, cascaded chopper instrumentation amplifiers, and capacitances to reduce integrated noise have been employed to reduce integrated noise through chopping techniques [6] or integrated ADCs to process the signal on-chip [7].

A solution based on programmable-gain amplifiers with correlated double sampling and a 6-bit ADC achieves $262 \text{ pW}/\sqrt{\text{Hz}}$ range at 600 GHz using high chopping frequency (40 kHz), though not all THz sources can operate at this frequency and the readout is poorly scalable [69]. VCO-based ADC implementations avoid prefilter requirements but place VCOs outside the pixel, resulting in non-scalable architectures, achieving 218 kV/W responsivity and $91 \text{ pW}/\sqrt{\text{Hz}}$ NEP at 930 GHz [70].

Advanced readout chains incorporating notch filters and chopper instrumentation amplifiers with high-resolution sigma-delta converters achieve 3.3 kV/W responsivity and $106 \text{ pW}/\sqrt{\text{Hz}}$ NEP at 860 GHz, with the sigma-delta converter occupying $400 \times 260 \text{ }\mu\text{m}^2$ and the chopper amplifier occupying $1330 \times 440 \text{ }\mu\text{m}^2$ [71]. Current-biased approaches can increase gain at the cost of more flicker noise [72], while successive-approximation calibration schemes adjust pixel operating points to improve uniformity in the presence of pixel-to-pixel process variation [73].

Low-noise CMOS THz imagers based on source modulation with in-pixel high-Q passive switched-capacitor N-path filters have been demonstrated [6] and 1 k-pixel video cameras for 0.7-1.1 THz imaging have been implemented in 65-nm CMOS achieving real-time imaging capability

[74]. Compact implementations based on continuous-time incremental sigma-delta ADCs with chopper stabilization achieve pixel-level integration in $400 \times 400 \mu\text{m}^2$ with $80 \mu\text{W}$ power consumption [7].

Despite the performance reached, the main problems regarding these interfaces remain large area, high power consumption, and complexity. An ideal solution should achieve small area while maintaining low noise level, performing direct conversion between detected THz signal and digitized output.

1.9.2 Current-Mode Detection and Single-Electron Counting

An alternative approach considers the FET output from a current-mode perspective. The THz-induced channel modulation creates discrete electron injection events that generate detection current when the FET senses the THz signal [68]. This current-mode view becomes particularly relevant when considering device-level amplification strategies. An ideal solution should achieve small area while maintaining low noise level, performing direct conversion between detected THz signal and digitized output. This motivates exploration of alternative readout approaches capable of detecting individual electron events through avalanche multiplication, as discussed in Section 1.10.

1.10. Single-Electron Detection Principles

Single-electron detection represents the fundamental limit of sensitivity in electronic sensing systems, offering the theoretical possibility of achieving quantum-limited performance through the detection and enumeration of individual charge carriers [9]. Traditional single-electron devices, such as single-electron transistors (SETs), have demonstrated individual charge detection capabilities but typically require cryogenic operation and sophisticated nanofabrication techniques that limit practical implementation [75]. The primary challenge in room-temperature single-electron detection lies in overcoming thermal noise in the detection structure and readout electronics, which at ambient temperatures corresponds to energies significantly exceeding the charging energy of conventional quantum dots.[76]. This thermal noise floor creates a detection threshold that obscures individual electron events, representing a fundamental barrier to practical room-temperature sensing. Avalanche multiplication provides a promising solution by offering intrinsic signal amplification at the device level [77]. Through avalanche processes, individual electrons trigger multiplication cascades that amplify detection signals to levels substantially above the thermal noise floor. This approach enables the conversion of quantum-scale events into macroscopic signals de-

tectable by conventional electronics, effectively bridging the gap between quantum-limited sensitivity and practical implementation requirements [78]. The integration of avalanche multiplication with single-electron detection forms the theoretical foundation for developing room-temperature, quantum-limited detection systems that maintain ultimate sensitivity while addressing practical limitations of conventional approaches. Fig. 1-6 summarizes the challenges of Single-Electron detection and the proposed avalanche-based solution.

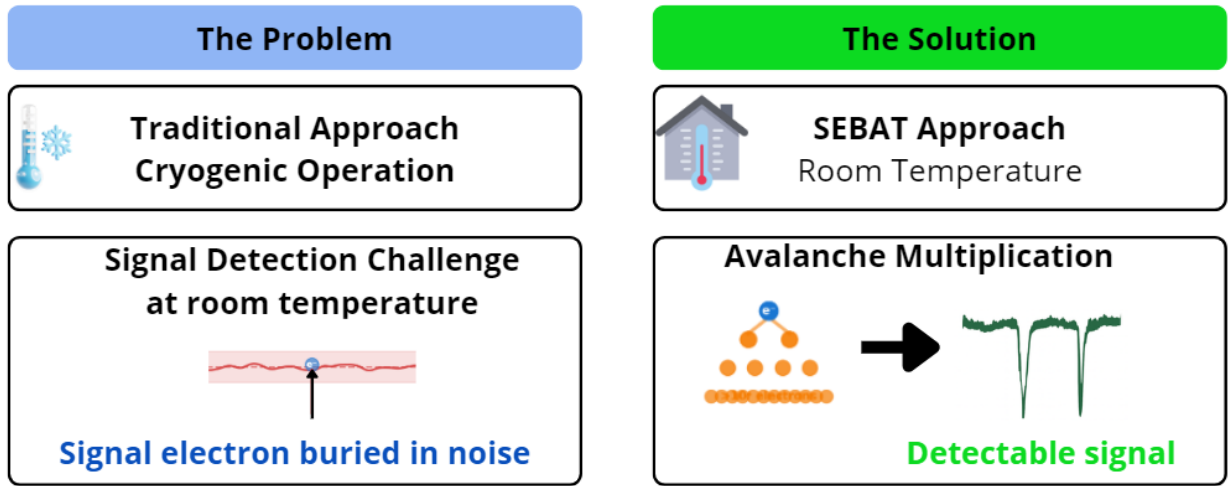


Fig. 1-6. Single-Electron Detection: Problem vs Solution.

Single-electron detectors based on avalanche multiplication can be fabricated using silicon planar technology, derived from the structure of Single-Photon Avalanche Diodes (SPADs). Given their shared operational principles, the next section first introduces the SPAD architecture before detailing the development and characteristics of the single-electron detector.

1.11. Single-Photon Avalanche Diode Technology

SPADs are advanced semiconductor devices that have attracted considerable interest due to their suitability for a broad range of applications, including Light Detection And Ranging (LiDAR), three-dimensional (3D) face recognition, gesture recognition, and space navigation [79]. Furthermore, SPADs have demonstrated exceptional potential in various biomedical imaging techniques, such as Fluorescence Correlation Spectroscopy (FCS), fluorescence lifetime imaging microscopy (FLIM), and Time-of-Flight (ToF) positron emission tomography (PET) [80], [81], [82]. For these applications, SPADs fabricated in complementary metal-oxide-semiconductor (CMOS) technology have a great advantage in terms of cost and the integration capability with electronics on the

same chip. CMOS-compatible SPADs enable monolithic integration of detector arrays with on-chip quenching circuits, time-to-digital converters, counters, and signal processing, eliminating bulky external electronics while leveraging mature fabrication processes for cost-effective, high-yield production [83], [84].

1.11.1 SPAD Structure

Fig. 1-7 shows the cross-sectional structure of a CMOS-integrated SPAD. The device features a p-well/deep n-well junction forming the primary avalanche diode structure. The multiplication region, located in the deep n-well beneath the p-well/deep n-well junction, constitutes the critical high-field zone where avalanche multiplication occurs. When properly biased above breakdown, the electric field in this region exceeds 3×10^5 V/cm [77], enabling single-photon detection through controlled avalanche breakdown processes. The fundamental difference between a conventional avalanche photodiode (APD) [85] and a SPAD lies in the bias voltage. APDs are biased below the avalanche breakdown voltage V_{BD} , inducing linear charge multiplication where the output signal remains proportional to input light intensity. In contrast, SPADs are biased well above V_{BD} in what is termed Geiger mode operation, analogous to a Geiger counter. This over-biasing creates conditions where a single photon can trigger a self-sustaining avalanche, producing a macroscopic current pulse that marks the photon detection event.

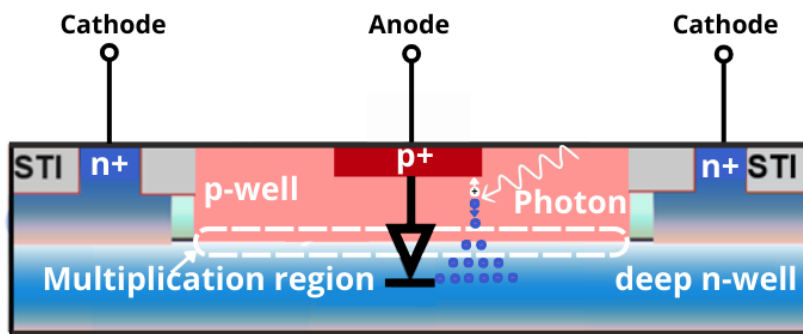


Fig. 1-7. Cross section of the structure of a SPAD.

1.11.2 SPAD Operating Principle

The SPAD operation proceeds through a cyclic sequence, as illustrated in Fig. 1-8. The device is connected in series with a quench resistor R_{quench} that enables passive quenching of the avalanche current:

- **Initial State (Point 1):** The SPAD is biased at a voltage V_S , which exceeds the breakdown voltage V_{BD} by the excess bias V_{EX} . In this quiescent state, no current flows through the device, and the full bias voltage appears across the p⁺/deep n-well junction.
- **Photon Detection and Avalanche Triggering (Point 1 → Point 2):** When a photon enters the device through the anode, it is absorbed in the p-well or multiplication region, generating an electron-hole pair. The high electric field in the multiplication region accelerates these carriers, initiating impact ionization. Since the bias exceeds V_{BD} , this ionization process becomes self-sustaining: both electrons and holes generate additional carrier pairs through impact ionization, creating a positive feedback mechanism. The avalanche current rises rapidly to macroscopic levels (milliampere range), producing a detectable current pulse.
- **Quenching Phase (Point 2 → Point 3):** The avalanche current $I_{avalanche}$ flowing through the quench resistor R_{quench} generates a voltage drop $I_{avalanche} \times R_{quench}$. This voltage drop reduces the bias across the SPAD junction. When the junction voltage falls below the self-sustaining avalanche threshold (approaching V_{BD}), the multiplication process ceases and the avalanche is quenched. The quench resistor value is chosen such that during the avalanche, the resistor current is much smaller than the avalanche current, ensuring effective voltage reduction through capacitive discharge.

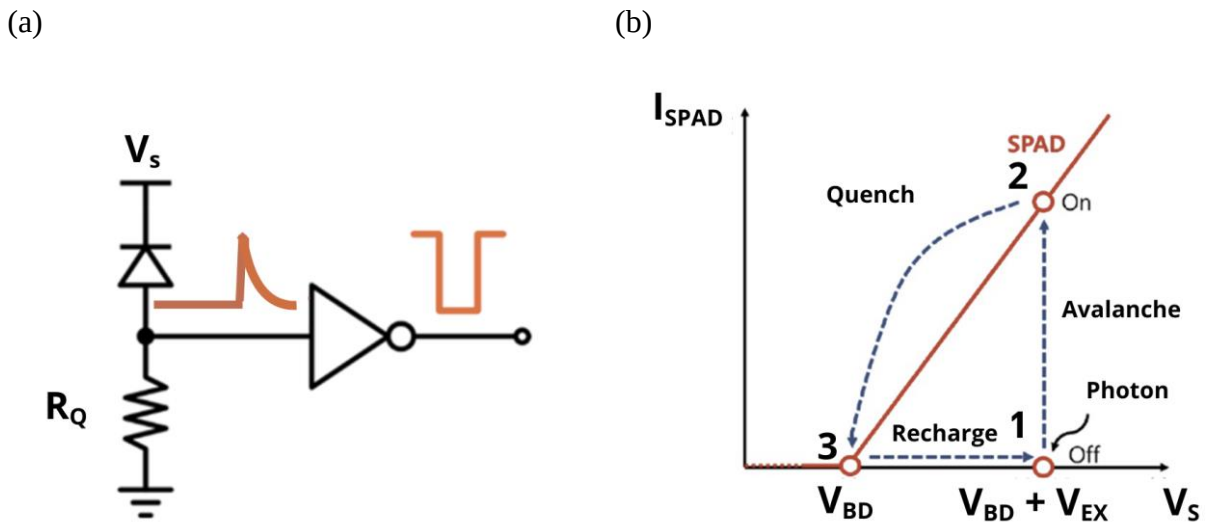


Fig. 1-8. SPAD Geiger Mode Operation: (a) Biasing Configuration, (b) Avalanche Multiplication Timeline

- **Recovery Phase (Point 3 → Point 1):** After quenching, the current through R_{quench} gradually recharges the junction capacitance, restoring the bias voltage to the initial value V_S .

The recharge time constant $\tau = R_q \times C_{\text{junction}}$ determines the dead time, the period during which the SPAD cannot detect subsequent photons and thus limiting the maximum counting rate of the device.

This Geiger-mode operation produces spike-like current pulses, with each pulse corresponding to the detection of a single photon. The binary nature of the output distinguishes SPAD operation from linear-mode APDs and enables true single-photon counting capability. The leading edge of the avalanche pulse marks the photon arrival time with 10-100's picosecond jitter, making SPADs suitable for applications requiring both single-photon sensitivity and precise timing information

1.11.3 Dark Counts: Primary Noise Source

Dark counts represent the primary noise limitation in SPAD operation, arising from avalanche events triggered in the absence of incident photons. These spurious detection events, quantified as the dark count rate (DCR), originate from four physical mechanisms: thermal generation of electron-hole pairs, trap-assisted thermal generation from crystal defects, trap-assisted tunneling in the presence of interface states, and direct band-to-band tunneling enabled by the strong electric field in the multiplication region [83].

DCR exhibits strong dependence on excess bias voltage and technology node. Advanced CMOS technologies employ higher doping concentrations that create narrower depletion widths, resulting in increased band-to-band tunneling contributions and higher DCR [86]. Experimental characterization of CMOS SPADs in 110nm technologies demonstrates normalized DCR ranging from 0.4 to 585 cps/ μm^2 depending on device structure and fabrication optimization, with typical values of 2-10 cps/ μm^2 for optimized deep-junction implementations at moderate excess bias (1-2V) [87].

The DCR also exhibits strong temperature dependence, typically decreasing by factors of 2-3 per 10°C cooling due to reduced thermal generation [77]. Dark counts follow Poisson statistics as shown in Fig. 1-9, appearing as randomly distributed events with exponential inter-arrival time distributions. This random, uncorrelated nature distinguishes dark counts from afterpulsing effects, which exhibit temporal correlation with preceding avalanche events, as discussed in Section 1.11.4.

1.11.4 Afterpulsing in SPADs: Mechanisms and Impact

Afterpulsing occurs when charge carriers, trapped during an avalanche event, are later released and trigger spurious avalanches, resulting in false counts. The probability and timing of afterpulses

depend on trap density, carrier lifetime, temperature, and device structure. Afterpulsing is a correlated noise source, distinct from random dark counts, and is especially problematic at high count rates or short dead times. The characterization of afterpulsing is typically performed through analysis of output pulses from the SPAD under dark conditions at controlled temperatures. A common and efficient method involves evaluating the inter-arrival times between successive detection events [88], [89]. By plotting amplitude versus inter-arrival time and constructing histograms of the inter-arrival time distribution, as shown in Fig. 1-9, primary dark counts can be separated from correlated noise contributions. The primary dark count rate is extracted by fitting the long inter-arrival time tail of the distribution; where afterpulsing contributions are negligible—with an exponential function. The deviation between measured data and this exponential fit at short inter-arrival times quantifies the afterpulsing probability and characteristic time constants, enabling complete characterization of this correlated noise component [90].

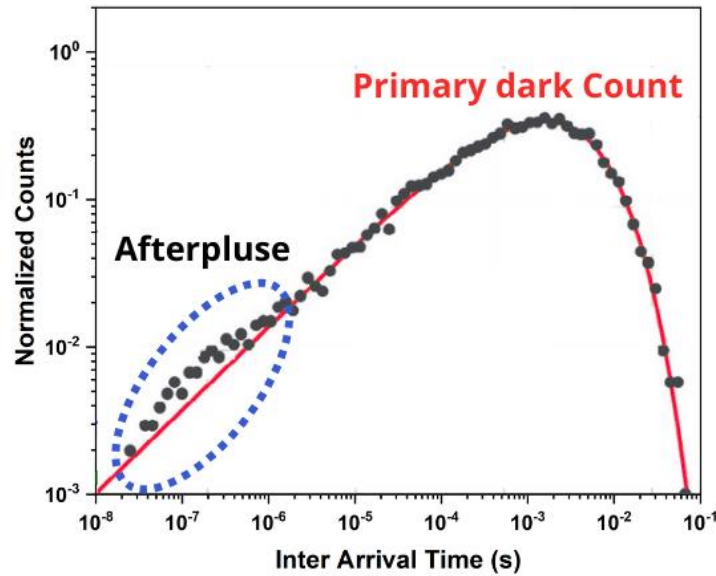


Fig. 1-9. Histogram of the inter-arrival time shows the afterpulsing.

1.12. SEBAT Fundamentals and Prior Work

The Single-Electron Bipolar Avalanche Transistor (SEBAT), shown in Fig. 1-10, is a semiconductor device designed for room-temperature single-electron detection applications. The device architecture integrates the fundamental structure of a bipolar junction transistor with the avalanche multiplication region characteristic of avalanche photodiodes [91].

The device features a vertical NPN structure: the n^+ injector (n-inj) acts as the emitter, the p-well forms the base, and the deep n-well serves as the collector. This configuration enables the detection of individual charge carriers through controlled avalanche while maintaining compatibility with standard CMOS fabrication technologies. The SEBAT operation principle relies on avalanche multiplication triggered by single-electron injection events. Electrons injected through the base-emitter junction initiate impact ionization within the base-collector depletion region when the device is biased in Geiger-mode [92].

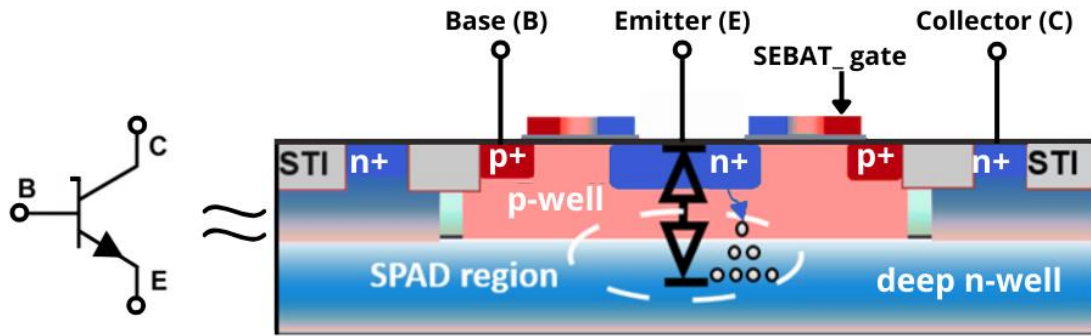


Fig. 1-10. Cross-section of a SEBAT implemented in 150nm CMOS.

Electrons injected through the base-emitter junction initiate impact ionization within the base-collector depletion region when the device is biased in Geiger-mode [92]. The key performance metric of the SEBAT is the Electron Detection Efficiency (EDE), defined as:

$$\text{EDE} = \frac{\text{Count Rate}}{I_E/e} \quad 1-3$$

where Count Rate (s^{-1}) is the measured avalanche pulse rate at the collector output, I_E is the emitter current measured, and e is the elementary charge.

1.13. SEBAT Geiger Mode Operation

The SEBAT operates in Geiger mode analogous to a SPAD, with a critical distinction: while the SPAD detects photons through their direct absorption in the avalanche region, the SEBAT detects charge carriers injected through the emitter-base junction. The device structure, as shown in Fig. 1-11, features a vertical NPN bipolar transistor with the base-collector junction biased above

breakdown voltage. The modified symbol, with a bar on the base terminal, distinguishes the SEBAT from a conventional NPN transistor.

The operational cycle mirrors SPAD behavior: (1) the device awaits an injection event in the quiescent state with voltage exceeding V_{BD} , (2) either an absorbed photon or an injected electron triggers self-sustaining avalanche multiplication through impact ionization, producing a macroscopic current pulse, and (3) a quenching resistor terminates the avalanche by reducing the collector voltage below V_{BD} , followed by capacitive recharge to restore the initial bias. The photon detection mechanism is identical to SPADs, with photogenerated carriers in the high-field region initiating avalanche breakdown. However, the additional electron injection capability through the emitter-base junction distinguishes SEBAT operation. This injection can be modulated externally, enabling the SEBAT to function as an electron-counting device for applications ranging from radiation detection to signal digitization. For electron-counting applications, photon-triggered avalanches constitute an intrinsic noise source, generating spurious counts indistinguishable from electron injection events. To ensure reliable operation, the SEBAT sensitive area is covered with opaque metal layers, blocking incident photons while preserving electron injection functionality through the emitter terminal. The key advantage of this architecture is the separation of signal transduction and avalanche amplification: the emitter acts as an electron injector (which can be coupled to various sensors like FET detectors), while the base-collector junction provides avalanche multiplication and pulse generation for both photon-generated and externally-injected carriers.

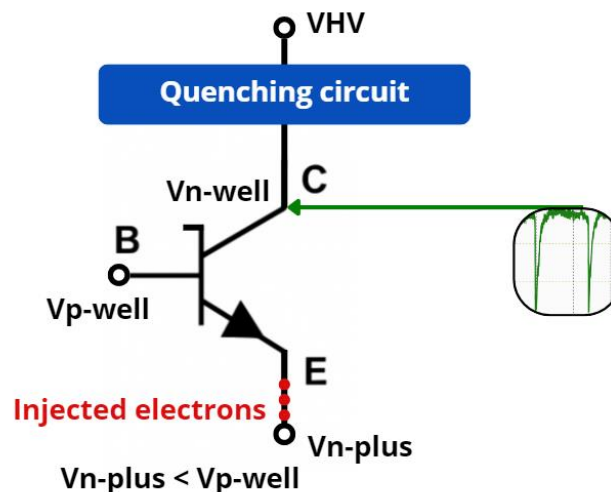


Fig. 1-11. Biasing configuration of a SEBAT in Geiger mode operation.

The avalanche current resulting from an electron detection, subsequently quenched through external circuitry, produces discrete voltage pulses corresponding to individual electron detection events. This operational mode transforms analog current signals into digital pulse trains, facilitating direct interface with digital processing circuits. The experimental characterization of early SEBAT implementations demonstrated the feasibility of single-electron detection at room temperature [9].

1.14. Research Objectives and Scope

Infrared and terahertz (IR-THz) detection technologies enable applications across multiple sectors. In healthcare, THz imaging can identify cancerous tissue margins during surgery and detect skin cancer non-invasively. Manufacturing quality control benefits from THz's ability to detect structural defects, measure coating thickness, and identify material composition without damaging samples. Security applications include detection of concealed weapons and explosives through clothing and packaging. However, widespread adoption requires detection systems that combine sensitivity, room-temperature operation, and integration with standard electronics at practical cost points.

A particularly promising approach involves integrating FET-based THz detectors with Single-Electron Bipolar Avalanche Transistor (SEBAT) readout systems. This combination leverages mature semiconductor fabrication technologies while potentially providing the sensitivity needed for practical IR-THz applications. FET-based detectors can operate at room temperature and integrate with standard electronics, while SEBAT technology promises to amplify weak THz-generated signals to easily detectable levels through avalanche multiplication of individual electrons. The detailed operating principle and integration mechanism are presented in Chapter 2.

While early implementations in $0.35\mu\text{m}$ CMOS nodes suggest that SEBAT-based systems should achieve electron-to-pulse conversion efficiencies approaching 70% [9], recent experimental implementations in deep-submicron processes have demonstrated efficiencies on the order of 10^{-4} [8], a degradation of nearly four orders of magnitude compared to what was previously achieved. This performance gap represents a fundamental barrier to achieving practical IR-THz detection systems. Understanding and solving this efficiency problem requires comprehensive modeling approaches that can handle the complex physics in SEBAT operation. Analytical methods can't properly model how avalanche multiplication, charge transport, and parasitic effects work together in these devices. TCAD simulation can model these complex processes accurately, providing the insights needed for systematic optimization.

Building upon previous work that demonstrated the fundamental viability of SEBAT-based THz and IR detection, this thesis focuses on three primary objectives that make significant contributions to the field:

- A comprehensive simulation framework, including both TCAD and SPICE models, was introduced. These models capture the transient behavior of SEBAT devices, including the effects of parasitic elements on detection efficiency, providing design tools for optimization and circuit integration.
- . Following the modeling and experimental analysis, we identified key parasitic elements that degrade performance and introduced modified SEBAT architectures, leading to improved electron-to-pulse conversion efficiency and signal-to-noise ratio with respect to previous deep-submicron SEBAT implementations.
- Three distinct detector arrays have been designed and fabricated, optimized for different spectral regions: THz detection at 900 GHz and 1.5 THz, and IR detection. This chip design demonstrates the versatility of the SEBAT-based FET detection approach across a broad range of frequencies and applications.

This thesis is organized as follows. Chapter 2 presents the theoretical framework and modeling methodology for SEBAT devices, including TCAD simulation development and SPICE model validation. Chapter 3 describes the experimental implementation and characterization of optimized SEBAT structures, analyzing the impact of parasitic elements on detection efficiency. Chapter 4 details the design and implementation of a test chip with 3 different imaging arrays, including the architecture of detector arrays for 900 GHz, 1.5 THz, and IR. Chapter 5 concludes the thesis with a summary of contributions and recommendations for future work.

Chapter 2

2. SEBAT Modeling and Characterization

Building upon the SEBAT operating principles introduced in Chapter 1, this chapter presents the characterization and modeling of a SEBAT test device fabricated in 150 nm CMOS technology to identify the physical mechanisms limiting electron-to-pulse conversion efficiency. The work employs TCAD transient simulations and SPICE compact modeling validated against experimental measurements, focusing specifically on parasitic circuit elements and contact design effects that dominate device performance. DC characterization through Gummel plot analysis and forward-bias I-V measurements provides parasitic resistance extraction from the fabricated device. Transient TCAD simulations reveal the coupling between base parasitic resistance, collector capacitance, and electron injection dynamics during avalanche operation. The validated SPICE compact model captures these effects and enables circuit-level optimization studies. This analysis establishes the optimization framework applied in subsequent chapter, demonstrating that minimizing base parasitic resistance through contact area optimization and reducing collector parasitic capacitance are essential requirements for achieving practical SEBAT performance in THz detection applications.

2.1. Device Physics and Operation Principles

2.1.1 Device Under Test: THzSET Implementation

This work experimentally characterizes a THz Single-Electron Transistor (THzSET) fabricated in 150 nm CMOS technology, which integrates a THz FET detector with a custom-designed SEBAT (cross-section shown in Fig. 1-10) [68], operating as described in Chapter 1 with the base-collector junction biased above breakdown voltage ($V_{BD} \approx 19.5$ V) to enable avalanche multiplication triggered by single-electron injection. The THzSET achieves power-to-frequency conversion: the incident THz radiation gathered by the antenna and fed into the FET detector, generates a constant current in the transistor channel proportional to the impinging power, which injects electrons into the SEBAT. Each injected electron triggers an avalanche pulse, enabling direct conversion of incident THz power into a pulse rate. This direct digital conversion eliminates large-area analog

readout chains, reducing power consumption and circuit complexity. The compact SEBAT footprint ($27 \times 22 \mu\text{m}^2$) compared to conventional analog readout chains enables high-density pixel arrays; a critical advantage for multi-pixel array integration.

The SEBAT is a three terminal device, with the emitter connected directly to the FET detector, thus, the characterization is performed by sweeping both base (p-well) and collector voltages. The base voltage controls electron injection through the emitter-base junction, while the collector voltage (VHV) applied through an external quenching resistor, sets the avalanche multiplication condition. The polarization of the FET detector changes its drain-source resistance, which appears in series with the SEBAT injector as it is shown in Fig. 2-1, this can vary the SEBAT polarization condition. The experimental characterization addresses multiple device parameters: (1) base-collector breakdown voltage V_{BD} , which determines the Geiger-mode operating point, (2) base parasitic resistance R_p , extracted from forward-bias I-V measurements, (3) electron-to-pulse conversion efficiency, defined as the ratio of counted pulses to injected electrons and serving as the primary performance metric, (4) dark count rate (DCR), representing spontaneous avalanche events that establish the noise floor, and (5) maximum achievable count rate, limited by junction recharge dynamics. Collector parasitic capacitance C_{pc} is extracted from layout, providing accurate value; this value is validated through TCAD transient simulations matching experimental pulse characteristics.

2.1.2 THzSET Architecture

The THzSET consists of three integrated components (Fig. 2-1):

1. An NMOS transistor with bow-tie antenna (300 GHz) as a THz detector.
2. The custom SEBAT that converts detector current into avalanche pulses.
3. The readout circuitry that counts pulses.

In this configuration, the avalanche pulse rate directly encodes the THz signal intensity, enabling direct digitization without intermediate amplification stages.

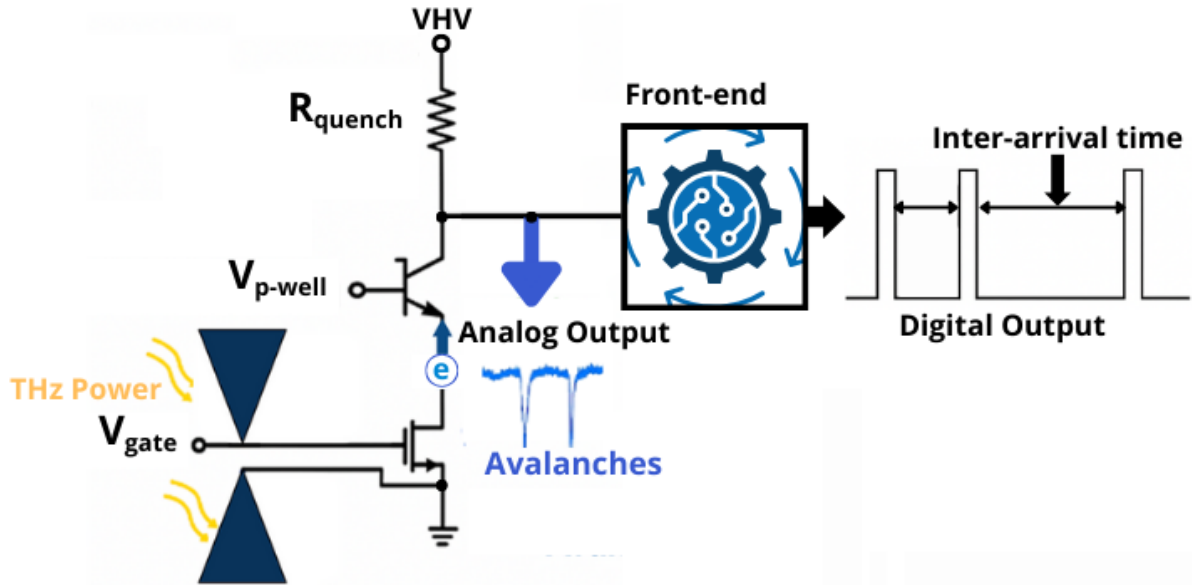


Fig. 2-1. THz Single-Electron Transistor (THzSET): Three-Component Integration for Direct THz Detection and Digital Conversion.

The test structure was implemented in a commercial 150 nm CMOS process, with the FET detector positioned at the center of the antenna structure and the SEBAT covered by metal to shield unwanted light-dependent pulse generation [64].

The microphotograph of the implemented test structure is shown in Fig. 2-2. Although specifically designed for THz radiation sensing, all voltages can be externally controlled, making this device suitable as a comprehensive test bench for characterization of the main device characteristics.

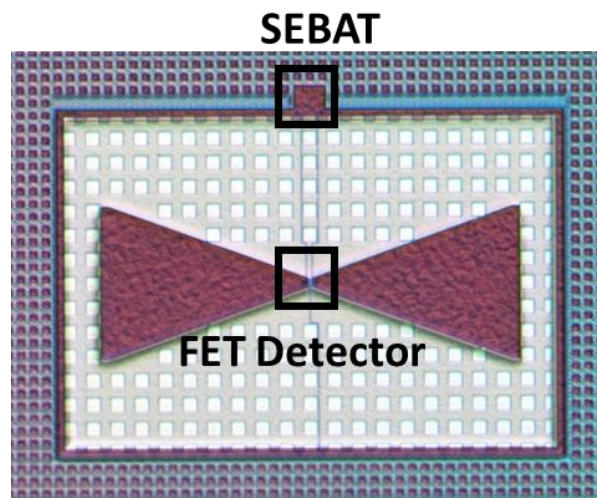


Fig. 2-2. Microphotograph of the implemented SEBAT in 150nm CMOS technology [64].

2.1.3 Efficiency Limitations and Underlying Mechanisms

The SEBAT tested by Lany et al. [9] achieved $\sim 70\%$ electron-to-pulse conversion efficiency, establishing the feasibility of room-temperature single-electron detection in avalanche bipolar transistors. However, subsequent implementations in deep sub-micron CMOS technologies exhibited severe efficiency degradation. Webster et al. reported avalanche pulse rates approximately 10^4 times lower than injected electron rates in 90 nm CMOS implementations [93]. Similarly, Perenzoni [8] observed injector efficiencies as low as $2 \times 10^{-40}\%$ in THz detection applications.

Initial explanations attributed this inefficiency to electron recombination in the base region [94]. However, recombination alone cannot account for efficiency losses of this magnitude in the thin base regions ($\sim 1 \mu\text{m}$) of modern CMOS processes, where carrier transit times are on the order of picoseconds. Comprehensive TCAD modeling [95] and the experimental characterization presented in this chapter reveal that parasitic circuit elements, specifically base parasitic resistance (R_p) and collector parasitic capacitance (C_{pc}) are the dominant mechanisms responsible for efficiency degradation.

2.2. Test Devices and Experimental Results

The fundamental objective of this experimental characterization is to quantify electron detection efficiency (EDE, Eq. 1-3) on the previously fabricated chip by comparing electron injection rates measured in linear mode with avalanche pulse detection rates recorded in Geiger mode. This approach enables direct correlation between the DC injector current (proportional to electron flow rate) and the count rate (number of detected avalanche events), providing a quantitative measure of how effectively injected electrons trigger avalanche breakdown. By measuring both quantities across identical voltage ranges and for multiple FET gate bias conditions, we extract the electron detection efficiency (EDE) as their ratio, thereby validating theoretical predictions and identifying performance limitations across different detector operating conditions.

2.2.1 Geiger Mode Characterization

Geiger mode characterization (Fig. 2-3) requires an external series resistor ($R_{\text{quench}} = 10 \text{ M}\Omega$) connected to the collector to provide passive quenching of avalanche events. The collector-base junction was biased at 2.5 V excess bias above the breakdown voltage, with the collector held at approximately 22 V. The device was maintained in dark conditions to eliminate photon-induced events. Avalanche pulses generated by electron injections were detected using a high-speed oscilloscope connected to a sensing resistor of $10 \text{ k}\Omega$ in series with the quenching circuit. The avalanche

pulse waveforms were acquired and processed offline to extract the pulse count rate as a function of base-emitter (p-well / n-inj) voltage. Measurements were recorded for each FET gate voltage condition ($V_{\text{gate}} = 0 \text{ V}$, 0.2 V , 0.4 V , 0.6 V , and 1.8 V) to characterize how the FET impedance affects avalanche detection performance across the full range of detector operating conditions.

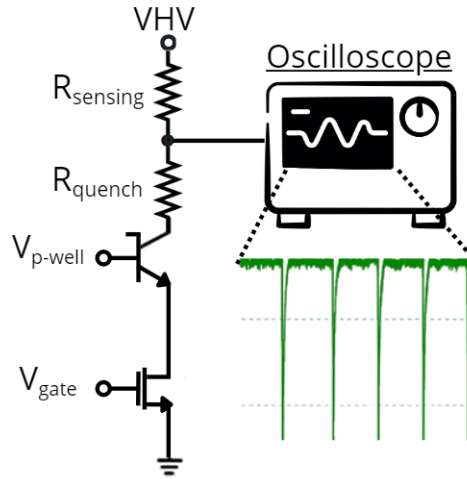


Fig. 2-3. SEBAT Characterization Circuit: Linear and Geiger Mode Configurations with External Resistor Quenching

The electron injection process follows Poisson statistics, as demonstrated by the exponential distribution of inter-arrival times (Fig. 2-4).

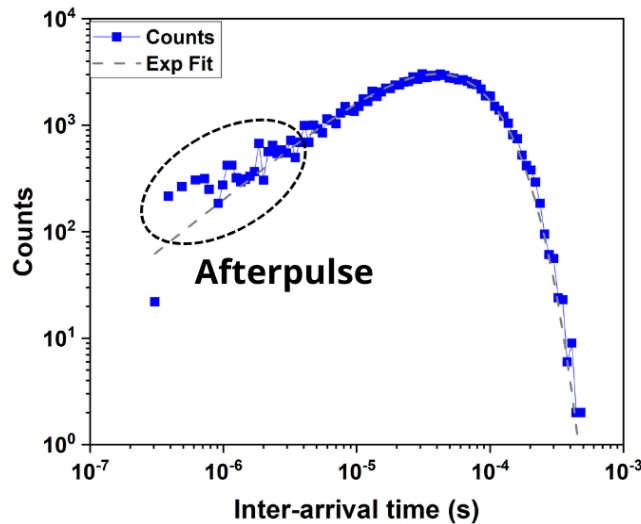


Fig. 2-4. Histogram of the inter-arrival times (horizontal log scale and log bins), with the exponential fitting of the primary events.

An exponential fit to the histogram (measured at $V_{\text{gate}} = 1.8 \text{ V}$ and $V_{\text{p-well/n-inj}} = 240 \text{ mV}$) shows good agreement for intervals larger than $3 \mu\text{s}$, while shorter intervals exhibit an excess of events attributed to afterpulsing; correlated avalanche events occurring shortly after the primary pulse due to trapped carriers released from defects in the multiplication region, as described in detail in Chapter 1.

Fig. 2-5 displays the inter-arrival time statistics plotted on logarithmic scales under two different gate bias conditions: $V_{\text{gate}} = 1.8 \text{ V}$ and $V_{\text{gate}} = 0 \text{ V}$. With the FET is fully ON at 1.8 V gate bias (Fig. 2-5 (a)), higher p-well (base) / n-inj (emitter) voltages result in distributions that shift toward shorter inter-arrival times, reflecting increased electron injection rates. In contrast, when the gate voltage is set to 0 V (Fig. 2-5 (b)), the distributions appear distorted and cannot be fitted with exponential characteristics. This deviation occurs because the FET channel resistance dominates the total series resistance (R_{inj}) feeding the SEBAT emitter. A small-signal equivalent circuit model including R_{inj} and all relevant parasitic elements is presented in Section 2.4 (Fig. 2-18). When the FET gate is biased at 0 V , the channel resistance becomes extremely high ($\text{G}\Omega$ range), making the emitter node effectively isolated from the bias voltage source.

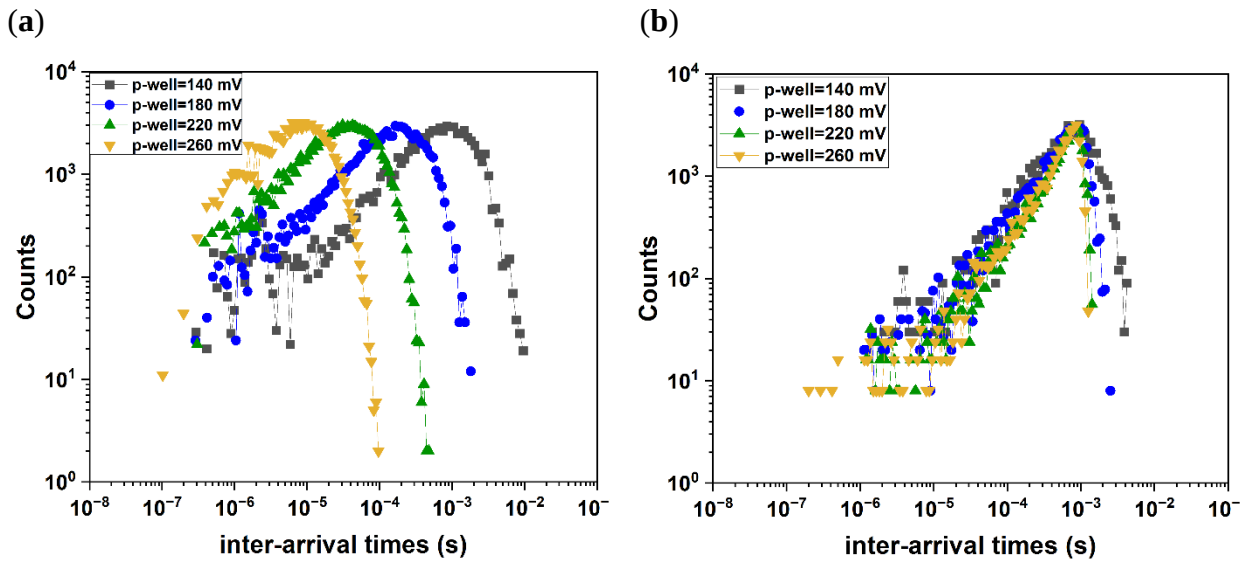


Fig. 2-5 Count rate as a function of the inter-arrival time for different values of the P-well voltage; a) $V_{\text{gate FET}}=1.8\text{V}$, b) $V_{\text{gate FET}}=0\text{V}$.

During each avalanche event, the large transient avalanche current flows through the base parasitic resistance (R_{p}), creating a voltage drop that temporarily increases the forward bias of the base-emitter junction. This enhanced forward bias causes multiple electrons to be injected from the

emitter during the avalanche. After the avalanche quenches, the emitter-base capacitance (C_{inj}) must recharge through the high series resistance (R_{inj}) to restore the original bias point.

The observed difference in inter-arrival time statistics between gate bias conditions suggests distinct recharge dynamics. When the gate voltage is set to 1.8 V (fully ON), the FET provides a low-resistance path ($R_{inj} \approx 2.7 \text{ k}\Omega$), which we hypothesize enables rapid restoration of the emitter bias after each avalanche event ($\tau \sim \mu\text{s}$), maintaining stable injection conditions consistent with the observed Poisson statistics. This hypothesis is supported by TCAD transient simulations presented in Section 2.3.6, which quantitatively demonstrate the relationship between R_{inj} and injection stability.

2.2.2 Linear Mode I-V Characterization

The linear mode characterization (Fig. 2-6.) was performed using a custom motherboard that provides external voltage control for device biasing. The FET gate was biased at 1.8 V, placing the FET in the fully ON state and grounding the n-inj (injector) node through the FET source. The forward bias of the p-well/n-inj junction was established by applying a positive voltage sweep from 0.0 V to 0.8 V to the p-well base terminal using a trimmer potentiometer on the motherboard. The collector (deep n-well) was held at 5 V (below breakdown voltage to avoid impact ionization). The collector current I_C ($I_{\text{deep n-well}}$ in the SEBAT case) was measured as a function of the applied base voltage. Due to the motherboard measurement configuration, only the collector current I_C could be directly measured. The base terminal (p-well) is biased through a trimmer potentiometer on the motherboard, which provides voltage control but does not allow current measurement without breaking the bias path. Similarly, the emitter (n-inj) is connected to the FET drain with no accessible current sensing point in the circuit path.

To extract the emitter current from the measured collector current, the bipolar transistor relationships were employed using parameters from the stand-alone test structure (Section 2.3.3). The common-emitter current gain $\beta \approx 10$ was extracted from DC characterization. Using the common-base gain:

$$\alpha = \frac{\beta}{1 + \beta} \approx 0.9$$

The emitter current was calculated from the measured collector current as:

$$I_E = \frac{I_C}{\alpha}$$

The average electron injection rate (electrons per second) was then obtained by:

$$\text{Injection rate [eps]} = \frac{I_E}{e}$$

where $e = 1.602 \times 10^{-19} \text{ C}$ is the elementary charge.

The average electron injection rate, obtained from the emitter current measured in linear mode (collector biased at 5 V, below breakdown), is then compared with the avalanche count rate measured separately in Geiger mode (collector biased at 22 V, above breakdown), both as a function of the same p-well/n-inj voltage, to extract the EDE (Fig. 2-7).

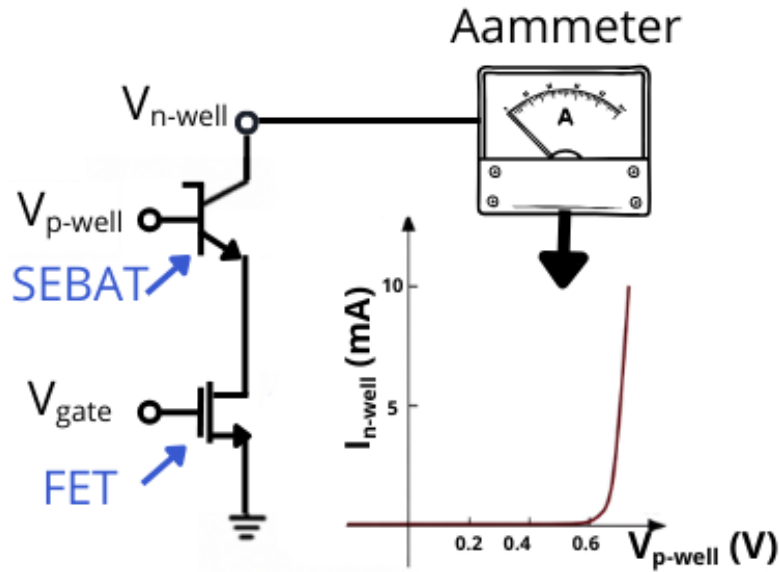


Fig. 2-6. SEBAT Linear Mode Characterization Circuit.

Fig. 2-7 shows the electron flow rate of the emitter in linear operation, calculated from the I-V curves, and the output pulse rate measured for the SEBAT as a function of the applied base-emitter (p-well/n-inj) voltage. When the gate voltage is larger than 0.2 V, the count rate increases exponentially with the applied p-well/n-inj voltage, as expected from the diode I-V characteristics. In contrast, when the gate voltage is set to 0 V, a significantly larger p-well/n-inj voltage is required to achieve the same count rate. This shift is attributed to voltage division across the high FET

channel resistance, though direct measurement of the FET voltage drop was not accessible in this configuration, consistent with the high FET channel resistance discussed previously.

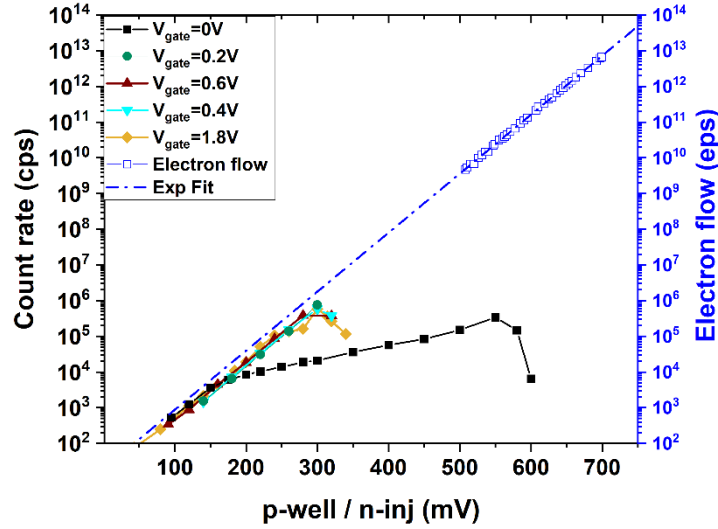


Fig. 2-7. Count rate measured on the SEBAT in the Geiger mode and electron flow rate estimated from the emitter current in linear mode.

The analysis utilized regression of experimental data points in the linear region where the PN junction exhibits an ideality factor close to 1, corresponding to ideal diode behavior. This regression approach was employed to estimate the electron flow rate at lower base-emitter (p-well / n-inj) voltages where direct current measurements are not reliable due to setup limitations, environmental noise, and packaging parasitics: at low applied voltages (typically below ~ 0.35 V), the measurement system cannot accurately resolve the collector current due to external leakage currents and interference that mask the true device signal. The exponential fit to data points measured in the reliable voltage region (where ideality factor ≈ 1) is therefore used to extrapolate the electron injection rate to lower voltages, enabling direct comparison with the Geiger mode count rate across the full measurement range.

Fig. 2-8 represents the zoomed version of Fig. 2-7 on the SEBAT counts. The EDE is extracted in the low-voltage exponential regime (p-well / n-inj < 150 mV), where both the count rate and the extrapolated electron flow rate follow the same exponential dependence and saturation effects are negligible. In this region, the ratio between the count rate and the extrapolated electron injection rate yields an electron detection efficiency of approximately 50% when the gate voltage is larger than 0.2 V. The efficiency is almost independent of the p-well / n-inj voltage until the saturation

point, which is around 300 mV, demonstrating relatively stable performance across the operational voltage range.

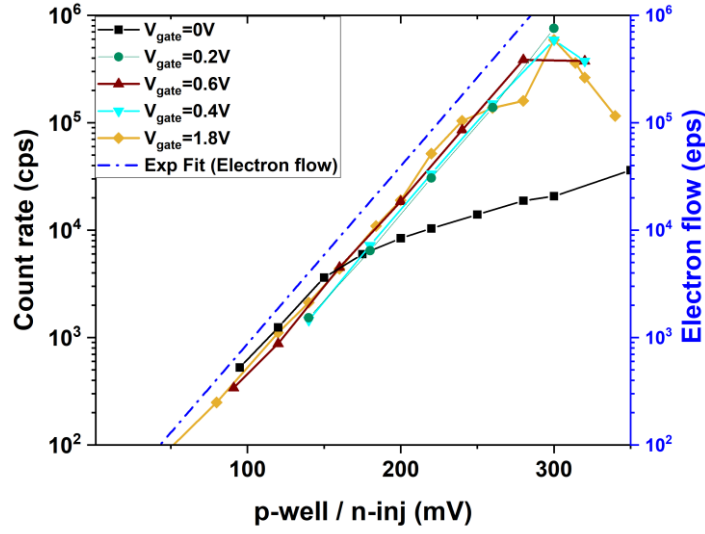


Fig. 2-8. Zoomed graph of the Count rate measured on the SEBAT in the Geiger mode and electron flow rate estimated from the emitter current.

2.3. TCAD Simulation Framework

2.3.1 Motivation and Simulation Approach

The linear mode characterization (Section 2.2.2) demonstrated 50% electron detection efficiency under continuous injection conditions, where the injection rate is estimated from the DC emitter current and the count rate is measured in Geiger mode. This efficiency therefore reflects the average injection-to-avalanche conversion under continuous carrier flow, not single-electron Geiger mode detection. However, Geiger-mode operation for single-electron detection exhibits substantially lower performance. Previous SEBAT-based THz detection implementations achieved electron-to-pulse conversion efficiencies of only $\sim 10^{-4}$ in Geiger mode [96], representing a four-order-of-magnitude degradation relative to linear mode. To identify the physical mechanisms responsible for this severe Geiger-mode efficiency loss and establish optimization pathways, comprehensive TCAD (Technology Computer-Aided Design) transient simulations and SPICE compact modeling were employed.

TCAD simulations provide the capability to analyze the internal device behavior during transient avalanche events, offering insights into the charge flow dynamics and the impact of parasitic elements that are difficult to observe experimentally. The simulation framework was designed to

model the complete THzSET system without the antenna, including both the semiconductor device physics and the external circuit elements. This mixed-mode (device-level physics simulation with circuit-level components) approach enables the investigation of how parasitic resistances and capacitances influence the device performance during avalanche multiplication events.

2.3.2 Physical Models and Simulation Domain

The TCAD simulations employ a drift-diffusion transport model, which provides adequate accuracy for the voltage and current ranges encountered in SEBAT operation while maintaining reasonable computational requirements. The physical models incorporated in the simulation include several key components essential for accurate avalanche device modeling. The carrier transport was modeled using doping-dependent mobility models that account for both lattice scattering and impurity scattering mechanisms. The Shockley-Read-Hall generation-recombination model was implemented with carrier lifetimes representative of typical CMOS imaging processes. High-field saturation effects were included to properly capture carrier behavior in the high-electric-field regions critical for avalanche initiation. The avalanche multiplication process was modeled using the Van Overstraeten and De Man impact ionization model, which provides good accuracy for silicon devices across the voltage ranges relevant to SEBAT operation. This model accounts for both electron and hole impact ionization, enabling proper simulation of the self-sustaining avalanche process. To balance simulation accuracy with computational efficiency, a two-dimensional simulation domain was constructed using cylindrical symmetry to approximate the three-dimensional device geometry. This approach is justified by the predominantly radial symmetry of the SEBAT structure. The simulation domain was carefully designed with an avalanche region diameter of $7.4\ \mu\text{m}$ and an injector diameter of $0.87\ \mu\text{m}$, matching the fabricated device dimensions. The TCAD model was developed based on the device layout and doping profiles provided by the foundry. Default values were used for most semiconductor parameters, with electron and hole lifetimes set to values representative of a typical CMOS imaging process. No additional fitting parameters were applied beyond those derived from the foundry-provided data.

2.3.3 Model Validation and Circuit Integration

Fig. 2-9 shows the Gummel plot of the SEBAT [97], i.e., the base and collector current measured as a function of the base-emitter voltage, where the emitter was grounded through the MOSFET biased in the fully ON state ($V_{\text{gate}} = 1.8\ \text{V}$), providing a low-resistance path to ground, and a positive voltage sweep was applied to the base ($V_{\text{p-well} / \text{n-inj}}$). This plot is widely used in the characterization of bipolar transistors to represent the device operation in DC conditions and was measured on a stand-alone test structure fabricated using the same $150\ \text{nm}$ CMOS process and the same

geometry as the SEBAT used in the complete THzSET detector. The TCAD model achieves a significant level of agreement with the experimental curves. From this plot, a common-emitter current gain β of approximately 10 was extracted. The parameter β represents the ratio of collector current to base current ($\beta = I_C / I_B$) and is visible in the plot as the slope difference between the collector and base current curves in the exponential region, providing a common-base current gain α of the order of 0.9. The common-base current gain α is defined as the ratio of collector current to emitter current ($\alpha = I_C / I_E$), related to β by the expression $\alpha = \beta / (1 + \beta)$, and indicates how efficiently the device collects injected electrons before recombination occurs. These parameters reflect the thin-base, high-collector-doping design optimized for avalanche operation rather than maximum current gain. The analysis was extended to show how the regression fit from the measured data compared against the simulation curve in the region down to approximately 0.35 V, where the exponential model remains valid for these PN junctions (the ideality factor is almost 1). As stated in Section 2.2.2, below 0.35 V, reliable direct measurements of the current could not be performed due to chip packaging and limitations in the measurement setup, where the device could not be properly shielded from environmental noise. The junction capacitances as a function of voltage were estimated from the TCAD simulation and were included in the model, since they are relevant for transient-mode operation.

The TCAD model demonstrates reasonable agreement with experimental measurements across the measurable voltage range, validating the simulation framework for subsequent transient analysis and optimization studies. The parameters of the SPICE model extracted from TCAD simulations and the corresponding Gummel plot validation are described in Section 2.4.

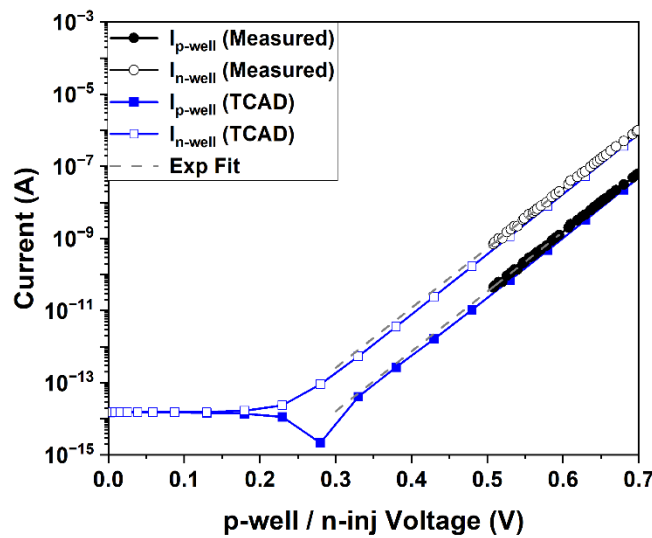


Fig. 2-9. Gummel plot of the SEBAT operated as a conventional bipolar transistor. Experimentally extracted characteristics are compared with the ones simulated with TCAD.

Following validation, the simulation framework was extended to include external circuit elements through a mixed-mode setup. This approach allows the semiconductor device simulation to be coupled with lumped circuit elements representing the parasitic and functional components of the complete system. Fig. 2-10 illustrates the cross-sectional view of the implemented SEBAT in 150 nm CMOS technology combined with the external lumped elements used in the mixed-mode simulations.

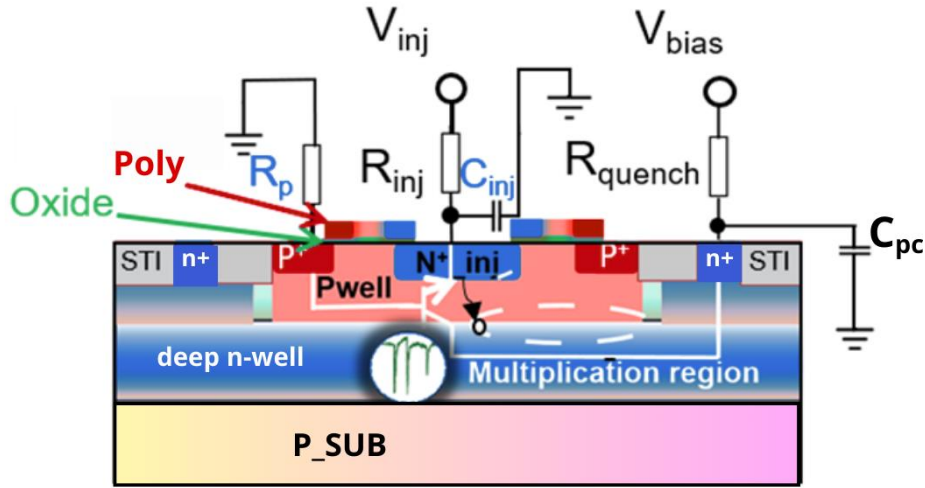


Fig. 2-10. Cross-section of the implemented SEBAT in 150nm CMOS combined with the external lumped elements.

The external circuit elements include several critical components that significantly influence device behavior. The base parasitic resistance (R_p) represents the series resistance encountered by current flowing to the base contact. This resistance includes contributions from both the semiconductor resistance and the contact resistance. The injector capacitance (C_{inj}) models the parasitic capacitance associated with the emitter contact and interconnect structures. The collector parasitic capacitance (C_{pc}) encompasses the pad capacitance, interconnect capacitance, and any external capacitance parallel to the quenching circuit. Additionally, the quenching resistance (R_{quench}) and the equivalent resistance of the signal source at the injector (R_e) were included as external elements. This comprehensive circuit representation enables investigation of how different parasitic values affect the device's transient behavior during avalanche events.

2.3.4 Parameter Extraction and Simulation Conditions

The parasitic element values were carefully determined through a combination of experimental extraction and layout-based estimation. Fig. 2-11 shows the SEBAT layout used for parasitic extraction, highlighting the main parasitic contributions that influence device performance. The layout analysis revealed that the primary resistive paths are dominated by the M2 metal layer connections to the n-well, p-well, and n+ terminals, while the capacitive contributions are mainly attributed to the analog pad structures.

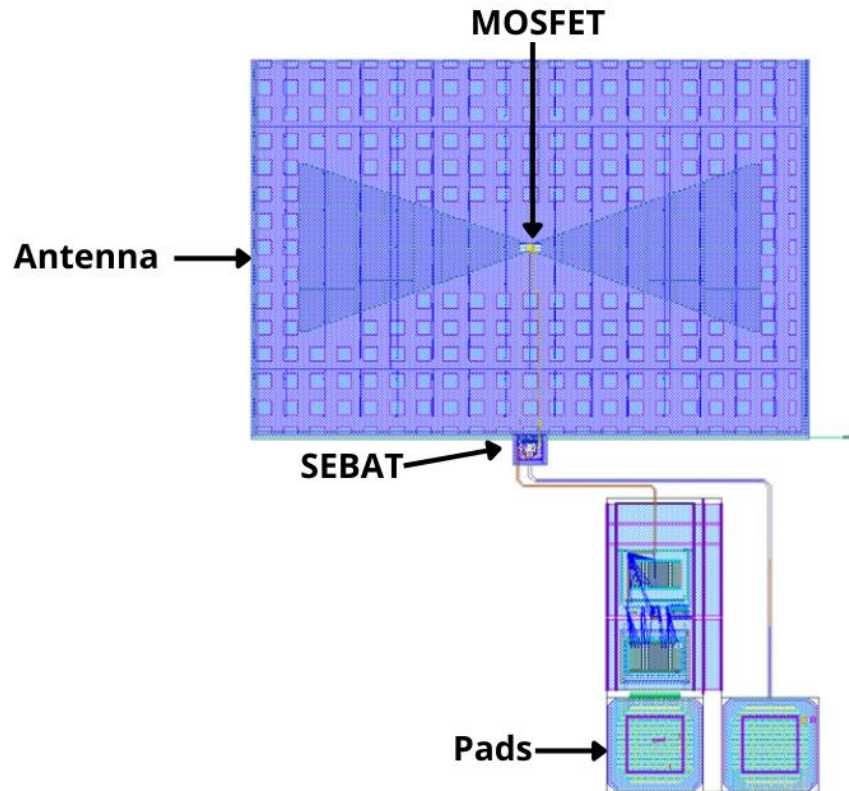


Fig. 2-11. SEBAT layout indicating parasitic resistances, capacitances, and external circuit components.

Fig. 2-12 presents the results of the parasitic extraction process, showing the equivalent circuit model with extracted resistance and capacitance values for each terminal. The parasitic extraction was performed using the Calibre PEX tool.

The extraction results show the n-well terminal with a resistance of $14\ \Omega$ and parasitic capacitance of $274\ \text{fF}$, while the p-well exhibits a resistance of approximately $21\ \Omega$ with $1.15\ \text{pF}$ capacitance. The n+ injector terminal demonstrates a resistance of $60\ \Omega$ and $21\ \text{fF}$ capacitance.

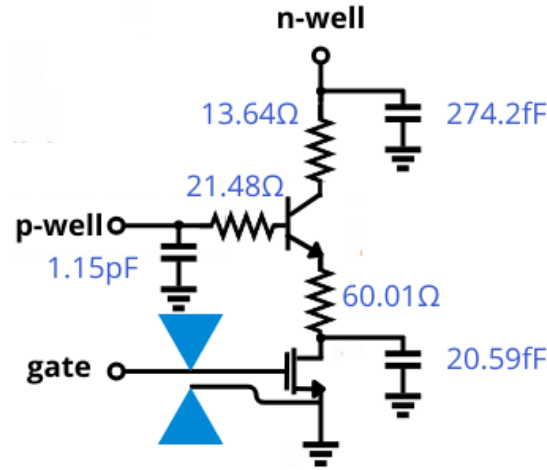


Fig. 2-12. Chip Parasitic Extraction of Integrated THzSET

These values were obtained from layout-based parasitic extraction using the PDK design tools, which compute resistance and capacitance from geometrical parameters and technology-specific layer properties rather than direct electrical measurement. The reported values therefore reflect the precision of the extraction tool output and should be interpreted as design estimates rather than experimentally verified quantities. It should be noted that the injector terminal is connected to the FET rather than directly to a pad, allowing for voltage control through the FET gatebias. The initial SEBAT devices implemented in 150 nm CMOS technology employed a two-contact base design with limited contact area not considering that this would have introduced extra parasitic resistance degrading the device performance. The devices were fabricated using the standard CMOS LFoundry LF15A process, where all contacts undergo silicidation as part of the standard process flow. While silicided contacts provide lower contact resistance than unsilicided alternatives, the relationship between contact resistance and avalanche operation performance has been documented in power MOSFET literature, where P-base contact resistance significantly impacts avalanche capability [99]. This motivated systematic investigation of contact design effects in SEBAT operation. Parasitic resistance extraction was performed through forward-bias I-V measurements on the base-collector junction. Since TCAD simulations estimated the semiconductor base resistance at approximately 10 Ω, the dominant contribution to total parasitic resistance arises from contact resistance. The two-contact configuration with limited contact area resulted in parasitic resistance, which became a key focus of the optimization study presented in Chapter 3.

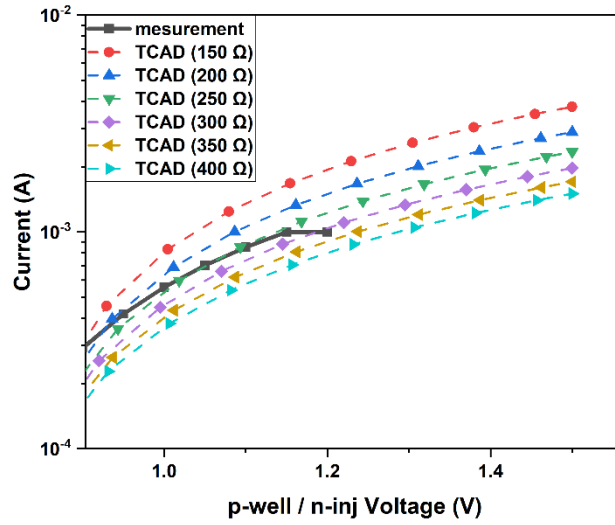


Fig. 2-13. Base Parasitic Resistance Extraction Validation: Experimental I-V Characteristics vs. TCAD Simulations with Varying Resistance Values.

Fig. 2-13 shows the comparison between experimental measurements and TCAD simulations with various resistance values ranging from 150 Ω to 400 Ω , along with the linear fit analysis used for resistance extraction. The analysis confirmed that the slope in the I-V curve above 0.9 V is primarily due to the series resistance (R_p) rather than high-injection effects, validating the resistance extraction approach.

Based on this analysis, the resistance extraction methodology was refined to use linear regression on the experimental I-V curve in the voltage range of 0.9V to 1.1V, where the series resistance dominates the curve slope. Further experimental characterization of the base resistance across multiple devices and measurement conditions was identified as necessary to establish the statistical distribution of this critical parameter and validate the modeling assumptions used in the TCAD simulations.

Experimental extraction was performed using forward-bias I-V measurements of the base-collector junction (Fig. 2-14). The measurement followed the configuration in Fig. 2-3, with the FET gate biased at $V_{gate} = 1.8$ V, which grounds the n-inj (injector) node through the low-impedance FET source. Under this condition, the measured parasitic resistance originates from the base-collector junction and represents the series resistance in the base current path. The collector parasitic

resistance is negligible in this measurement because the collector is a large area deep n-well contact ($400 \mu\text{m}^2$), and current flows from the base (small contact area) to the collector (large area), making the base resistance the dominant series element. The analysis of the I-V curve in the high-voltage region ($>0.9 \text{ V}$), where series resistance effects dominate, revealed a total base parasitic resistance of 357Ω .

Applying this linear regression technique to the experimental I-V characteristics yielded a base parasitic resistance value of $R_p = 357 \Omega$ extracted from the high-voltage linear region of Fig. 2-14. This extracted value represents the total resistance including both the semiconductor base resistance (estimated at approximately 10Ω from TCAD simulations) and the dominant contact resistance contribution. The relatively high resistance value can be attributed to the contact design constraints imposed by the avalanche device requirements.

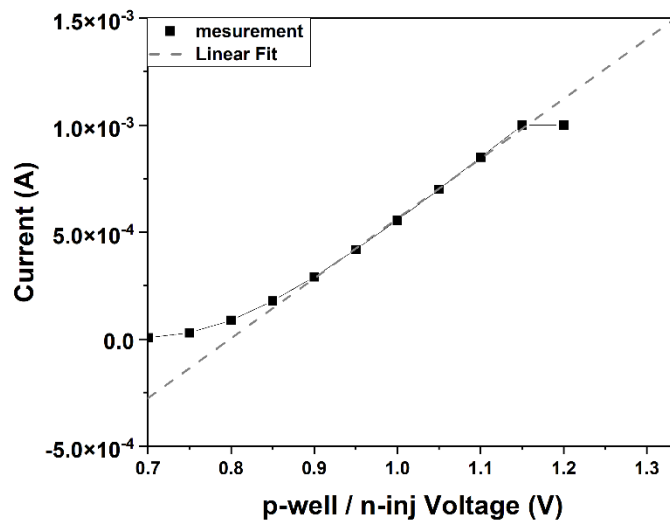


Fig. 2-14. SEBAT Base Resistance Determination: Linear Regression Analysis of Forward-Bias I-V Characteristics

The base parasitic resistance R_p is associated with the current path through the p-well contact, while the injector capacitance C_{inj} represents the parasitic capacitance at the n+ emitter terminal. The collector parasitic capacitance C_{pc} encompasses the capacitance at the deep n-well collector

connection, including external pad capacitances and interconnect parasitics, estimated at approximately 1 pF from PEX estimated.

To investigate the sensitivity to this parameter, simulations were performed with collector capacitance values ranging from 10 fF to 10 pF, and two base parasitic resistance values: the experimentally extracted value of 357 Ω and an optimized value of 10 Ω , representing different potential circuit configurations and contact designs.

The injector capacitance was estimated at 20 fF through parasitic extraction tools. The inclusion of the quenching resistance R_{quench} and the injector resistance R_{inj} completes the circuit representation, allowing investigation of how different external circuit configurations affect the SEBAT performance during avalanche multiplication events.

Table 2-1 summarizes the numerical values of all external lumped elements used in the mixed-mode TCAD simulations.

Table 2-1. Mixed-Mode TCAD Simulation Configuration: External Lumped Circuit Elements for SEBAT Avalanche Dynamics Analysis.

Symbol	Quantity	Value
R_p	Parasitic resistance at the p-well	357 Ω / 10 Ω
R_{inj}	External resistance at the injector	1k Ω – 100G Ω
C_{inj}	Parasitic capacitance at the injector	20fF
R_{quench}	Quenching resistance	10 M Ω
C_{pc}	Parasitic capacitance at the collector of the SEBAT	10fF-10pF

2.3.5 Simulation Setup and Bias Conditions

The simulation bias conditions were chosen to match the experimental operating points used in the THzSET characterization. The collector was biased at 22 V, providing sufficient excess bias above the breakdown voltage to ensure high triggering probability for injected electrons. The simulated breakdown voltage of 19.2 V demonstrated good agreement with the experimentally measured value of 19.5 V, confirming the accuracy of the device model and the validity of the physical parameters implemented in the simulation framework. Transient simulations were initialized with

quasi-static analysis to establish the steady-state bias conditions before triggering avalanche events. This approach ensures that the device reaches its equilibrium state under the applied bias voltages, providing a realistic starting point for the transient analysis. Avalanche events were then triggered through localized carrier generation in the high-field region, simulating the injection of individual electrons that initiate the avalanche multiplication process. The transient simulations capture the complete evolution of voltages and currents during avalanche events, including the initial triggering phase, the avalanche multiplication buildup, and the subsequent recovery phase. This comprehensive analysis enables detailed investigation of how the parasitic circuit elements influence each phase of the avalanche process and their cumulative effect on the overall device performance.

2.3.6 Simulation Results and Parasitic Effects Analysis

The TCAD transient simulations revealed significant insights into the mechanisms responsible for the poor electron-to-pulse conversion efficiency observed experimentally. The simulations demonstrated that the parasitic circuit elements play a dominant role in determining the actual charge injection characteristics during avalanche events, fundamentally altering the intended single-electron detection behavior. Fig. 2-15 presents the injected charge per pulse as a function of the collector parasitic capacitance, showing the dependence on parasitic parameters.

The results demonstrate that increasing C_{pc} from 10 fF to 10 pF results in the number of injected electrons per pulse increasing from less than 100 to the order of 10^5 when the base parasitic resistance R_p equals 357 Ω .

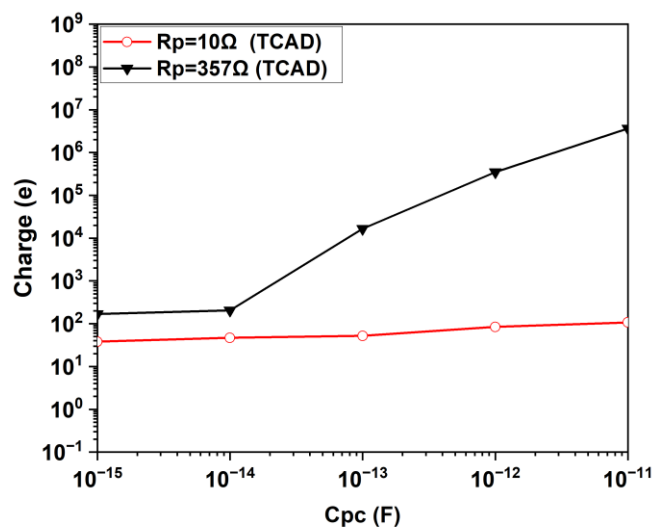


Fig. 2-15. Impact of parasitic elements on SEBAT charge injection: comparison of high and optimized base resistance values as function of collector capacitance.

This increase is not observed for optimized devices with low base resistance ($R_p = 10 \Omega$), highlighting the importance of minimizing the base parasitic resistance. The simulation results clearly indicate that large values of parasitic resistance and capacitance result in substantial instantaneous charge flow at the injector, producing significant inefficiency when the SEBAT is used for single-electron detection.

To understand the underlying physical mechanism responsible for this behavior, Fig. 2-16 shows the temporal evolution of the injector current during avalanche events for different values of collector parasitic capacitance. The plots reveal the effect of C_{pc} on both the duration and magnitude of the injector current pulses when $R_p = 357 \Omega$. As C_{pc} increases from 100 fF to 1 pF and then to 10 pF, the pulse duration extends significantly, and secondary current peaks appear. The current pulses at the injector stem from the increase in the forward bias of the base-emitter junction, which is caused by the avalanche current flowing into the parasitic resistance during the avalanche.

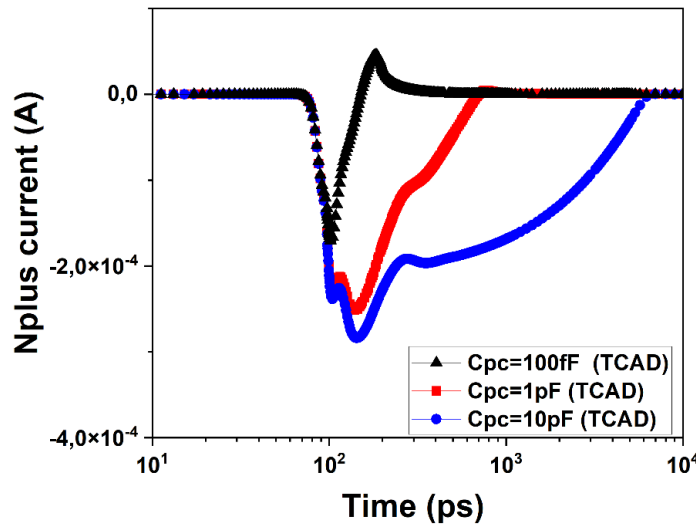


Fig. 2-16. TCAD transient analysis: injector current response to varying collector parasitic capacitance (100 ff to 10 pf) at $R_p = 357 \Omega$.

The root cause of this parasitic charge injection is revealed through analysis of the voltage evolution during avalanche events. Fig. 2-17 illustrates the p-well voltage transients that occur during the avalanche process for different values of collector parasitic capacitance.

The simulation results show how the p-well voltage evolves during an avalanche event, with distinct behavior depending on the parasitic capacitance value. For the lowest capacitance case ($C_{out} = 100 \text{ fF}$), the voltage transient is sharp and brief, reaching a peak around 0.7V and recovering quickly within approximately 40 ps.

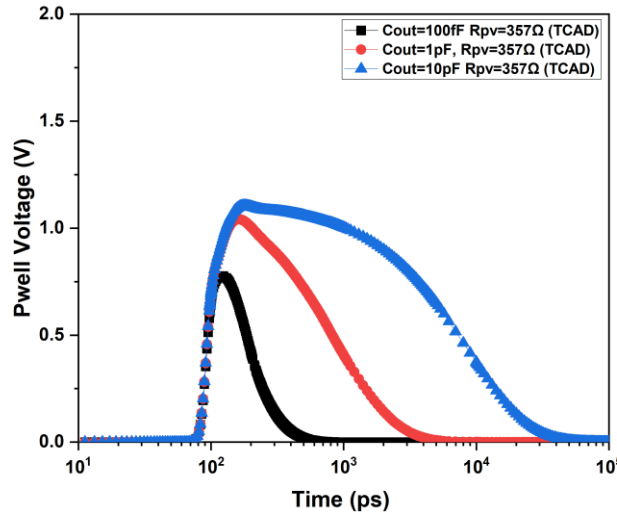


Fig. 2-17. P_{well} voltage transients during avalanche events: temporal evolution for different collector parasitic capacitance values at $R_p = 357 \Omega$.

As the collector capacitance increases to 1 pF, the voltage pulse becomes broader and reaches a higher peak value of approximately 1.1V, with a significantly longer recovery time extending to about 400ps. For the highest capacitance case ($C_{out} = 10$ pF), the voltage perturbation becomes even more pronounced, reaching over 1.2V and requiring approximately 0.1 μ s for complete recovery. During an avalanche event, the large transient current flowing through the parasitic base resistance creates these voltage drops that temporarily increase the forward bias of the emitter-base junction. This enhanced forward bias causes uncontrolled injection of multiple electrons rather than the intended single-electron detection, effectively converting single-electron events into multi-electron injection pulses. The extended duration of the voltage perturbation for larger capacitance values directly correlates with the prolonged periods of enhanced electron injection observed in the current transients. The duration and magnitude of this parasitic voltage perturbation depend critically on both the base resistance value and the collector parasitic capacitance.

A larger C_{pc} leads to a larger avalanche charge generated per event and a slower discharge process, which prolongs the duration of the avalanche current pulse and consequently extends the period of enhanced forward bias. A larger R_p increases the voltage drop across the base resistance during the avalanche current, creating a stronger forward bias of the base-emitter junction and thus injecting more electrons per avalanche event: R_p determines the injection strength (how many electrons per event), while C_{pc} determines the injection duration (how long the enhanced bias persists).

2.4. SPICE Model Development

2.4.1 Motivation and Model Architecture

While TCAD simulations provide detailed insights into the physical mechanisms underlying SEBAT operation, they are computationally intensive and not suitable for circuit-level design and optimization. To enable efficient circuit simulation, a compact SPICE model was developed that captures the essential device behavior while maintaining computational efficiency suitable for system-level analysis. As a design tool for the simulation of SEBAT-based circuits, the SPICE model was developed with parameters extracted from TCAD simulations to ensure consistency between the detailed physics-based analysis and the compact circuit representation. The SEBAT model combines a bipolar transistor model with a Geiger-mode avalanche diode representation, providing a comprehensive yet computationally efficient description of device behavior. The model architecture incorporates two main components: a conventional bipolar junction transistor model based on the widely used Gummel-Poon macro model [98], and an avalanche current generator that represents the Geiger-mode operation. The bipolar transistor component captures the DC and small-signal characteristics of the device in normal operation, while the avalanche component models the multiplication process during Geiger-mode events. For the avalanche diode representation, two modeling approaches were considered: a series branch containing a switch, voltage source, and resistance component [100], or a current source approach [101]. The current source approach was selected for this work due to its superior convergence characteristics in SPICE simulations, though both approaches can provide comparable results when properly implemented.

DC Parameter Extraction

Using the validated TCAD model that demonstrated good agreement with experimental measurements, the DC parameters were extracted from the simulated Gummel plots. The extraction methodology focused on the key bipolar transistor parameters required for the compact model:

- **Current gain extraction**

From the validated Gummel plot analysis (Fig. 2-9), the common-emitter current gain β of approximately 10 and common-base current gain $\alpha \approx 0.9$ were extracted in the exponential region (0.2 V to 0.4 V base-emitter voltage) by sweeping the p-well voltage from 0 V to 0.8 V while holding the collector at 5 V. These extracted parameters were then implemented in the SPICE compact model for subsequent circuit-level simulations.

- **Voltage-Dependent Capacitance Extraction**

The junction capacitances were extracted as functions of applied voltage from the validated TCAD simulations, as these voltage-dependent capacitances significantly influence the transient behavior

during avalanche events. The voltage-dependent nature of these capacitances is critical for accurate transient modeling, as the capacitance values change during the bias voltage variations that occur during avalanche events. The parasitic circuit elements identified in the TCAD analysis were incorporated into the SPICE model shown in Fig. 2-18 to ensure accurate representation of the complete system behavior. The parasitic base resistance R_p was extracted from the validated TCAD I-V characteristics, with the dominant contribution identified as contact resistance rather than semiconductor base resistance. Since the semiconductor base resistance was estimated around $10\ \Omega$ in TCAD simulations, the extracted total parasitic resistance of $357\ \Omega$ confirms that contact resistance (approximately $347\ \Omega$) is the primary contributor to the total base resistance.

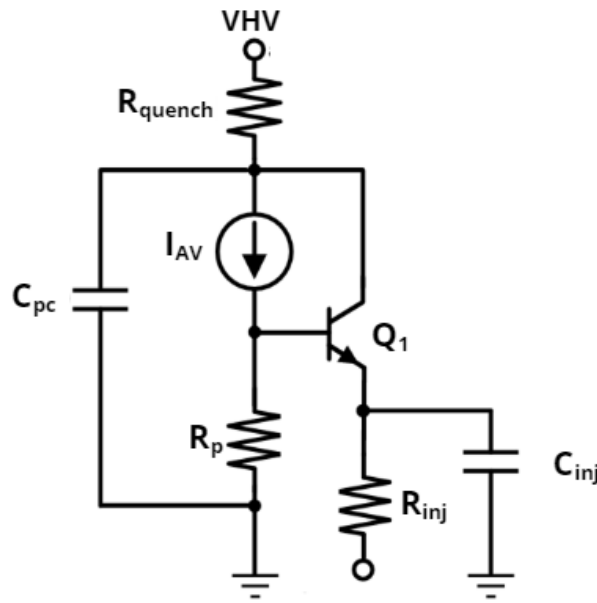


Fig. 2-18. SPICE model of the SEBAT.

2.4.2 DC SPICE Model Validation

The accuracy of the DC parameter extraction methodology was verified by comparing the SPICE model predictions against both TCAD simulation results and experimental measurements for steady-state characteristics. Fig. 2-19 presents the comprehensive comparison between experimental data, TCAD simulations, and SPICE model predictions for the Gummel plot characteristics, demonstrating the complete validation chain from experimental device to compact circuit model.

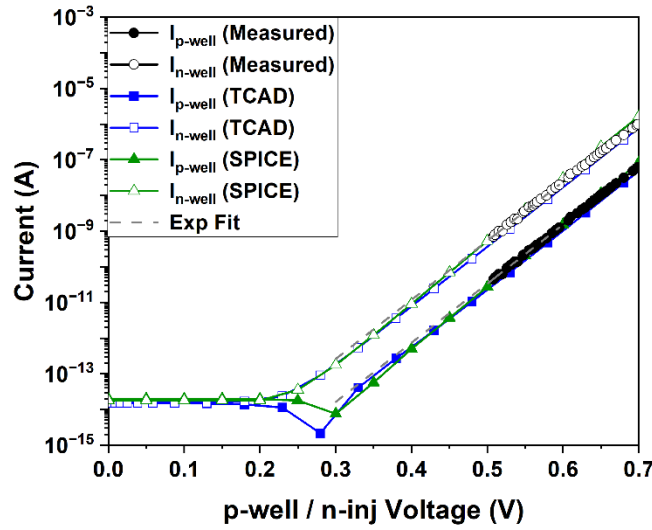


Fig. 2-19. DC Parameter Extraction Validation: Gummel Plot Comparison of Experimental Measurements, TCAD Simulations, and SPICE Model Predictions.

The SPICE model accurately reproduces both the TCAD curves and the underlying experimental behavior across the operational voltage range, confirming that the extracted parameters effectively capture the actual device physics. This three-way comparison provides strong confidence in using the compact model for circuit-level design, as it demonstrates fidelity to the real device characteristics while maintaining the computational efficiency needed for system optimization.

2.4.3 Transient Model Validation

The transient behavior validation represents the most critical aspect of SPICE model verification, as SEBAT operation relies primarily on avalanche event dynamics rather than steady-state characteristics. Fig. 2-20 presents the comparison between TCAD simulations and SPICE model predictions for injector current transients during avalanche events, demonstrating the model's ability to capture the complex temporal behavior that governs single-electron detection performance. The comparison shows that the SPICE model accurately reproduces both the pulse duration and amplitude characteristics predicted by TCAD simulations for different parasitic parameter values. This validation confirms that the compact model correctly represents the critical parasitic effects that determine charge injection efficiency and recovery dynamics. The agreement between the two approaches across different operating conditions provides confidence that the SPICE model can reliably predict the transient phenomena that ultimately determine SEBAT detection performance in practical circuit applications.

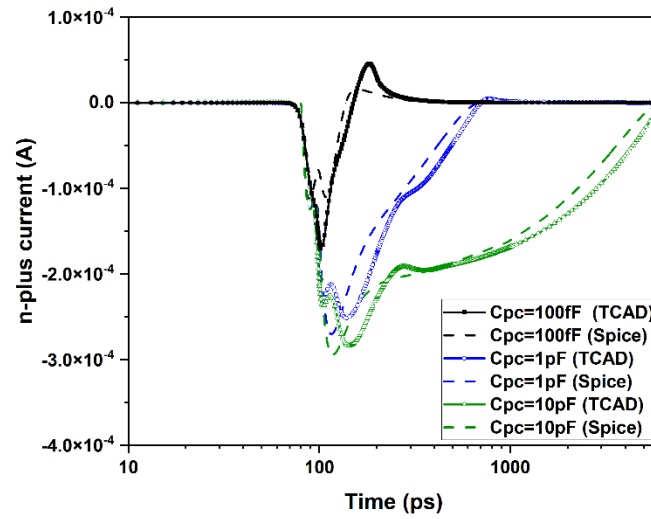


Fig. 2-20. SPICE Model Transient Validation: Injector Current Pulses Showing Agreement with TCAD and Experimental Data Across Parasitic Parameter Variations.

2.5. SPICE Model THz-SET Application Results

The validated SPICE model provides a powerful tool for analyzing the complex interactions between circuit parameters and device performance, enabling systematic investigation of the phenomena observed experimentally in very short time. The effect of R_{inj} on SEBAT transient operation was reproduced by using the SPICE model, as shown in Fig. 2-21, where V_{inj} and the injector current are shown for both low and high values of R_{inj} . This analysis directly correlates with the experimental observations described in Section 2.2.1, where different gate bias conditions (high vs low V_g) resulted in distinctly different count rate statistics and inter-arrival time distributions. In both impedance cases, a net charge packet is injected from the emitter region into the base towards the avalanche junction.

For medium and low resistance connected to the injector, this effect does not affect the count rate vs voltage curves, as shown in Fig. 2-7 and Fig. 2-8 for $V_{gate} \geq 0.2$ V, since the duration of the current pulse is of the order of 1 ns and thus shorter than the avalanche junction recharge time. The SPICE simulations confirm rapid voltage recovery and short-duration current pulses that do not significantly affect the device recharge characteristics, corresponding to the exponential inter-arrival time distributions observed experimentally and confirming proper single-electron detection operation. The presence of a transient current at the injector becomes relevant, however, when a very high resistance source is connected to the injector.

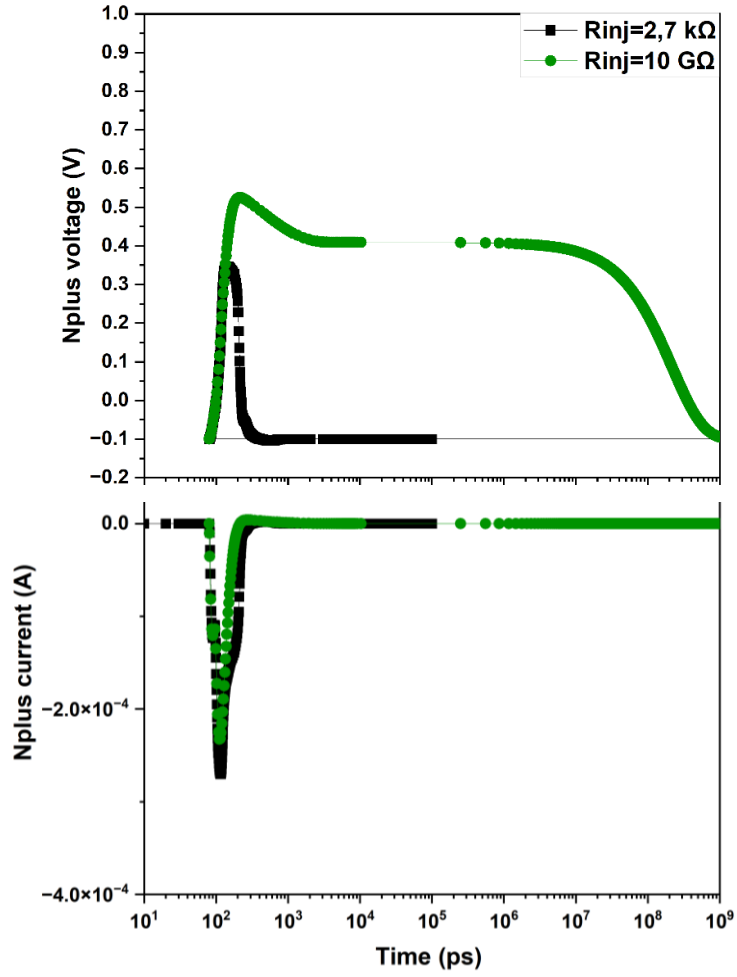


Fig. 2-21. Temporal evolution of injector voltage and current with high and low impedance injector load.

In this case, the transient current discharges the base-emitter capacitance, and the emitter recharge time is determined by the time constant $C_{inj} \times R_{inj}$. If this time constant is larger than the device recharge time, the base-emitter voltage increases slowly after an avalanche event until it reaches the initial value again after a few time constants. During the injector recharge time, the count rate will be reduced, and the electron emission statistics will be affected. The SPICE model reveals these extended voltage perturbations and prolonged current transients that significantly impact the device recovery dynamics, creating the distorted statistics observed experimentally. Therefore, with these considerations, both effects observed experimentally in Section 2.2 for an applied voltage $V_{gate} = 0$, i.e., the reduction of the count rate and the distortion of the inter-event time distribution statistics, can be explained. This application demonstrates that the SPICE model successfully captures the fundamental mechanisms responsible for the operational differences observed

in experimental characterization, providing designers with a reliable tool for optimizing SEBAT-based circuits and predicting performance across different operating conditions.

2.5.1 Performance Analysis and Optimization

Critical Parameters for SEBAT Efficiency

The comprehensive modeling study conducted through TCAD simulations and validated with the SPICE compact model has identified two key parameters that fundamentally determine SEBAT performance in single-electron detection applications. These parameters directly influence the electron-to-pulse conversion efficiency, which is critical for achieving the high sensitivity required in THz detection systems.

- Base Parasitic Resistance (R_p)

The base parasitic resistance emerges as the most critical parameter affecting charge injection efficiency during avalanche events. TCAD simulations demonstrate that high base resistance values create significant voltage drops when avalanche current flows through the parasitic resistance, temporarily increasing the forward bias of the emitter-base junction. This enhanced forward bias causes uncontrolled injection of multiple electrons rather than the intended single-electron detection, effectively converting single-electron events into multi-electron injection pulses.

- Collector Parasitic Capacitance (C_{pc})

The collector parasitic capacitance plays an equally critical role in determining device performance by controlling the duration and magnitude of avalanche events. TCAD analysis reveals that larger C_{pc} values lead to increased avalanche charge generated per event and slower discharge processes, which prolong the duration of avalanche current pulses. This extended current flow through the base parasitic resistance creates longer periods of enhanced forward bias at the emitter-base junction, resulting in more extensive parasitic charge injection.

The combination of high base resistance and large collector capacitance creates the worst-case scenario for single-electron detection efficiency.

Quantitative Impact on Performance

The effect of parasitic parameters on SEBAT performance is demonstrated through TCAD and SPICE simulations. By increasing C_{pc} from 10 fF to 10 pF, the number of injected electrons per

pulse increases from less than 100 to approximately 10^5 when $R_p = 357 \Omega$. This simulation result directly correlates with the experimentally measured efficiency of $\sim 0.001\%$ (1 detected pulse per $\sim 10^5$ injected electrons), confirming that parasitic-induced charge injection is the dominant mechanism limiting device performance. In contrast, this increase is not observed for low base resistance ($R_p = 10 \Omega$), where the charge injection remains below 100 electrons even at maximum collector capacitance. This comparison highlights the fundamental importance of minimizing base parasitic resistance for efficient SEBAT operation.

Optimization Strategies

Based on the identified critical parameters, specific optimization strategies can be implemented to enhance SEBAT performance for single-electron detection applications. These strategies focus on minimizing the parasitic effects while maintaining the fundamental avalanche operation characteristics.

The most effective approach to reduce base parasitic resistance involves increasing the overall base contact area. Since the dominant contribution to R_p is contact resistance rather than semiconductor base resistance, larger contact areas directly reduce the total parasitic resistance. However, this optimization must be balanced against the need to avoid generation-recombination centers in the avalanche region, which necessitates careful layout design to position contacts outside the high-field regions while maintaining low resistance paths.

Reducing collector parasitic capacitance requires on-chip integration of the quenching resistance. In the present test devices, the quenching resistor is implemented externally, requiring the collector node to connect to a bonding pad with associated wire bonding. Parasitic extraction revealed that this external connection introduces significant capacitance contributions from the pad structure and bonding interface, which add to the base-collector junction capacitance to form the total C_{pc} . This total parasitic capacitance creates a parallel charging path with the quenching resistance, affecting recharge dynamics and limiting maximum count rates. Integrating the quenching circuit directly on-chip eliminates the need for external collector pads and bonding, thereby substantially reducing the effective capacitance at the collector node during avalanche operation.

2.6. Conclusions

This chapter presented comprehensive characterization and modeling of SEBAT devices fabricated in 150 nm CMOS technology to identify the mechanisms limiting electron-to-pulse conversion efficiency. Through combined TCAD transient simulation, SPICE compact modeling, and experimental validation, base parasitic resistance (R_p) and collector parasitic capacitance (C_{pc})

were identified as the dominant factors degrading performance. Experimental devices exhibited $R_p = 357 \, \Omega$ due to limited contact area in the two-contact base design, resulting in multi-electron injection during avalanche events.

The validated TCAD/SPICE modeling framework enables quantitative prediction of SEBAT performance based on parasitic parameters, establishing clear optimization pathways: (1) minimizing base parasitic resistance through increased contact area, and (2) reducing collector parasitic capacitance through on-chip quenching integration. These optimization strategies are implemented and experimentally validated in Chapter 3, where contact design improvements demonstrate substantial efficiency enhancement in 110 nm CMOS technology.

Chapter 3

3. SEBAT Structure Design, Fabrication, and Characterization

This chapter presents the optimization and comprehensive experimental validation of SEBATs for integrated sensing applications. Building on the theoretical framework and modeling predictions established in Chapter 2, five SEBAT device variants with different layouts were implemented in 110 nm CMOS technology, to improve understanding of device operation and achieve optimized performance. The experimental validation is presented, encompassing the following steps: DC characterization through Gummel plot analysis; parasitic resistance extraction to validate contact optimization approaches; inter-arrival time statistical analysis confirming ideal Poisson behavior; dynamic performance evaluation, including count rate measurements as a function of base-emitter voltage; dead time analysis; efficiency quantification under various operating conditions.

3.1. Proposed Enhanced SEBAT Devices

3.1.1 Design Philosophy and Optimization Targets

Chapter 2 identified base parasitic resistance (R_p) and collector parasitic capacitance (C_{pc}) as the performance-limiting factors in SEBAT devices. A set of test structures were designed and fabricated in a test chip, called Virgilio, to validate both the operation of the SEBAT and their use to read out antenna-coupled FET THz detectors. The SEBAT devices were implemented in the Virgilio chip considering multiple design variants, in order to optimize individual performance aspects. All device variants incorporate integrated on-chip quenching resistors, which dramatically reduce the collector parasitic capacitance to values in the range of tens of femtofarads compared to the picofarad-level capacitances associated with external quenching configurations analyzed in [8]. This integrated quenching approach eliminates the large parasitic capacitances of external load resistors and interconnects, enabling direct experimental validation of the intrinsic device capacitance effects on avalanche quenching dynamics. Additionally, effect of a gate surrounding the emitter on device operation was also considered, by including dedicated device versions.

The primary optimization targets base parasitic resistance by implementing ring-contact geometries that increase the effective contact area compared to point-contact configurations used for the device described in chapter 2. This approach enables experimental evaluation of the behavior predicted by numerical models.

To investigate the effects of a gate on SEBAT performance, matched device pairs were fabricated: one variant with a polysilicon gate surrounding the injector region and an identical variant without the gate structure. The gated configuration replicates the structure implemented in the previous 150 nm CMOS technology, which exhibited poor efficiency. The investigation aims to determine whether the gate causes charge pumping effects or enables electrons to diffuse laterally within the base region without entering the avalanche multiplication zone, thereby reducing detection efficiency. This approach isolates the gate's influence on electric field distribution in the injector-base region, which controls electron injection trajectories toward the avalanche junction. Furthermore, it enables the characterization of parasitic characteristics including gate-to-base capacitance and potential additional current paths, to assess whether the gate's effect on detection efficiency and breakdown behavior is beneficial or detrimental.

3.1.2 Vigilio Chip SEBAT Device Variants

The SEBAT devices were implemented on the Vigilio chip, a multi-purpose integrated circuit designed for the characterization of several different devices and circuits. The chip was fabricated in 110 nm CMOS technology, which provides a good tradeoff between device scaling and fabrication cost. Fig. 3-1 shows the optical micrograph of the fabricated chip with the integrated SEBAT test structures. The chip includes standalone SEBAT devices for electrical characterization, as well as SEBAT structures integrated with THz-FET detectors at 850 GHz frequencies (with and without antennas).

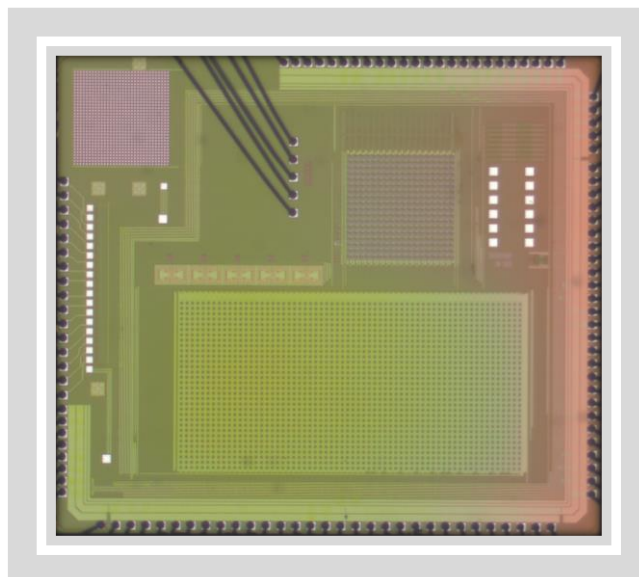


Fig. 3-1. Optical micrograph of the Vigilio chip fabricated in 110nm CMOS technology.

This test-structure-focused approach enables the validation of the optimization strategies before committing to full array implementations of chips. Five distinct SEBAT device configurations were implemented, each with dedicated bond pads for independent electrical characterization, allowing direct comparison of parasitic resistance values, efficiency metrics, and break-down characteristics across the different design configurations.

The Vigilio chip incorporates five distinct SEBAT device variants, each designed to investigate specific aspects of device optimization and validate elements of the modeling predictions. These variants explore the design space of contact geometry and gate structure configuration. Table 3-1 summarizes the configuration of each device variant.

Table 3-1. Summary of Five SEBAT Structure Variants.

Device	Gate	Ring contact	Controllable gate
01	✓	✓	×
02	×	✓	×
03	✓	✓	✓
04	✓	×	×
05	×	×	×

Device 01 - Gated SEBAT with Ring Contact

This device implements the primary optimization strategy of minimizing base parasitic resistance through ring-contact design. The ring-contact geometry shown in Fig. 3-2 significantly increases the base contact area compared to point contacts in [64], directly reducing the contact resistance. The gate serves as an implant mask for the n-plus Emitter definition during fabrication, and is electrically connected to the base.

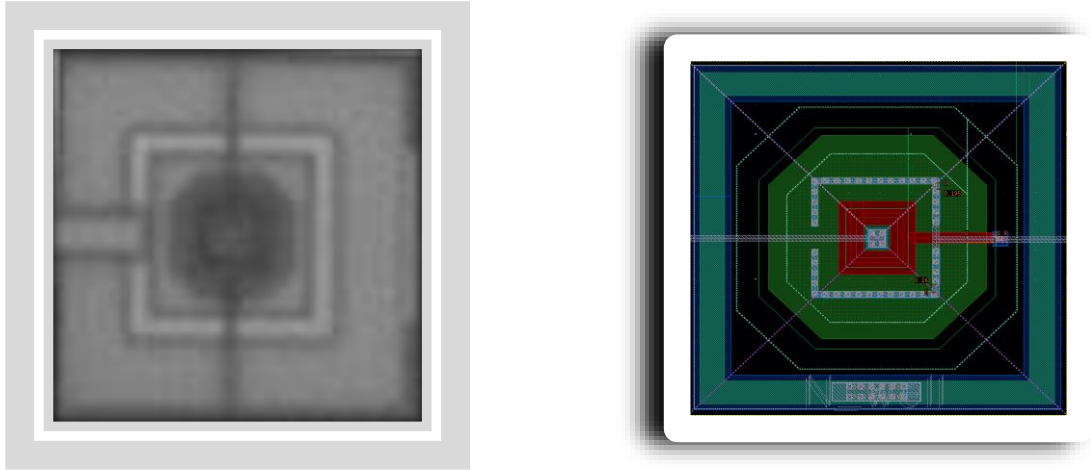


Fig. 3-2. Device 01 - Gated SEBAT with ring contact for minimized base resistance.

Device 02 - Gateless SEBAT with Ring Contact

Device 02 is identical to Device 01 in all aspects except that the gate structure has been removed from the design. The gateless device, shown in Fig. 3-3, eliminates potential parasitic capacitances associated with the polysilicon gate and gate-to-base overlap regions while modifying the electric field distribution in the injector region.

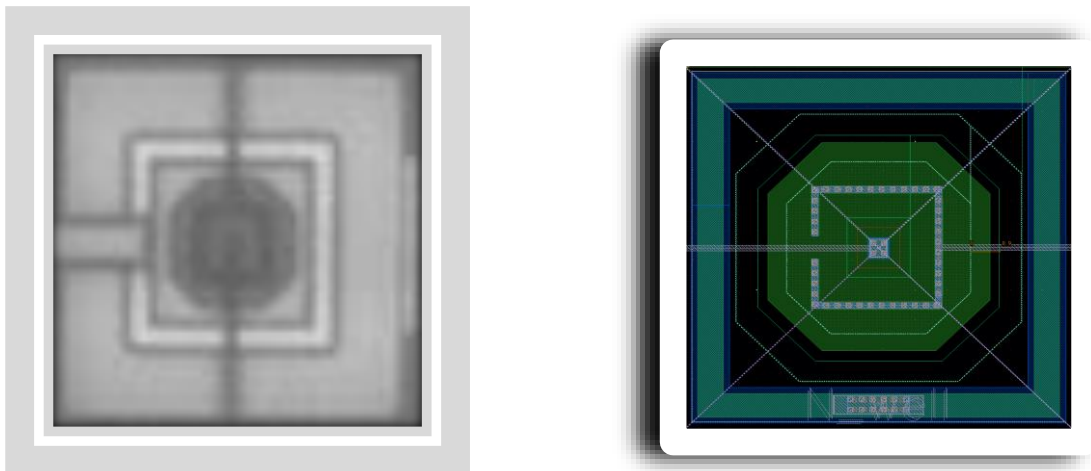


Fig. 3-3. Device 02 - Gateless SEBAT with ring contact for reduced parasitic capacitance.

Device 03 - Gate-Controlled SEBAT with Ring Contact

This device retains the gate structure with a dedicated pad for the independent bias of the gate, as shown in Fig. 3-4. The independent gate terminal allows testing the effect of its bias voltage on lateral charge escape, where electrons injected from the emitter may diffuse laterally into the base region rather than entering the avalanche multiplication zone. By applying different gate bias conditions, the potential barrier can be modulated to either suppress or enhance this lateral escape mechanism, enabling quantification of its impact on single-electron detection efficiency

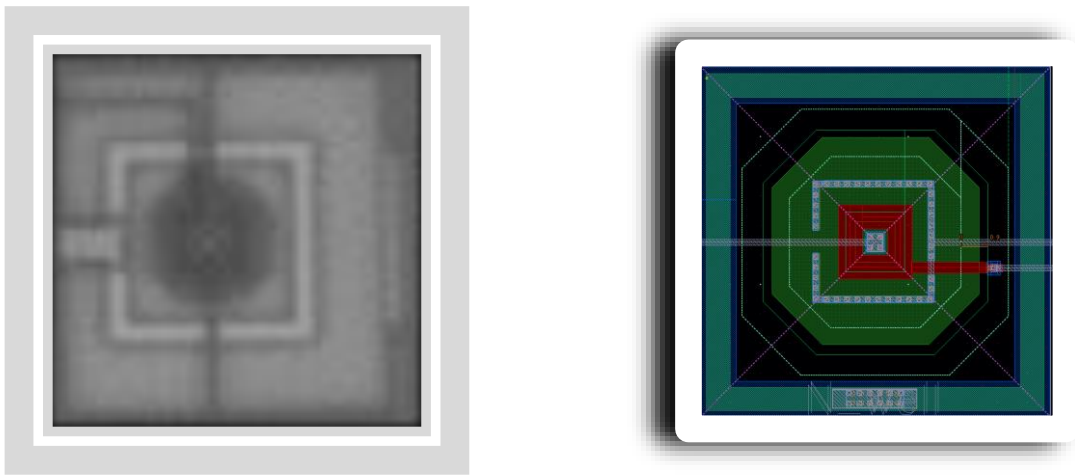


Fig. 3-4. Device 03 - Gate-controlled SEBAT with ring contact and dedicated probe pad.

Device 04 - Gated SEBAT with Two-Contact Base

This device employs two-contact base design instead of the ring-contact configuration, as shown in Fig. 3-5. The gate structure is included in this design to maintain consistency with the previous 150 nm CMOS SEBAT implementation and enable direct comparison with the gated ring-contact Device 01. This device serves as a control structure to quantify the improvement achieved through ring-contact implementation when compared with Devices 01.

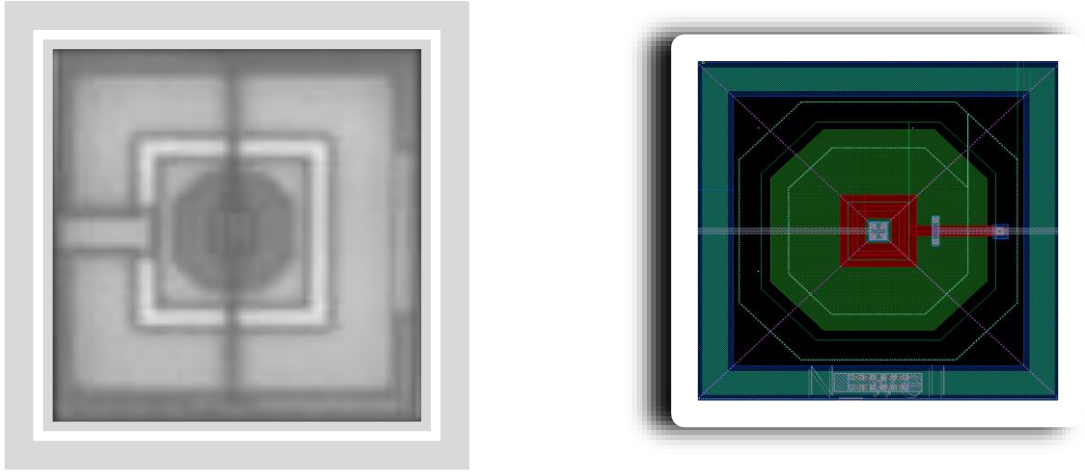


Fig. 3-5. Device 04 - Gated SEBAT with two-contact base design.

Device 05 – Non-Gate SEBAT with Two-Contact Base Resistance

This device combines a layout without gate with two-contact base design, as shown in Fig. 3-6, representing the baseline configuration for comparison with all optimized devices. Comparison between Device 05 and Device 04 isolates the gate effect, while comparison with Device 02 isolates the contact geometry effect, enabling systematic validation of the modeling predictions regarding the relative importance of each parameter.

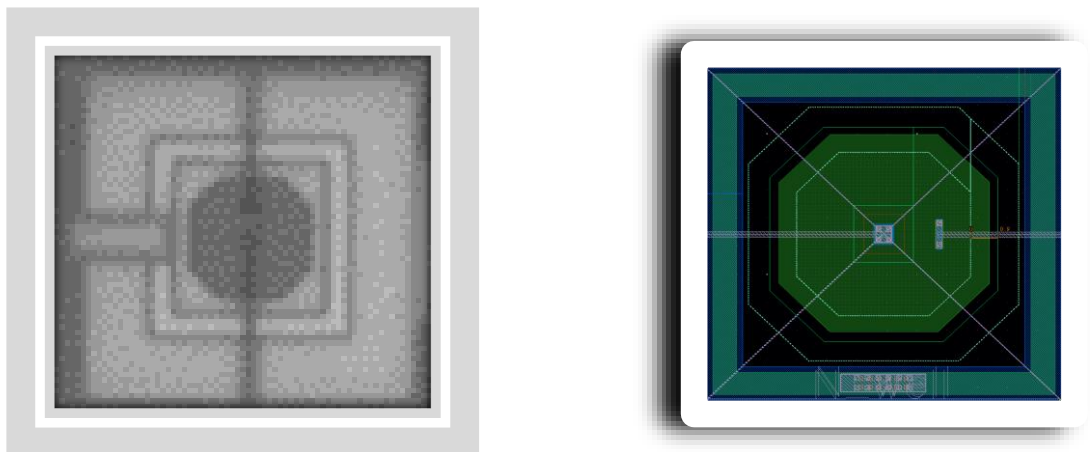


Fig. 3-6. Device 05 - Gateless SEBAT with two-contact baseline configuration.

3.2. SEBAT_THz implementation architecture

This section describes the THz detection architecture, device organization, and selection mechanisms integrated into the Vigilio chip.

3.2.1 SEBAT Test Structures and THz Integration Architecture

The SEBAT_THz section integrates 10 SEBAT devices organized in two main blocks. The first block (ROW_SEBAT) contains five SEBAT variants designed for count rate measurements to characterize the performance differences between the different designs. The second block (ROW_THz) contains the same five variants integrated with antenna-coupled FET detectors for THz measurements and system performance comparison. Both blocks are controlled sequentially through a shared selection chain, as shown in Fig. 3-7.

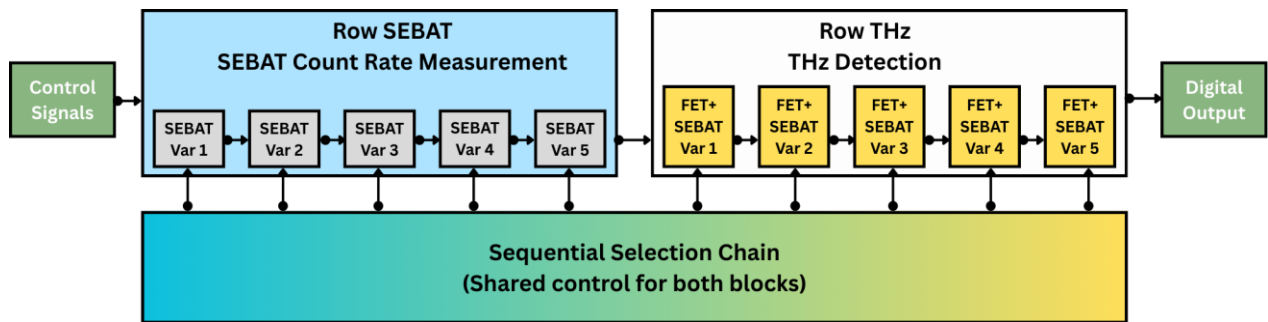


Fig. 3-7. Block diagram the SEBAT_THz section

Selection Architecture and Device Activation

To facilitate reliable data exchange between the control unit and peripheral modules, a Serial Peripheral Interface (SPI) protocol was implemented with a 64-bit register architecture. The SPI communication is governed by synchronized control signals: SPI_CLOCK, SPI_LOAD, SPI_SELECT, and optionally SPI_RESETn—ensuring precise timing during both writing and reading operations. During the write phase, data bits are serially transmitted from bit 63 down to bit 0,

while the read phase retrieves the stored data in the same order, with any excess clock cycles yielding zero output.

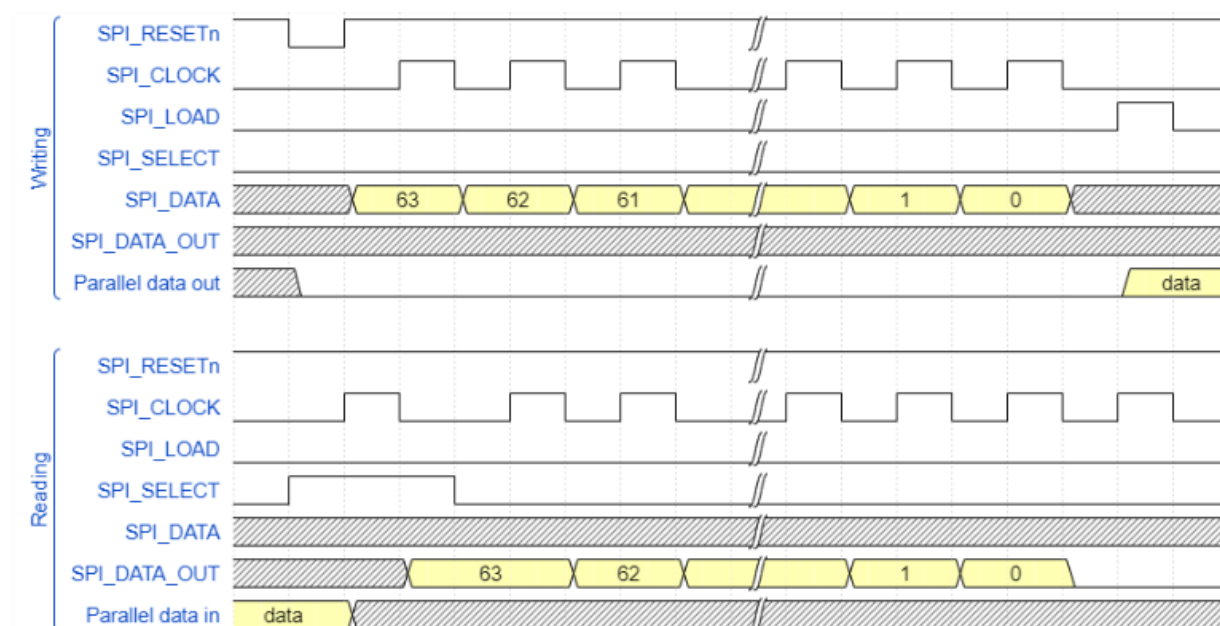


Fig. 3-8. SPI waveforms.

The register is logically partitioned to support experimental configuration (bits 0–2), output pad control (bits 3–6). This structure enables efficient multiplexing of control and data signals while maintaining compatibility with downstream processing requirements. The Reset in the writing phase is optional. By reading the SPI register it is possible to read the data written after a write phase. Any clock cycle that exceeds the 64 bits while reading will result in a 0 output.

A second stage of the selection of SEBAT devices uses a 10-stage shift register enabling independent characterization of each device variant through clock pulse counting as shown in Fig. 3-9. The shift register operates with an active-low reset signal (RESETn): pulling RESETn LOW clears all flip-flops to '0', then releasing RESETn automatically activates the first experiment (S01) without requiring any clock pulses. Pulsing the clock input shifts the '1' state down the 10-stage chain to activate subsequent experiments one-by-one. Any desired experiment can be selected by pulsing the clock the appropriate number of times: 0 pulses selects S01, 1 pulse selects S02, 2 pulses select S03, and so forth up to 9 pulses to select S10.

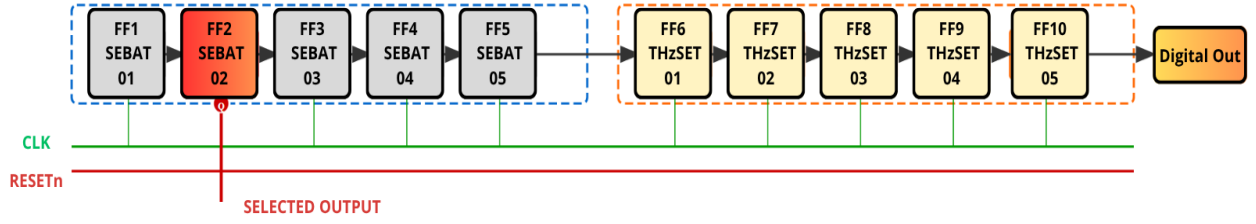


Fig. 3-9. Shift Register-Based Selection Architecture

Fig. 3-10 illustrates the timing sequence for selecting S02: RESETn initialization sets S01 active; one clock pulse shifts the active state to S02, deactivating S01; When electron injection occurs in the selected Device 02, avalanche multiplication generates a current pulse at the collector. This pulse is processed by the integrated quenching and detection circuit, which quenches the avalanche and converts the analog current pulse into a digital output signal at the output pad for measurement by external instrumentation. This shift register architecture enables flexible sequential control of all 10 experiments.

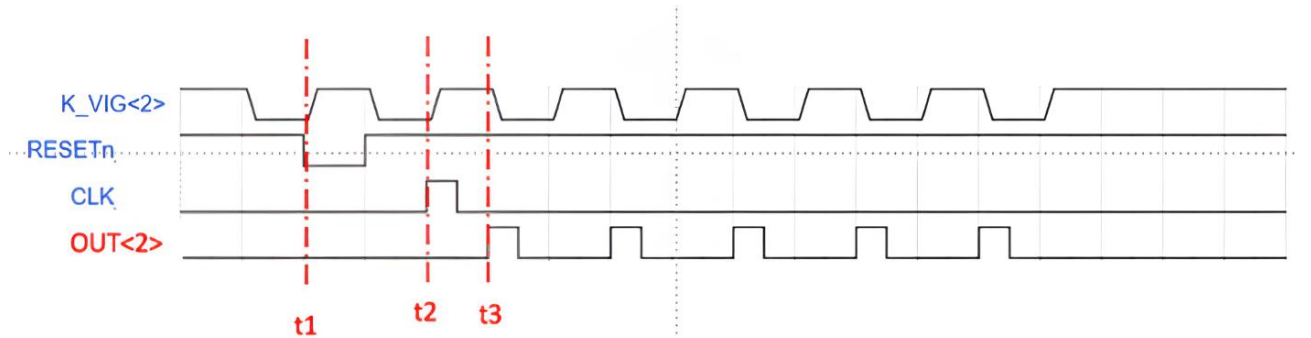


Fig. 3-10. The timing diagram to select the second SEBAT structure.

3.2.2 SEBAT structures with unprotected pads

In addition to the SEBAT devices with integrated quenching circuits, the Vigilio chip includes a separate block containing five SEBAT structures with pads without ESD protection specifically designed for DC measurements and detailed electrical characterization without the complexity of integrated readout circuits. The unprotected pad structures are necessary because ESD protection devices, integrated quenching and readout circuits introduce additional parasitic elements that would interfere with accurate extraction of intrinsic device parameters. Direct probe access to bare device terminals enables precise measurement of the base-emitter I-V characteristics required for parasitic resistance extraction using the forward-bias PN junction methodology described in Sec-

tion 3.3, as well as collector-emitter breakdown voltage measurements under controlled bias conditions without circuit loading effects.

The micrograph and the layout of the devices are shown in Fig. 3-11 a and b.

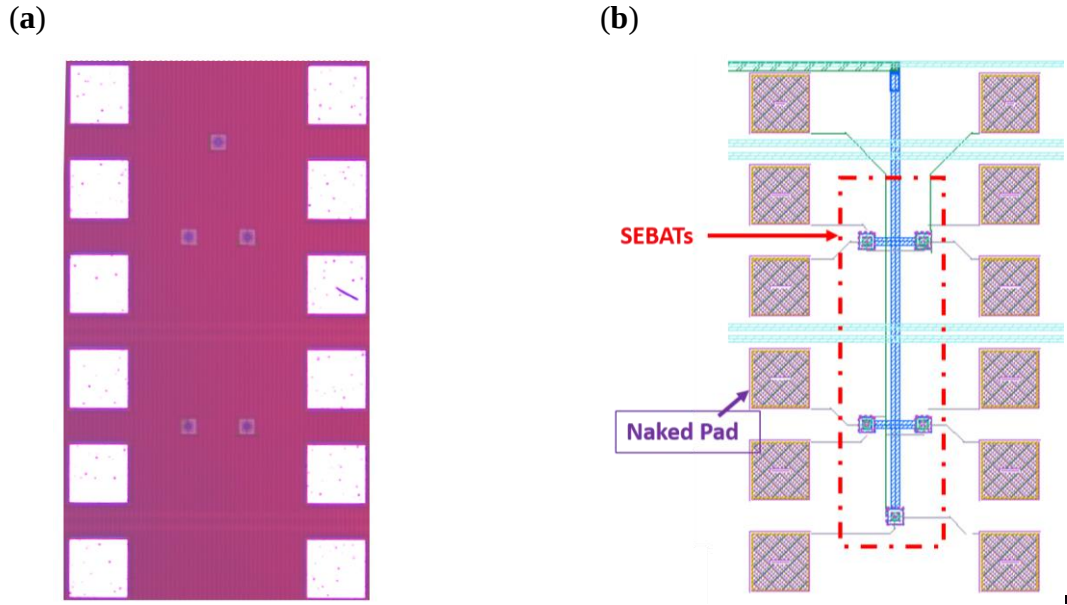


Fig. 3-11. SEBATs with unprotected Pads; (a) Micrograph (b) layout.

3.3. Electrical Characterization Setup and Methods

A comprehensive electrical characterization was performed on all five device variants to validate the modeling predictions and extract critical performance parameters. The characterization campaign encompassed different measurements. On stand-alone test structures, DC characterization through Gummel plot analysis, forward-bias I-V measurements for parasitic resistance extraction- and breakdown voltage measurements to assess avalanche junction characteristics were conducted. Test devices with integrated quenching were used to perform dynamic measurements including count rate analysis, inter-arrival time statistics, and efficiency quantification across the operating voltage range. The measurement setup utilized a probe station for DC characterization with precise source-measure units, and a shielded dark chamber providing complete optical isolation for dynamic measurements to ensure all detected events originate from electrical injection rather than stray photons.

DC Characterization Setup

DC measurements were carried out using a probe station (Fig. 3-12) to maintain electrical isolation and ensure reliable data collection. The probe station chuck uses vacuum suction to secure the chip during measurements, providing mechanical stability for reliable probe contact. The station is electrically isolated from external interference through proper grounding and shielding of measurement cables. The characterization procedure included Gummel plot analysis to validate bipolar transistor behavior [98], breakdown voltage measurements to determine the avalanche threshold, and parasitic resistance extraction through I–V analysis.



Fig. 3-12. Probe station setup for DC characterization measurements with electrical isolation.

- **Gummel Plot Analysis and breakdown voltage**

DC characterization was performed through Gummel plot analysis to validate bipolar transistor operation and extract key device parameters. Since all five devices were fabricated in the same 110 nm CMOS process using identical junction configurations, Device 01 is taken as representative of the DC behavior. In the measurements, 5V were applied to the collector with p-well voltage swept from 0 V to 0.75 V, recording both base current ($I_{p\text{-well}}$) and collector current ($I_{n\text{-well}}$) simultaneously at room temperature. The experimental Gummel plot shown in Fig. 3-13 demonstrates exponential behavior in the forward bias region with clear separation between collector and base currents, indicating significant current amplification. Device 01 exhibits a common-emitter current gain $\beta \approx 80$, and a common-base gain α approaching 0.99, consistent with theoretical expectations. More details about the Gummel plot extraction methodology are reported in section 2.3.3.

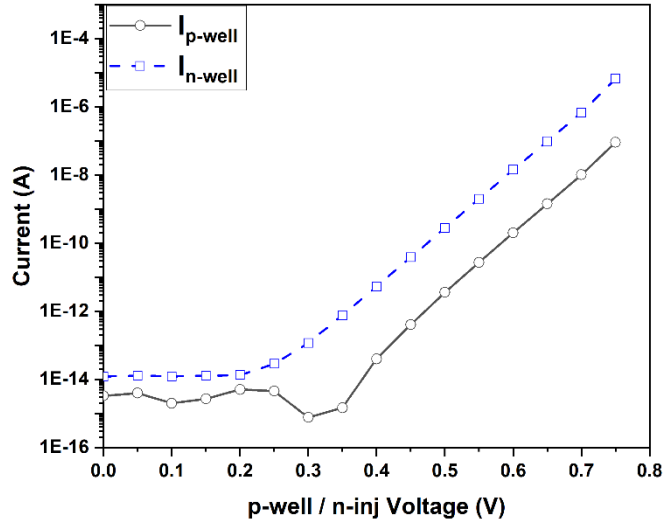


Fig. 3-13. Gummel plot of the SEBAT operated as a bipolar transistor, with the collector biased at 5V.

The reverse-biased p-well / n-well junction breakdown voltage of Device 01 was extracted from the I-V characteristics shown in Fig. 3-14 using the tangent line intersection method applied on the log-scale characteristic, yielding $V_{BD} \approx 17.6$ V.

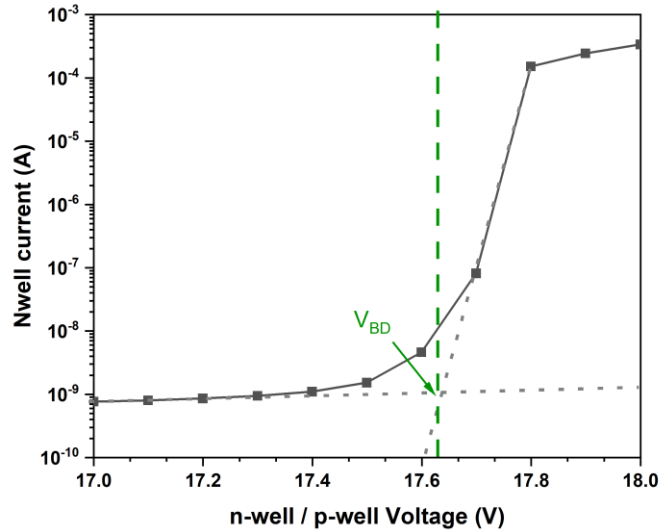


Fig. 3-14. Reverse-bias I-V characteristics of the p-well/n-well junction (Device 01)

This value is compatible with 110 nm CMOS SPAD characteristics reported for this technology node [87]. This value enables Geiger-mode operation at $V_{HV} = 20$ V, providing an excess bias of

$V_{EX} \approx 2.4$ V above breakdown, sufficient to ensure high avalanche triggering probability for single-electron detection.

- **Base Parasitic Resistance Extraction**

Base parasitic resistance (R_p) was extracted from experimental I-V curves on the p-well / n-well junction in forward bias as shown in Fig. 3-15. The n-well contact resistance was minimized by using a large number of contacts on the external n-well frame. Since the semiconductor base resistance is estimated around $10\ \Omega$ in TCAD simulations, the dominant contribution is due to contact resistance. Notably, an accurate estimation of the contact resistance using TCAD is challenging due to complex mechanisms involving hole tunneling, field-induced barrier lowering, and unknown parameters such as the metal work function. The experimental extraction of this parameter ensures a more realistic representation of the device's electrical characteristics.

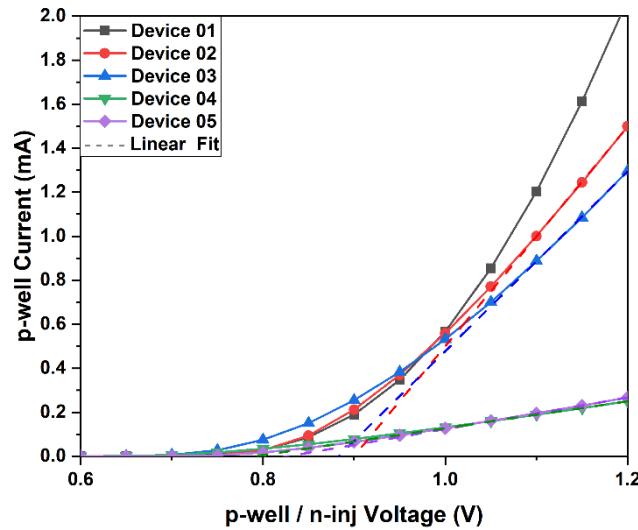


Fig. 3-15. IV characteristics of the SEBATs p-well/n-well junction implemented in 110nm CMOS.

At low forward-bias voltages (below approximately 0.8 V), the p-well/n-well diode exhibits ideal exponential I-V behavior following the Shockley diode equation $I = I_0 \exp(qV/nkT)$, where the current is dominated by junction physics. However, at higher voltages (above 0.8 V), the increasing current causes a significant voltage drop across the series parasitic resistance R_p . This voltage drop reduces the voltage appearing across the junction itself, causing the I-V characteristic to deviate from exponential behavior and transition to a linear relationship between current and applied voltage. In this linear regime, the slope of the I-V curve directly equals $1/R_p$, allowing straightforward extraction of the parasitic base resistance from the linear fit to the experimental data, as illustrated in Fig. 3-15. Devices 01, 02, and 03 with optimized base contacts featuring forty-two

contact squares distributed along the p-well perimeter demonstrated significantly low parasitic resistance values of 113 Ω , 202 Ω and 253 Ω , respectively. In contrast, Devices 04 and 05 with only two contact squares exhibited much higher resistance values of 1418 Ω and 1658 Ω respectively, demonstrating the dominant role of contact number in determining parasitic resistance. The approximately 13 $\times$ increase in parasitic resistance is smaller than the ratio between the number of contacts (21 $\times$) in the two variants. The semiconductor and n-well contact resistance, which also contribute to the measured parasitic resistance and add to the p-well contact resistance, can account for this difference. A certain dispersion in resistance values among devices with the same number of contacts is observed since the contacts are not silicided, which increases the variability of contact resistance values compared to an ideal optimized configuration.

3.3.1 Geiger-Mode Operation and Time-Resolved Characterization - Measurement Setup and Results

Geiger-mode characterization measures SEBAT performance under avalanche operation with continuous electron injection, where each injected electron triggers a self-sustaining avalanche pulse. Unlike DC measurements that characterize the device as a bipolar transistor in linear mode, Geiger-mode operation evaluates the device's ability to detect individual electrons and convert them into digital output pulses. The time-resolved measurements were conducted in an optically isolated setup to ensure all recorded avalanche events originate exclusively from electrical injection rather than stray photons that could trigger spurious avalanches. The enclosure was maintained at room temperature (approximately 25°C) throughout all measurements.

This dynamic characterization employed a Tektronix DPO3034 digital phosphor oscilloscope (300 MHz bandwidth, 2.5 GS/s sampling rate) for inter-arrival time analysis with sufficient temporal resolution to capture individual avalanche pulses and measure sub-microsecond timing statistics, and a Tektronix FCA3100 counter for count rate recording over extended measurement periods up to several minutes.

The SEBAT pulses are processed on-chip through the readout circuitry to generate digital output as shown in Fig. 3-16. The integrated quenching resistance was 800k Ω , providing adequate avalanche quenching while maintaining reasonable recharge times.

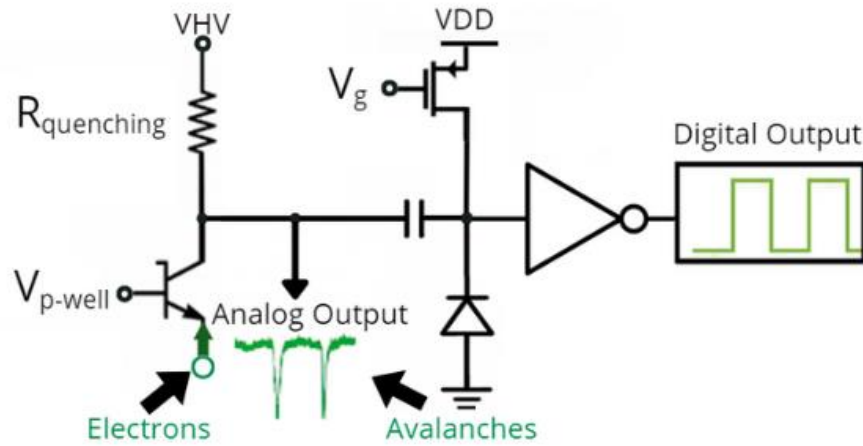


Fig. 3-16. SEBAT with Integrated Quenching and Pulse Detection Circuit.

The collector node couples through a capacitor to an inverter input node held high by a pull-up transistor, which is connected to protection diode, which clamps the input node to prevent negative voltage excursions that could damage the inverter gate oxide. Avalanche pulses pull this node below the inverter threshold, generating digital output pulses. On-chip integration of front-end electronics minimizes collector parasitic capacitance.

All data underwent offline processing for statistical analysis and parameter extraction across multiple bias conditions.

Inter-Arrival Time Statistics

The inter-arrival time distributions for Device 01 were measured to validate Poisson statistics and single-electron detection operation. Device 01 features the optimized ring contact configuration and provides an ideal testbed for statistical characterization. The measured distributions follow the expected exponential behavior across multiple bias conditions, as demonstrated in Fig. 3-17. Quantitative analysis across the extended p-well / n-well voltage range demonstrates reproducible exponential behavior spanning five orders of magnitude in count rate, validated across multiple experimental runs and consistent with theoretical predictions.

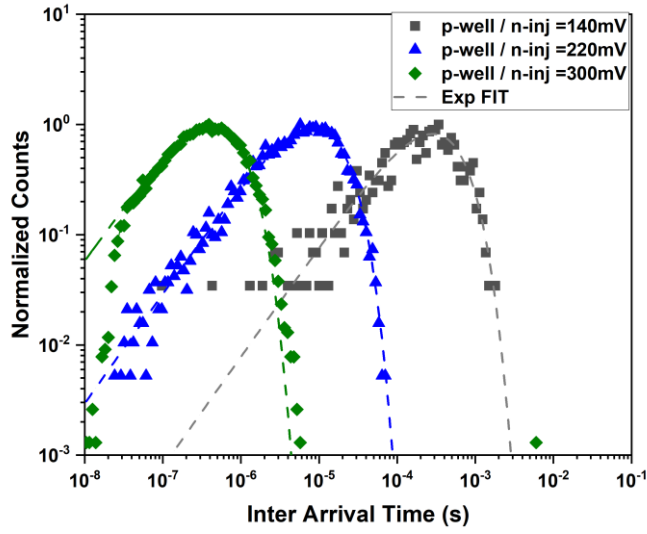


Fig. 3-17 Inter-arrival time distributions for Device 01 normalized to exponential behavior.

Count Rate Comparison - All Devices

Fig. 3-18 presents the count rate as a function of p-well / n-inj voltage for Devices 01, 02, 04, and 05 at VHV = 20 V. Device 03 was excluded from this comparison as it operates under different gate voltage conditions and will be analyzed separately in subsequent sections. All four devices exhibit nearly identical exponential rise in count rate; spanning from a few 10s to over 10^7 counts per second (cps)—up to approximately 0.4 V. This consistency across different contact configurations confirms that the SEBAT avalanche triggering mechanism is reproducible and independent of structural variations.

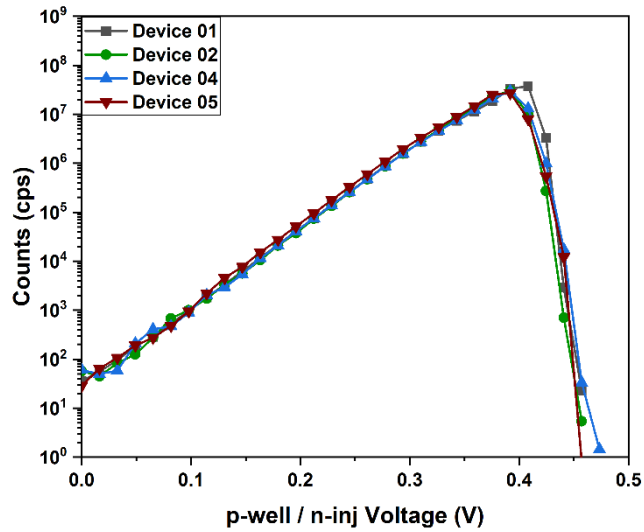


Fig. 3-18. The count rate as a function of applied voltage for the four devices.

Device 01 - Performance Under Variable High-Voltage Bias

Fig. 3-19 shows count rates for Device 01 under three different high-voltage n-well bias conditions (18.5 V, 19.5 V, and 20.5 V).

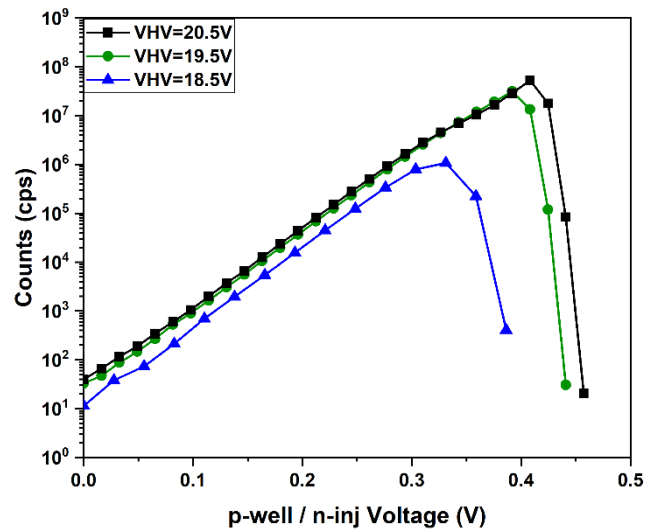


Fig. 3-19. Count rate versus p-well voltage for Device 01 at different high-voltage bias conditions.

For all three biases, the count rate displays a pronounced exponential increase, ranging from 10 cps at the lowest voltages up to more than 10^7 cps at higher voltages, spanning more than six orders of magnitude. The scaling behavior remains nearly identical up to approximately 0.35 V across all bias conditions. At higher p-well voltages, the 18.5 V condition exhibits saturation and eventual decline, while the higher VHV biases continue exponential growth.

3.3.2 Parasitic Resistance Impact on Efficiency

Parasitic resistance differences between optimized and poor contact designs manifest distinctly in injector current characteristics and their relationship to avalanche detection performance.

Injector Current Characterization

Fig. 3-20 presents the injector current as a function of p-well / n-inj voltage for (a) Device 05 (poor contact design) and (b) Device 02 (optimized ring contact), both designs without gate under varying high-voltage bias conditions.

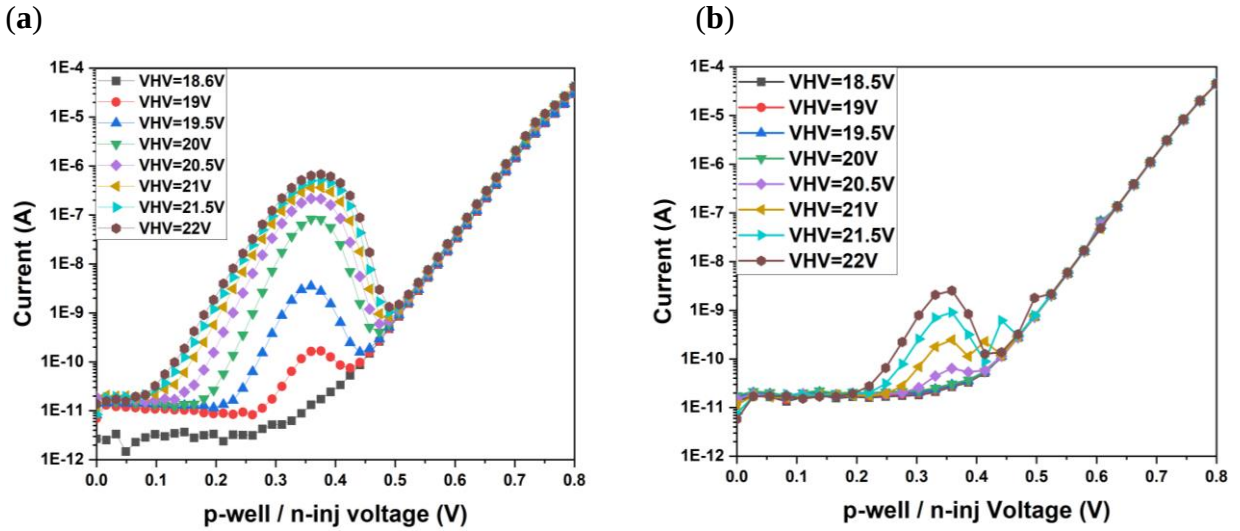


Fig. 3-20. Injector current vs applied voltage for (a) Device 05 (poor contact design, without gate), (b) Device 02 (optimized ring contact, without gate).

Device 05 exhibits pronounced and persistent local maxima in the I-V curve throughout most high-voltage bias conditions, especially at voltages between 20 V and 22 V, with distinct peaks and irregularities across the current profiles. These local maxima are connected to a transient injection effect caused by the excessive IR drop across the base parasitic resistance, as explained in Chapter 2. For device 05, regular operation is restricted to the low voltage of 18.5 V. Conversely, Device 02 shows that although local maxima appear at higher voltages, they progressively diminish as VHV decreases and effectively vanish near 20 V. Below this voltage, Device 02 transitions to smooth, monotonic current profiles. Contact optimization shifts the regular operation condition to a practical voltage range below 20 V in Device 02.

Fig. 3-21 extends this comparison to devices with gate, presenting the injector current for (a) Device 04 (poor contact design with gate) and (b) Device 01 (optimized ring contact with gate). Device 04 demonstrates similar behavior to its counterpart without gate (Device 05), with pronounced local maxima in the I-V curves dominating the high-voltage regime. Device 01 mirrors the improved performance of Device 02, achieving regular operation at $VHV \approx 20$ V with smooth monotonic I-V characteristics. The near-identical behavior between devices without gate (Devices 02/05) and devices with gate (Devices 01/04) confirms that contact geometry, not gate configuration, determines the device operating conditions.

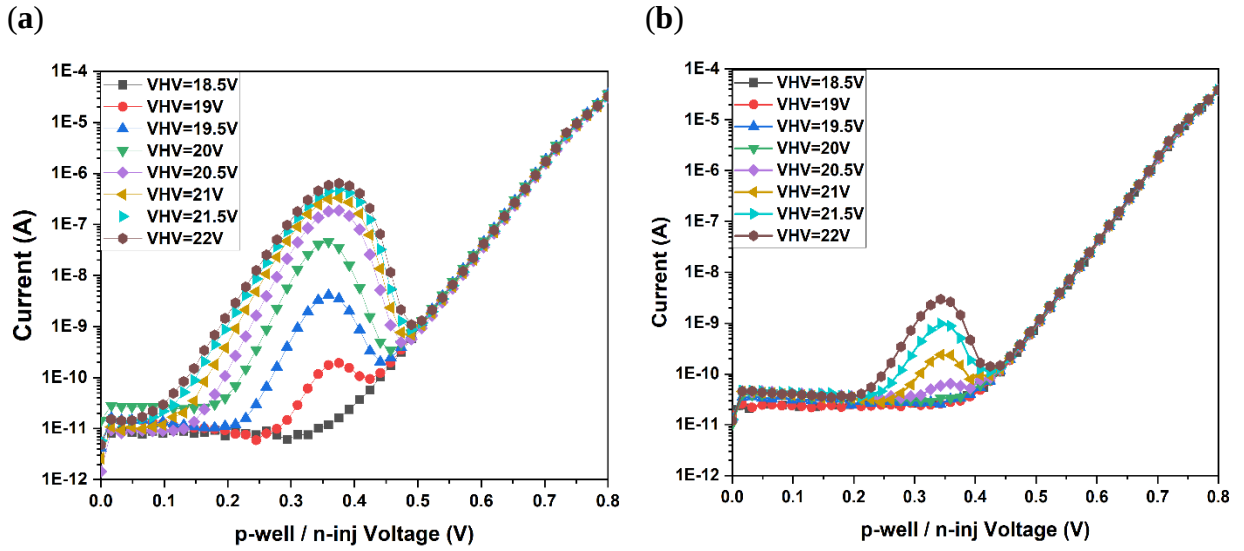


Fig. 3-21. Injector current vs applied voltage for (a) Device 04 (poor contact design, with gate), (b) Device 01 (optimized ring contact, with gate).

Fig. 3-22 presents the injector current for Device 03 operating with floating gate configuration. Device 03 employs the same optimized ring contact geometry as Devices 01 and 02 but operates with the gate terminal left floating rather than biased or grounded. The current behavior closely mirrors that of Devices 01 and 02, exhibiting local maxima at elevated voltages that progressively diminish as VHV decreases, with regular operation achieved near $VHV \approx 20$ V.

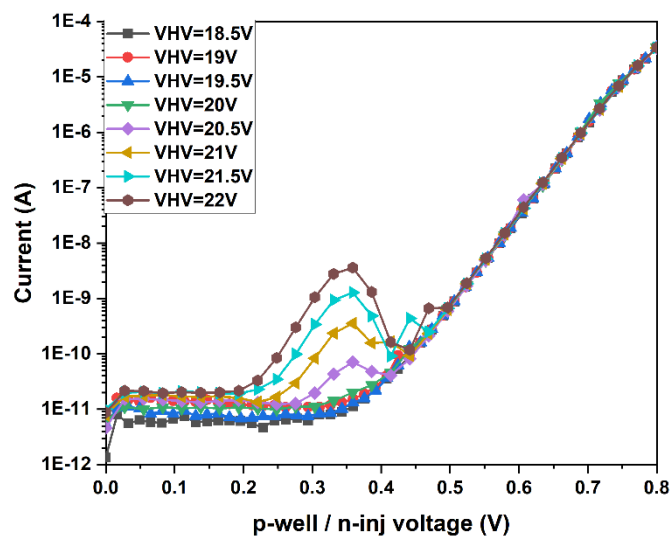


Fig. 3-22. Injector current vs applied voltage for Device 03 (optimized ring contact, floating gate), under varying VHV bias conditions.

Detection Efficiency

The estimation of electron detection efficiency can be based on the comparison between the current injected at the emitter, which can be transformed into a injected electron flux, and the count rate observed at the SEBAT collector. In this section, this comparison is analyzed for the different device variants implemented in Vigilio chip. Fig. 3-23 reveals that the injected charge flux in Device 05 exhibits a local maximum at a voltage slightly larger than 0.35V. Below 0.3V, the injected current follows an exponential trend (dashed line), but its value is several orders of magnitude larger than the count rate measured at the collector. The presence of a local maximum indicates that the parasitic resistance effects causes multi-electron injection during avalanche triggering. These additional electrons flowing in the base-emitter junction cannot trigger further avalanche events since they are injected when the avalanche junction is still discharged. In this regime, the electron injection rate can be much larger than the avalanche count rate, depending on the number of electrons injected during each avalanche event.

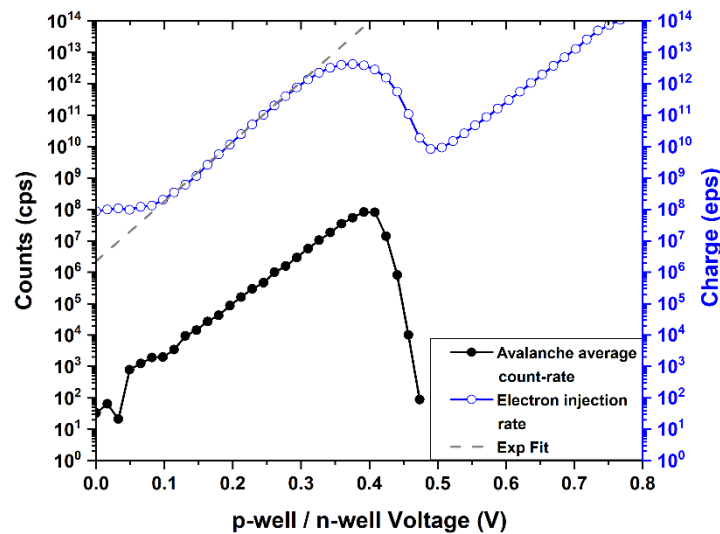


Fig. 3-23. Electron injection rate and avalanche count rate as a function of applied voltage for Structure 05 at VHV = 22V.

Fig. 3-24 presents electron injection rate and avalanche count rate as functions of p-well / n-inj voltage at VHV=22V (p-well / n-well junction reverse bias) for Devices 02 and 05, illustrating the influence of base contact optimization on device performance. Exponential curve fitting (dashed lines) is shown alongside experimentally measured avalanche count rates (solid lines with markers).

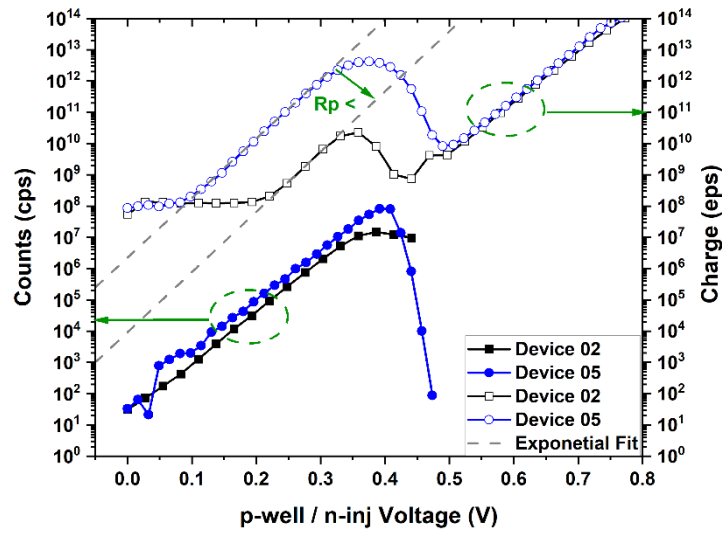


Fig. 3-24. Electron injection rate and avalanche count rate as a function of applied voltage for Structure 05/02 showing exponential charge injection behavior and inefficiency factor analysis at VHV = 22V.

In device 05, a very high injected charge level, approaching 10^{13} electrons per second, can be observed, while the avalanche count rates saturate around 10^7 - 10^8 cps. The pronounced gap between injected charge and detected counts translates in a very low electron detection efficiency. In contrast, Device 02 with optimized ring contacts shows a reduced local maximum compared to Device 05. Despite this substantial reduction, Device 02 exhibits a noticeable gap between the theoretical injection rate and measured count rate, indicating that parasitic effects remain present. It is worth noting that the local maximum in the I-V curve of Device 02 is only present at bias voltages $VHV > 20V$, while above this threshold a monotonic I-V curve is measured, indicating the absence of the transient injection effect.

Fig. 3-25 presents the injected charge per pulse as a function of applied voltage for Devices 02 and 05. Device 05, exhibits injected charge per pulse in the range of 10^5 electrons per pulse. Device 02, with optimized ring contacts, demonstrates substantially lower injected charge per pulse—ranging from approximately 10^3 to 10^4 electrons per pulse: representing a 100-1000 $\times$ reduction across the measured voltage range compared to Device 05. These measured values are in agreement with TCAD modeling predictions presented in Chapter 2, thereby confirming parasitic resistance-limited operation. The substantial reduction in injected charge per pulse in Device 02 validates the effectiveness of contact optimization in minimizing parasitic charge injection during avalanche events. However, the residual injected charge per pulse remaining at 10^3 electrons per pulse at low voltages and reaching 10^5 electrons per pulse at higher voltages indicates that parasitic

effects persist despite optimization, requiring a lower bias voltage for efficient operation. For $V_{HV} > 20V$, a direct estimation of the efficiency can be inferred from the injected charge per pulse shown in Fig. 3-25. Since each avalanche event ideally triggers from a single injected electron, the efficiency is approximately the inverse of the injected charge per pulse. At $V_{HV} = 22V$, Device 02 shows injected charge per pulse in the range of 10^3 electrons/pulse, corresponding to estimated efficiencies of less than 0.1%.

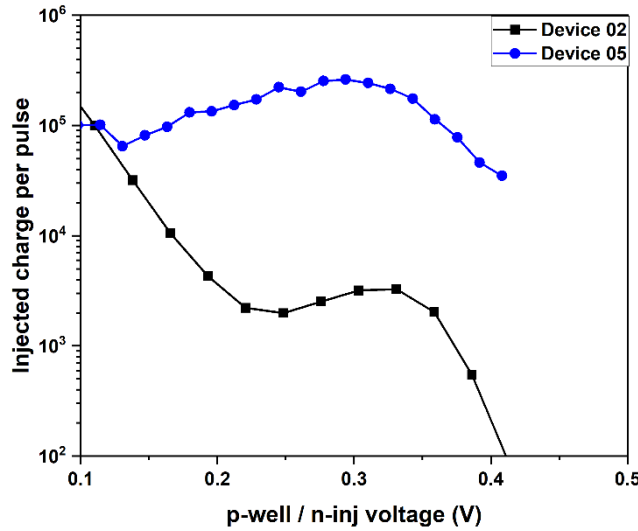


Fig. 3-25. Injected charge per pulse as a function of p-well / n-inj voltage for devices 02 and 05 ($V_{HV} = 22V$).

SEBAT-Gate Effect Analysis - Gate connected to the p-well

Fig. 3-26 presents a comparison of gate effects on SEBAT device performance by analyzing devices with identical contact designs, differing only in the presence of the gate. The left panel compares the injected charge per pulse in Device 01 (with gate) and Device 02 (without gate), both featuring optimized ring contacts, while the right panel compares Device 04 (with gate) and Device 05 (without gate) with unoptimized contact configurations. The SEBAT gates are electrically connected to the p-well, which means they are biased at the same voltage. In the optimized contact group, both Device 01 and Device 02 exhibit similar injected charge per pulse at low applied voltages, ranging from approximately 10^2 to 10^3 electrons per pulse. The similarity in injected charge profiles confirms that contact optimization dominates device performance more strongly than gate-related variations. For the group with unoptimized contact, Devices 04 and 05 both demonstrate consistently high-injected charge per pulse at low voltages, exceeding 10^5 electrons per pulse. The presence of a gate in Device 04 does not significantly affect these high charge levels,

indicating that parasitic limitations imposed by poor contacts dominate over any gate-related effects also in this case. The substantial reductions in injected charge per pulse achieved with optimized ring contacts are reproducible regardless of gate inclusion, confirming that contact design—not gate configuration—is the primary determinant of SEBAT parasitic charge control.

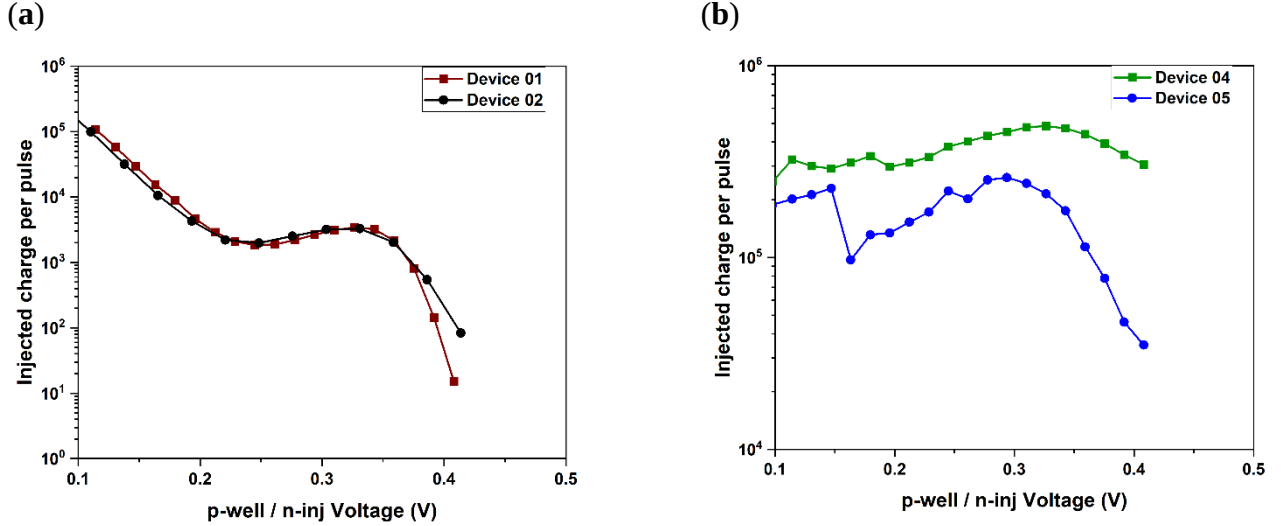


Fig. 3-26. Injected charge per pulse as a function of p-well / n-inj for (a) Device 01 and 02, (b) Device 04 and 05 (VHV = 22V).

SEBAT-Gate Effect Analysis - SEBAT with externally biased gate

Fig. 3-27 compares count rate as a function of pwell/n-inj voltage for Device 03 when the gate is biased at different voltages.

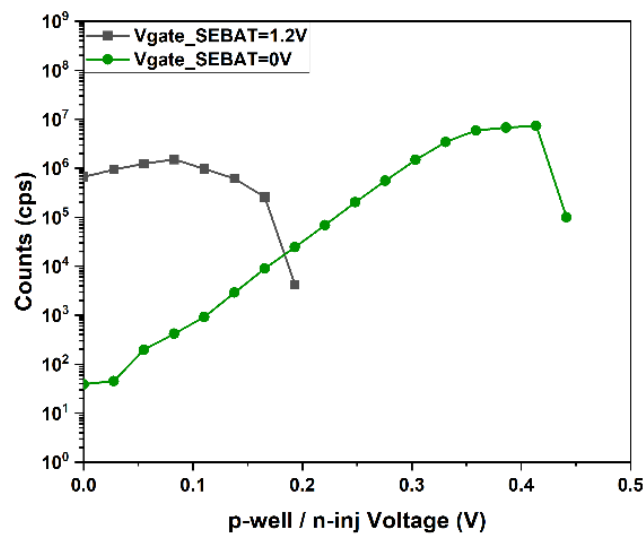


Fig. 3-27. Count rate as a function of p-well/n-inj voltage for Device 03.

At $V_{\text{SEBAT_gate}} = 0 \text{ V}$, the count rate exhibits exponential trend consistent with the previous results at the same $\text{VHV} = 20 \text{ V}$, validating that the gate at zero bias does not introduce anomalous charge injection.

At $V_{\text{SEBAT_gate}} = 1.2 \text{ V}$, the count rate is significantly increased at low applied voltages, indicating that positive gate bias enhances electron injection into the base region. This early elevated count rate reveals that a positive gate bias introduces additional charge injection, probably originating from the charge generation at the Si/SiO₂ interface below the gate, and it adversely affects the functionality of the transistor.

VHV Optimization and Operational Window Definition

The experimental data discussed previously for devices 01 and 02 identifies $\text{VHV} \approx 20 \text{ V}$ as the critical operational threshold that determines SEBAT device performance by controlling the transient injection effect. Devices 01 and 02 demonstrate that as VHV decreases, the local maxima in the injection profile become progressively smaller and eventually disappear starting from this critical voltage, allowing the device to transition into a monotonic current-voltage curve. This threshold represents the optimal point where high single-electron sensitivity is maintained while providing a sufficiently high bias voltage to ensure a good avalanche triggering probability. The physical mechanisms underlying this threshold can be understood in view of the simulation analysis presented in chapter 2. At VHV above 20 V, the excess bias is high, driving a significant current through the base resistance R_p , and thus determining a substantial temporary increase in the voltage drop across it. This in turn result in a large forward bias of the base-emitter junction for a fraction of nanosecond, causing the injection of an electron packet from the emitter towards the avalanche junction. As VHV is reduced below 20 V, the lower excess bias reduces the current pulse magnitude, which in turn decreases voltage drops across parasitic resistances and suppresses unwanted electron injection.

Fig. 3-28 and Fig. 3-29 provide a comparison of the electron injection rate and the measured count rate at $\text{VHV} = 20 \text{ V}$ for Devices 01 and 02, respectively, both exhibiting similar trends. The count rate and charge injection rate exhibit smooth, monotonic progression: the measured count rate increases exponentially up to 10^7 cps before saturating in a controlled manner, while the injected charge is constant until 0.4V and then shows an exponential increase. The high electron injection rate measured at low voltages is likely due to limitations of the measurement setup: at low applied voltages (typically below $\sim 0.35 \text{ V}$), the measurement system cannot accurately resolve the collector current due to external leakage currents and environmental interference that mask the true device signal, as well as packaging parasitics that introduce spurious current contributions at the

measurement nodes. The exponential fit to data points in the reliable voltage region (ideality factor ≈ 1) is therefore used to extrapolate the true injection rate to lower voltages.

In all efficiency presented in Fig. 3-29 and Fig. 3-30, the EDE is computed as the ratio of the measured avalanche count rate to the extrapolated electron injection rate (Fig. 3-28, Fig. 3-29), obtained from the exponential fit applied to the reliable voltage region ($p\text{-well} / n\text{-inj} > 0.35$ V, where ideality factor ≈ 1), as described in Section 2.2.2.

The raw measured injection rate at low voltages is not used due to measurement setup limitations discussed above.

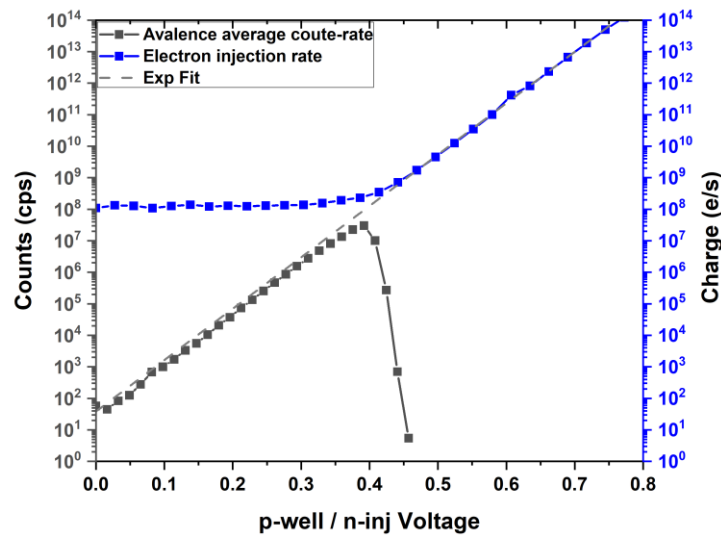


Fig. 3-28. Electron injection rate and avalanche count rate as a function of applied voltage for Device 01 at VHV = 20V

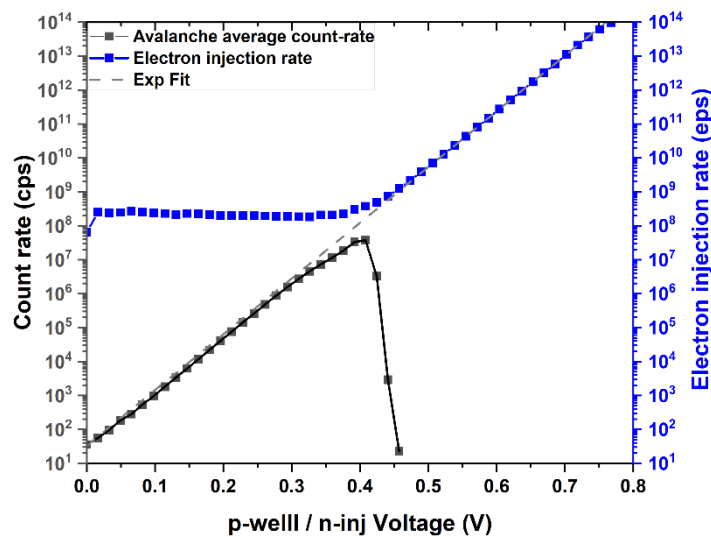


Fig. 3-29. Electron injection rate and avalanche count rate as a function of applied voltage for Device 02 at VHV = 20V.

The extrapolation of the electron injection rate aligns very well with the measured count rate for both devices. This close correspondence demonstrates that at the 20V threshold, nearly ideal electron-to-avalanche conversion is achieved.

Fig. 3-30 presents the electron detection efficiency of Device 01 (optimized ring contact with gate) as a function of applied voltage for multiple VHV values (18.5 V, 19 V, 19.5 V, and 20 V). Device 01 exhibits systematic efficiency improvement with increasing VHV. At VHV = 20 V, Device 01 achieves a peak efficiency of approximately 74% in the 0.2-0.3 V applied voltage range, maintaining elevated efficiency across an extended voltage window before gradual decline.

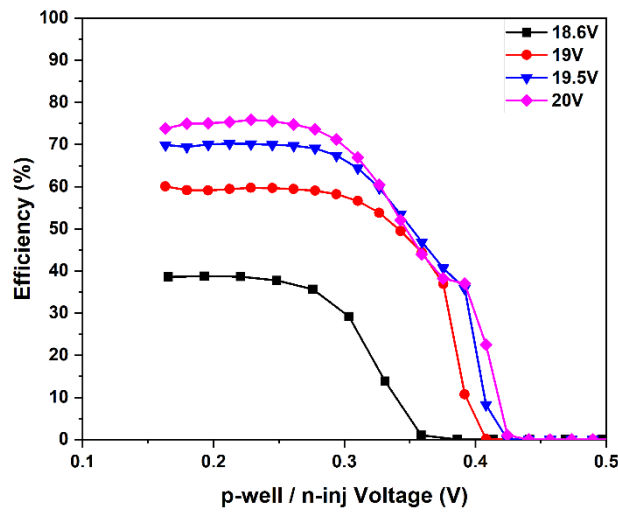


Fig. 3-30. Efficiency vs VHV for Device 01.

As VHV decreases, efficiency degrades progressively: at 19.5 V, peak efficiency reaches approximately 70-73%; at 19 V, efficiency falls to approximately 57-60%; and at 18.5 V, efficiency is limited to approximately 36% within a restricted voltage range. This dependence is probably dominated by the voltage dependence of avalanche triggering probability.

Fig. 3-31 presents the electron detection efficiency of Device 02 as a function of applied voltage for multiple VHV values (18.5 V, 19 V, 19.5 V, and 20 V), demonstrating the direct influence of high-voltage bias optimization on device performance. At VHV = 20 V, Device 02 achieves peak efficiency exceeding 80% in the 0.1-0.2 V applied voltage range and maintains efficiency above 80% across an extended voltage window before gradual decline at higher voltages. This represents

the optimal operating condition. As VHV is reduced below this threshold, efficiency systematically degrades: at 19.5 V, peak efficiency drops to approximately 75%; at 19 V, peak efficiency falls to approximately 60%; and at 18.5 V, efficiency is limited to approximately 40%.

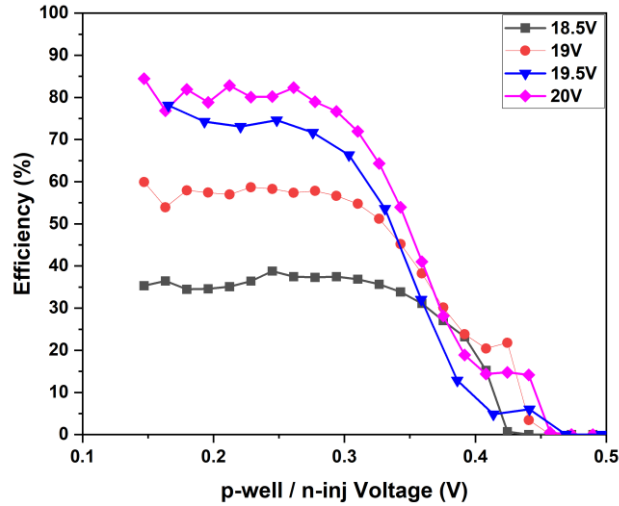


Fig. 3-31. Efficiency vs VHV for Device 02.

As for device 01, the dependence of efficiency on VHV is probably determined by the avalanche triggering probability.

The similar voltage-dependent behavior between Device 01 (with gate, peak 74% at VHV = 20 V) and Device 02 (without gate, peak >80% at VHV = 20 V) confirms that contact design, not gate configuration, determines the operational voltage requirements and efficiency trends.

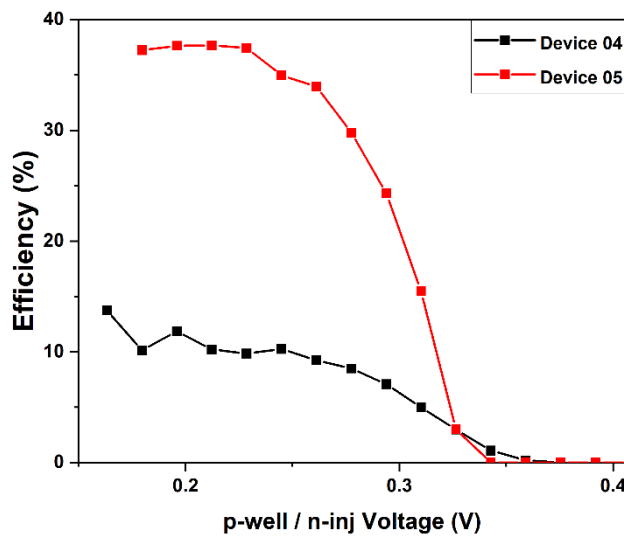


Fig. 3-32. Electron detection efficiency at VHV = 18.5V for Device 04 and 05.

Both optimized devices demonstrate that $V_{HV} = 20\text{ V}$ provides optimal performance for efficient single-electron detection.

Fig. 3-32 presents the electron detection efficiency of Devices 04 and 05 at $V_{HV} = 18.5\text{ V}$, their optimal bias point where the local maximum in the I-V curve is not observed. Device 04 achieves 10-15% efficiency across the operational voltage range (0.15-0.35 V), while Device 05 reaches peak efficiency of 37% at low voltages (0.1-0.2 V) before declining sharply above 0.25 V.

3.3.3 Performance Analysis and Experimental Validation

The comprehensive experimental characterization of multiple SEBAT devices presented in this chapter validates the theoretical model developed in Chapter 2. Contact design optimization emerges as the dominant factor determining single-electron detection efficiency. Optimized ring contacts in Devices 01 and 02 reduce parasitic base resistance to 100-200 Ω , matching TCAD predictions and overcoming limitations of two-contact designs. The operational threshold $V_{HV} \approx 20\text{ V}$ has been identified as the optimal bias voltage for efficient SEBAT operation in devices 01 and 02. At this bias, Device 02 achieves electron detection efficiency of 60-80% with smooth, monotonic current behavior across an extended applied voltage range. In contrast, devices with unoptimized contact designs (Devices 04 and 05) achieve their best operating conditions at $V_{HV} = 18.5\text{ V}$, limiting their efficiency to a value lower than 37%. Contact optimization thus shifts the operational window from low-bias, to voltage ranges providing a high avalanche triggering probability, suitable for practical applications. The results serve as design guidelines for SEBAT implementations in the readout electronics for integrated sensors.

Chapter 4

4. SIRTech Chip Design and Implementation

Building upon the validated SEBAT optimization principles presented in Chapter 3, this chapter introduces the design of a chip called SIRTech (SEBAT Infrared and Terahertz Technology), which includes 2D pixel arrays based on antenna-coupled FET detectors with SEBAT-based readout. This chip integrates three separate arrays, each optimized for a specific frequency band: 900 GHz ($\lambda \approx 330 \mu\text{m}$), 1.5 THz ($\lambda \approx 200 \mu\text{m}$), and long-wavelength infrared (LWIR, 8–14 μm / 21–38 THz), thereby addressing a wide range of application domains, from security screening to biomedical diagnostics.

4.1.1 Multi-Band Detection Integration

The SIRTech chip is a test vehicle designed to validate pixel operation and quantify performance across different spectral bands. The chip integrates three separate imaging arrays operating independently for characterization purposes: two terahertz arrays (2×2 pixels each) at 900 GHz and 1.5 THz for proof-of-concept validation, and one long-wave infrared array comprising 7056 pixels (84×84) organized into 3×3 macro-pixels, which can be connected together or read individually for higher-resolution characterization. In addition to these imaging arrays, the chip incorporates five SEBAT test structures identical to those implemented in the Vigilio chip (Chapter 3) for comparative characterization and process validation. Fig. 4-1 presents the micrograph of this chip, illustrating the arrays arrangement and interface connectivity of all integrated components.

4.1.2 Chip Floorplan and Functional Organization

The SIRTech chip shown in Fig. 4-2 ($4000 \mu\text{m} \times 3000 \mu\text{m}$) is organized as follow:

1. **IR array.** It houses the infrared array with 84×84 pixels arranged in macro-pixels with an $86 \mu\text{m} \times 69 \mu\text{m}$ pitch (rectangular layout), each macro-pixel integrates a 3×3 matrix of FET detectors (antenna + NMOS) coupled to a single SEBAT stage.
2. **THz section.** It is composed of two blocks for terahertz detection. The upper block contains the 900 GHz 2×2 -pixel array with its dedicated row decoder and SEBAT-based readout circuit, positioned at the top-right corner for optimal electromagnetic shielding. The lower

block accommodates the 1.5 THz 2×2 array, similarly, structured with array-specific readout and characterization circuits.

3. **Test structure section:** Contains five SEBAT test structures from previous designs arranged linearly for comparative characterization with common interface circuits to facilitate DC and Geiger-mode measurements, enabling direct comparison with previous characterization results in Chapter 3 and evaluation of process variations between fabrication runs.

The chip incorporates a standard padding with integrated ESD protection (except for SEBAT high-voltage bias pads) and I/O buffering for external connectivity.

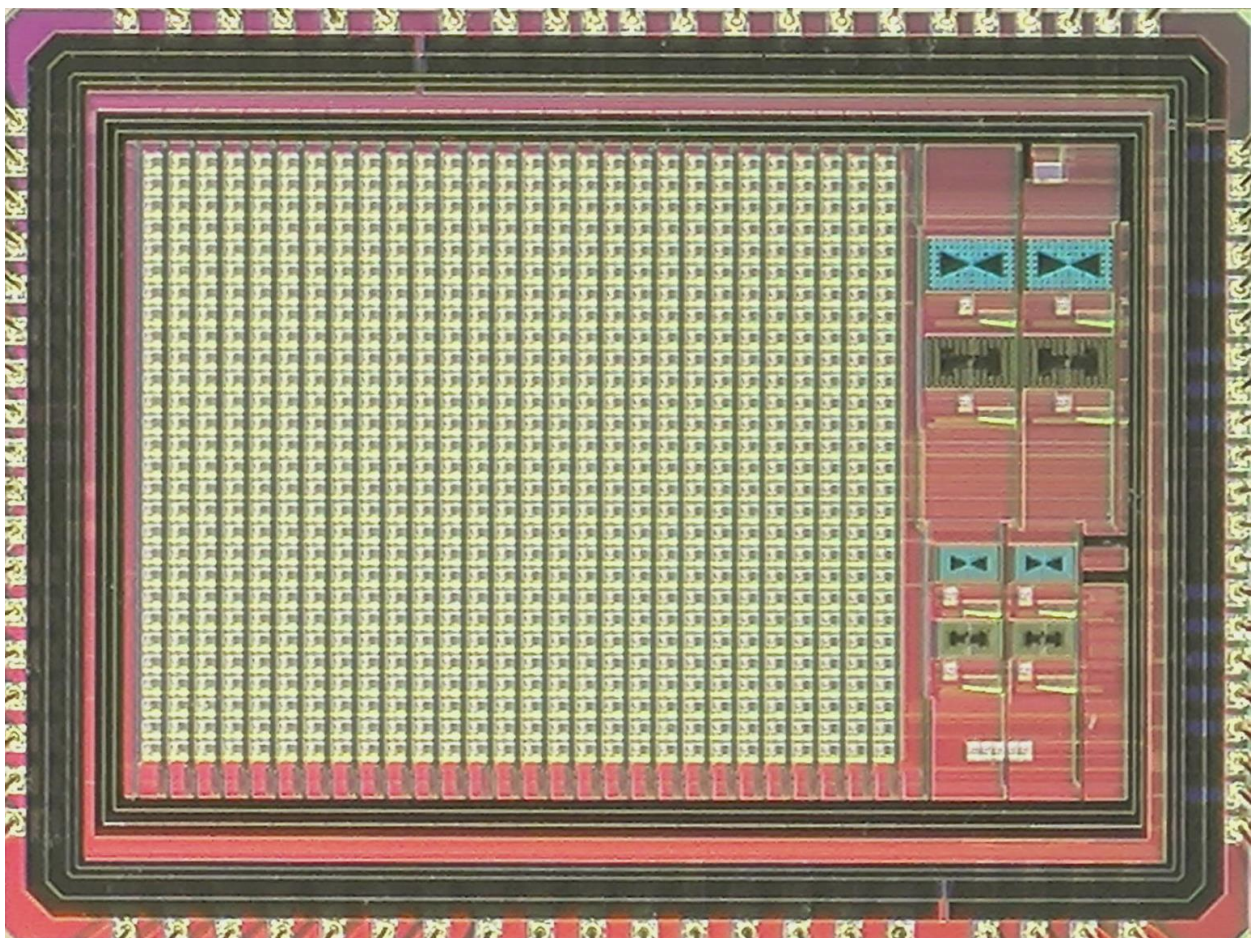


Fig. 4-1. SIRTech Chip micrograph.

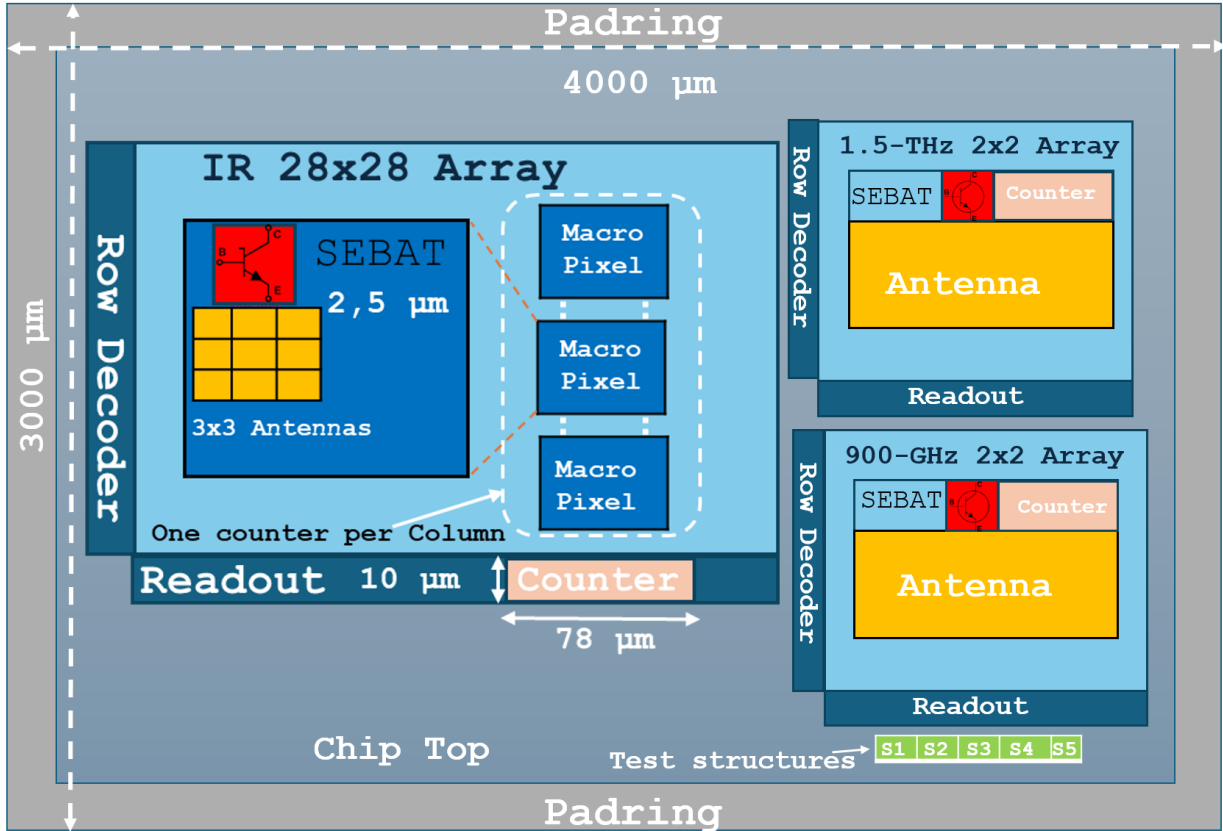


Fig. 4-2. Floorplan Organization and Interface Architecture.

The pading consists of an 84-pad interface distributed along four chip sides. Pads dedicated to SEBAT biasing (VHV, n-plus, p-well) are left unprotected to enable direct application of the required voltages.

The power distribution network is segmented into multiple isolated voltage domains: 1.2 V for digital logic, 3.3 V for analog circuits, and up to 30 V for high-voltage SEBAT biasing, reducing noise coupling between subsystems. Metal shielding structures are incorporated between arrays to prevent electrical crosstalk between readout circuits, enabling independent testing of each array

4.1.3 Hierarchical Selection Architecture of the SIRTech Chip

The SEBAT devices integrated within pixels use the optimized ring contact design (Device 02 from Chapter 3), which provides maximum electron detection efficiency.

High-Level Array Selection:

Control signals are shared among all arrays as it is shown in Fig. 4-3: RESn_ROWDEC (row decoder reset), SEL_CNT (integration window gating) and CNT_EN (counter enable), and

CLK_ROW. Three array-specific selection signals (SELECT_IR, SELECT_900GHz, and SELECT_1.5THz) determine which array responds to these shared control signals. When an array's SELECT signal is low, that array ignores all shared control inputs and remains inactive.

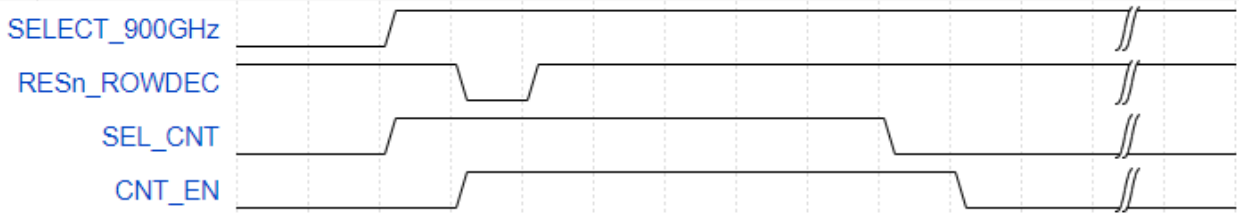


Fig. 4-3. Array selection waveforms.

The Vigilio-like test structures can be independently selected via dedicated pads separated from the arrays. These five SEBAT test structures use a shift register-based selection system, sequentially activated through clock pulse counting, as described in Chapter 3.

4.2. THz Array Design and Implementation

The 900 GHz and 1.5 THz arrays share identical architecture, readout circuitry, and SEBAT-based detection principles, differing only in antenna dimensions optimized for their respective frequencies. This section presents the common architectural framework before detailing the frequency-specific antenna implementations.

4.2.1 Circuits Pixel Architecture: Integrated Detection and Readout

The THz arrays implement the power-to-digital conversion principle introduced in Section 2.1.2, where each pixel integrates the complete signal chain from THz detection to digital output. Fig. 4-4 illustrates this architecture: the antenna-coupled FET generates a DC current (or AC if the source is modulated) proportional to incident THz power, which injects electrons into the SEBAT structure to produce avalanche pulses at a rate proportional to the THz signal amplitude. These pulses are conditioned by capacitive coupling and inverter circuitry, then accumulated by an in-pixel 12-bit counter.

Pixel Architecture and Signal Flow

Each pixel functions as a self-contained detection and digitization unit, composed of several functional blocks integrated within the pixel area (Fig. 4-4). The bow-tie antenna captures the incoming THz radiation and couples it to the FET detector, whose operation region is controlled by the gate

voltage (V_{gate}). Acting as a self-mixing detector, the FET converts the high-frequency terahertz signal into a DC voltage proportional to the incident power as described in Chapter 1. The FET drain is connected to the emitter of a passively quenched SEBAT featuring the optimized base ring contact design presented in Chapter 3 (Device 02), which provides high electron detection efficiency. Variations in the drain voltage modulate the emitter current, and since the FET signal modulates electron injection into the avalanche region, single-electron avalanche events are generated at a rate proportional to the terahertz input power. Each avalanche event produces a voltage pulse at the collector, which couples through a capacitor to an inverter input node held high by a pull-up transistor. This AC coupling circuit is necessary to isolate the high-voltage domain ($V_{HV} \leq 30$ V at the SEBAT collector) from the low-voltage digital domain (1.2 V logic). The capacitor blocks the DC component while transferring only the transient avalanche pulses, and the pull-up resistor fixes the inverter input DC bias point at the proper voltage for the 1.2 V logic domain. Without this coupling, the high SEBAT collector voltage would exceed the 1.2 V digital circuit breakdown limits and damage the inverter. Avalanche pulses pull the inverter input below threshold, generating clean 1.2 V digital output pulses. This capacitive coupling and inverter configuration effectively converts high-voltage analog avalanche pulses into low-voltage digital edges suitable for counting. The on-chip integration minimizes collector parasitic capacitance, achieving optimal single-electron counting. These digitally conditioned pulses are delivered to the in-pixel 12-bit ripple counter, which accumulates events as digital counts, completing the pixel-level detection and digitization chain.

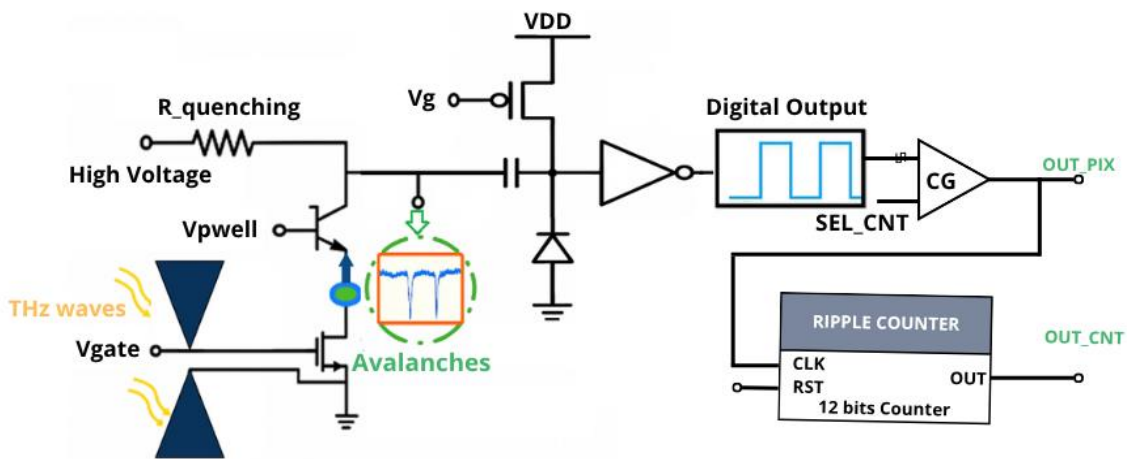


Fig. 4-4. Complete THz Pixel Architecture (THz Detection and Digital Readout).

Bow-Tie Antenna Design for THz

The THz arrays employ bow-tie antennas (Fig. 4-5) adapted from previous designs [68] to couple terahertz radiation to the integrated FET detectors. At 900 GHz ($\lambda \approx 330 \mu\text{m}$) and 1.5 THz ($\lambda \approx 200 \mu\text{m}$), the antenna dimensions differ according to the operating wavelength, as visible in the chip floorplan. The bow-tie antennas are connected between the gate and source terminals of the FET detector. The larger antenna dimensions at THz arrays provide sufficient area within the pixel for implementing the complete readout circuitry, including the 12-bit counter and pulse conditioning circuits.

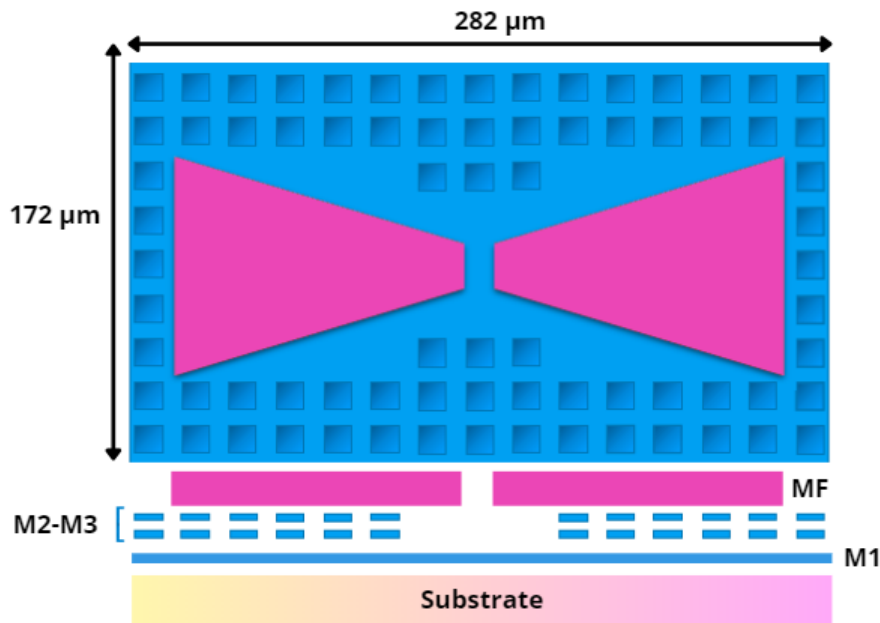


Fig. 4-5. Antenna Design for 900 GHz Detection.

Counter Architecture and Operation

The 12-bit ripple counter integrated in each pixel offers a range from 0 to 4095, which provides sufficient dynamic range to accurately capture the expected avalanche event rates under typical terahertz illumination conditions. The counter is constructed from D-type flip-flops organized into 12 logical cells and supports bidirectional operation. The counting direction is determined by the UP-DOWN control signal, allowing the device to operate in either up-counting or down-counting mode. This flexibility enables advanced measurement schemes, such as background subtraction and differential detection, particularly useful when the system is synchronized with modulated terahertz sources.

By alternating between up-counting during signal+background periods and down-counting during background-only periods, the counter directly accumulates the differential signal, effectively sup-

pressing common-mode noise and background contributions [6]. To avoid count overflow and underflow issues, the counter implements dedicated saturation logic: during up-counting, when the maximum value of 4095 is reached, the logic prevents further increments; similarly, during down-counting, the minimum value of 0 is maintained, preventing further decrements. This saturation mechanism is controlled within the first cell through an AND gate. When the gate output is low, incoming pulses are blocked at the input stage, effectively disabling counting operation regardless of further SEBAT output events. The counter is governed by several control signals that define its operation modes:

- SEL_CNT (Gating Control) defines the integration window during which avalanche events are counted. This signal controls a dedicated clock-gating cell that ensures clean window boundaries by filtering glitches during enable transitions. When SEL_CNT = 0, incoming pulses are blocked; when SEL_CNT = 1, pulses are passed to both the counter and pixel output simultaneously.
- CNT_EN (Counter Enable) allows the counter pass the pulses to the column decoder.
- PIX_EN (Direct Pixel Enable): Enables direct readout of digitized pulses from the inverter output, bypassing the counter accumulation. This mode is used in case that the counter doesn't work properly.
- RST (Reset): An active-low signal that clears the counter to zero prior to the start of each new integration period.

At the end of each integration cycle, the counter output is presented as a 12-bit parallel output. This output is transferred to the column decoder during the readout phase, making the digitized signal ready for serial transmission.

Fig. 4-6 represents the timing diagram of the pixel's counter bidirectional operation. Cadence Virtuoso simulation results validate the bidirectional counting and saturation protection capabilities of the pixel counter. Realistic SEBAT cathode pulses, generated from a TCAD-extracted SPICE model (Chapter 2), are used as test stimuli. The diagram illustrates down-counting operation with the UP_DOWN signal held high, where each avalanche pulse decrements the counter value and saturation logic prevents underflow below zero. Controlled integration windows are defined by the SEL_CNT gating signal, which safely manages pulse propagation and mode transitions. Upon switching to up-counting mode (UP_DOWN low), subsequent cathode pulses increment the counter accordingly. The simulation confirms the correct operation of bidirectional counting, saturation logic, and window control under realistic input signals.

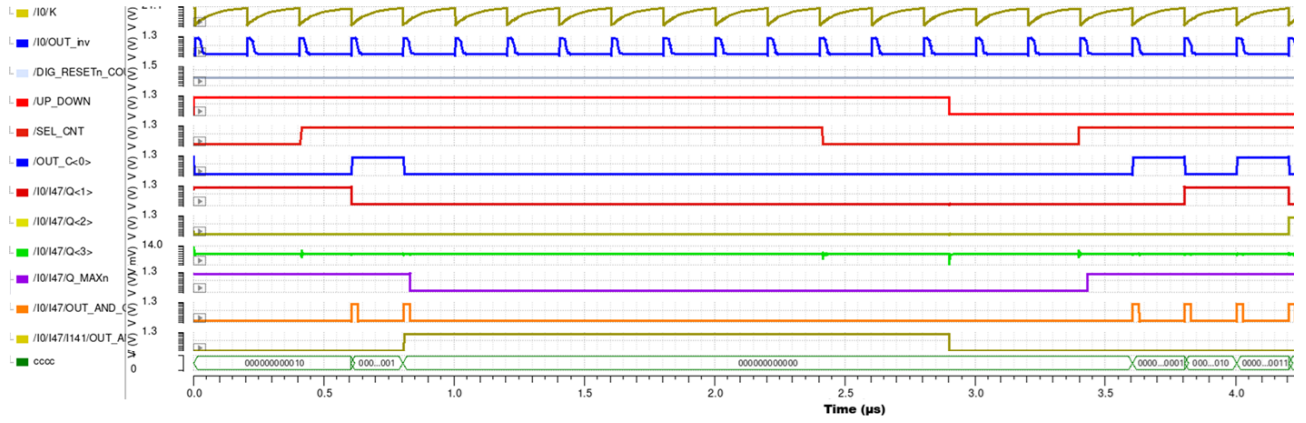


Fig. 4-6. Bidirectional Counter Operation and Saturation Logic Validation.

4.2.2 Array Architecture and Configuration

The THz arrays implement a hierarchical control structure with three main functional blocks (Fig. 4-7). The row decoder provides sequential pixel selection through row-by-row addressing, controlled by reset (RESn_ROWDEC) and clock (CLK_ROW) signals. Each pixel integrates a digital counter for direct pulse counting, converting SEBAT avalanche events into digital counts that encode the incident terahertz power.

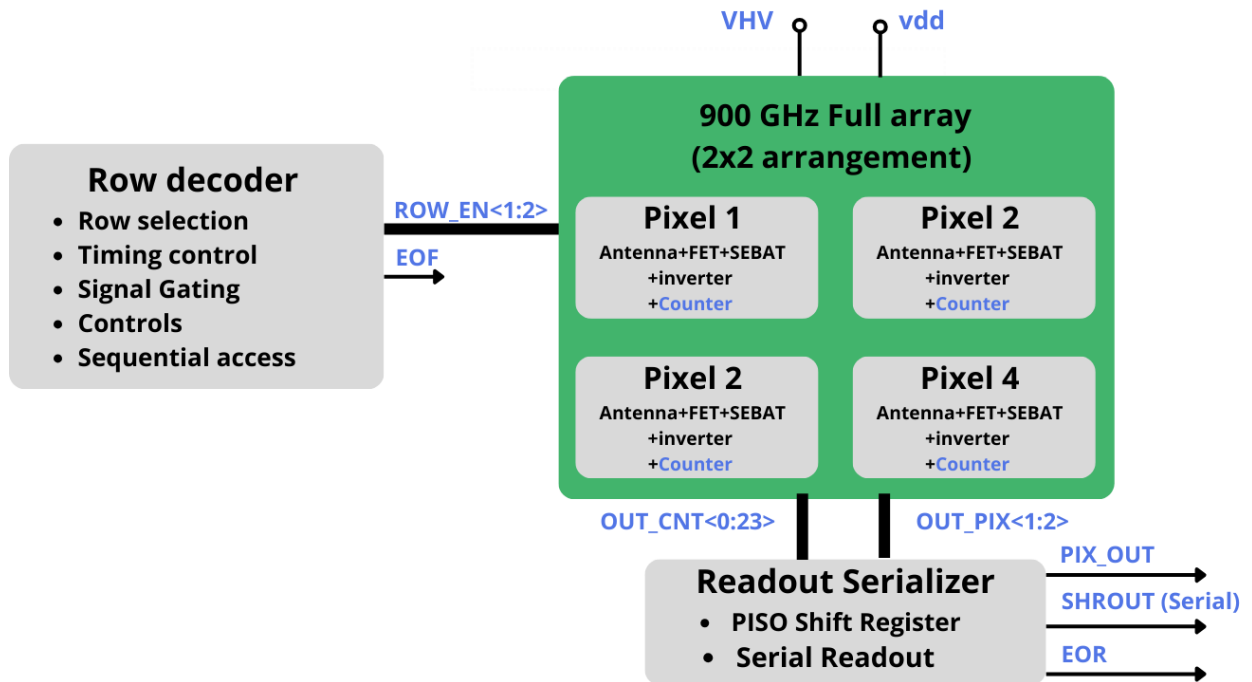


Fig. 4-7. 900 GHz array architecture.

The column decoder implements a Parallel-In Serial-Out (PISO) shift register architecture, where counter values from all pixels in the selected row are loaded in parallel and then shifted serially to a single output line. This serial readout generates synchronized digital data streams including pixel values (PIX_OUT), end-of-row (EOR), and End-Of-Frame (EOF) timing signals for each array.

Table 4-1 provides a complete specification of all control and interface signals for the 900 GHz array. This architecture follows the proven design methodology established in the Vigilio chip, adapted specifically for the 900 GHz detection requirements and SEBAT-based readout integration.

Table 4-1. 900 GHz Array Control Signals.

Signal Name	Direction	Width	Description
ROW_EN<1:2>	Input	2	Row selection signals
CLK_ROW	Input	1	Row decoder clock
RESn_ROWDEC	Input	1	Row decoder reset
CNT_EN	Input	1	Counter enable
SEL_CNT	Input	1	Integration window gating
UP_DOWN	Input	1	Counter direction
VHV<2>	Input	1	High voltage bias ($\leq 30V$)
OUT_CNT<0:23>	Output	24	Parallel counter data
SHROUT	Output	1	Serial data output
EOF<2>	Output	1	End-of-frame flag

4.2.3 Row Decoder Architecture

The 2×2 THz array incorporates a shift register–based row decoder (Fig. 4-8), located on the left side of the array, to enable sequential selection of individual pixel rows. The decoder employs a 2-stage shift register, with each stage corresponding to a distinct row.

At any time, only one row is active, with a single '1' bit propagating through the register while all other stages remain at '0', thereby ensuring unambiguous row selection.

The row decoder is responsible for the management of row selection and timing, controlling the activation of pixel rows during sequential detection cycles. It also coordinates detection window

gating and pixel enable signals to facilitate accurate event accumulation and directly actuates pixel output lines for robust readout.

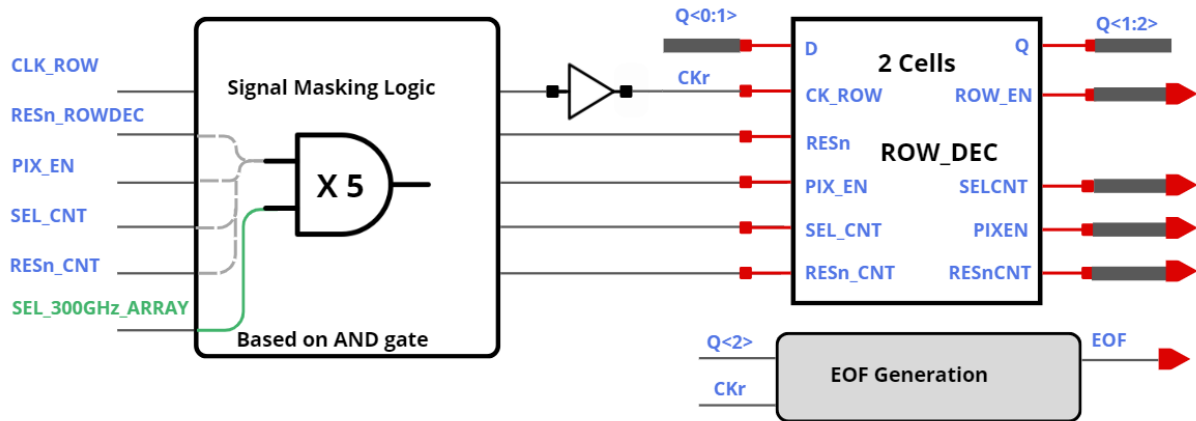


Fig. 4-8. Row Decoder Schematic Architecture.

To enhance operational reliability, the decoder employs a dual flip-flop architecture with two D flip-flops per row, operating on both rising and falling clock edges. This configuration prevents glitches and protects against setup and hold time violations that could corrupt the row selection sequence, causing the shift register to lose the '1' bit or generate multiple simultaneous '1' bits. The detailed schematic of the row decoder cell implementing the dual flip-flop architecture and signal gating is presented in Fig. 4-9.

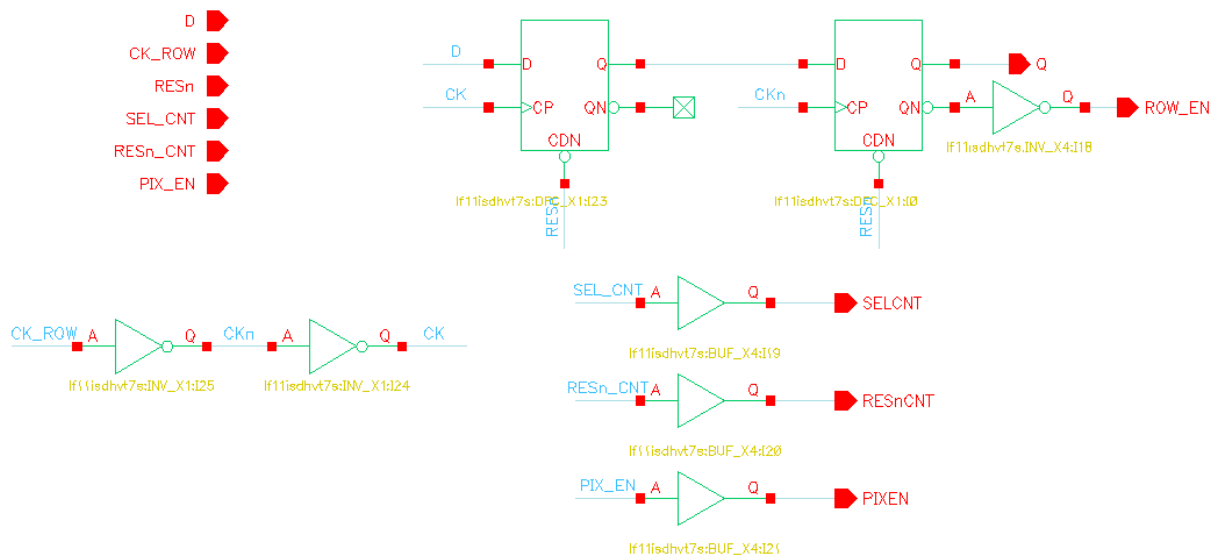


Fig. 4-9. Row decoder cell (ROW_DEC) architecture with dual D flip-flop design, row enable generation (ROW_EN), and control signal gating (SEL_CNT, PIX_EN, RESn_CNT).

This robust design is particularly important for arrays with large pixel pitch where routing delays become significant. Furthermore, the row decoder provides an end-of-frame output signal that flags the completion of a full array scan. This signal serves as a synchronization marker for the external control system, enabling coordinated acquisition of consecutive data frames.

4.2.4 Column Decoder Architecture

The 2×2 THz array incorporates a PISO shift register (Fig. 4-10) located at the bottom of the array to convert the 12-bit parallel counter outputs into a serial data stream for off-chip transmission.

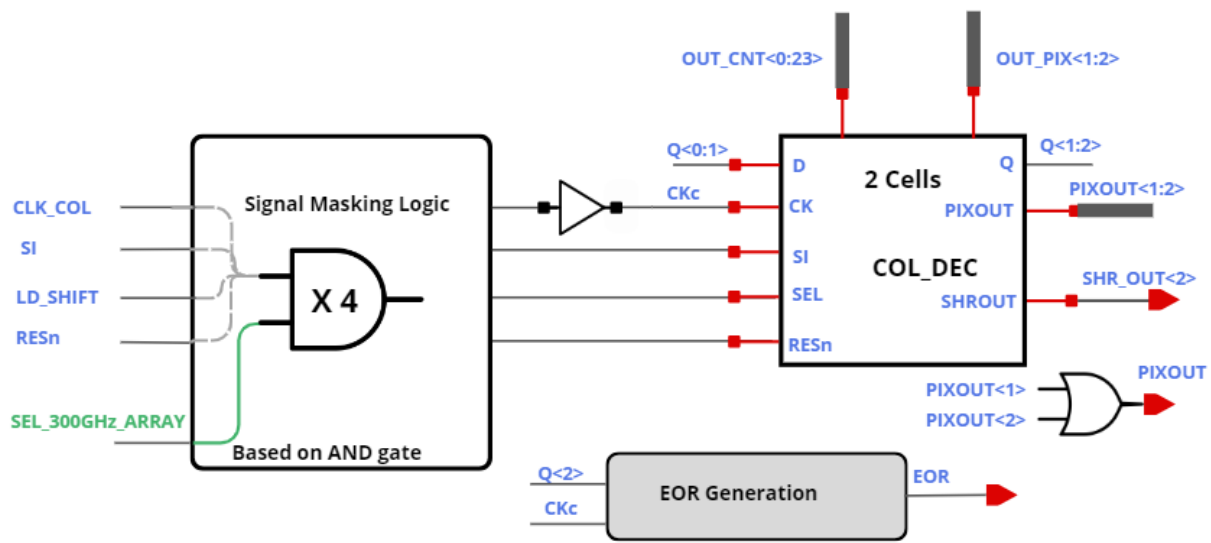


Fig. 4-10. Column Decoder Circuit Architecture.

The column decoder works in coordination with the output shift register to control the continuous serial data stream and arrange the reading sequence of pixels, functioning in tandem with the row decoder for full array addressing.

Key control signals governing the column decoder operation include:

- LD_SHIFT: A load/shift control that latches parallel data from the active row's pixels into the shift register and initiates the serial shifting process.
- CLK_COL: A clock signal, governing the timing for serial data output.

Upon activation of a specific row by the row decoder, both pixel counters in that row present their 12-bit values in parallel to the column decoder's shift register. The shift register, sized to accommodate the combined 24 bits (12 bits × 2 pixels), loads the data simultaneously and shifts it out

serially over 24 clock cycles. The detailed schematic of the PISO shift register cell implementing the load and shift functionality is presented in Fig. 4-11. The array operates in sequential row-by-row mode: each row is selected, integrates (SEL_CNT high), then is immediately read out before proceeding to the next row.

For the complete 2×2 array, the full frame readout entails sequentially reading all four pixels (across 2 rows and 2 columns). The architecture guarantees synchronization between data acquisition from the pixel counters and the serial transmission stages, ensuring integrity and accuracy of the readout.

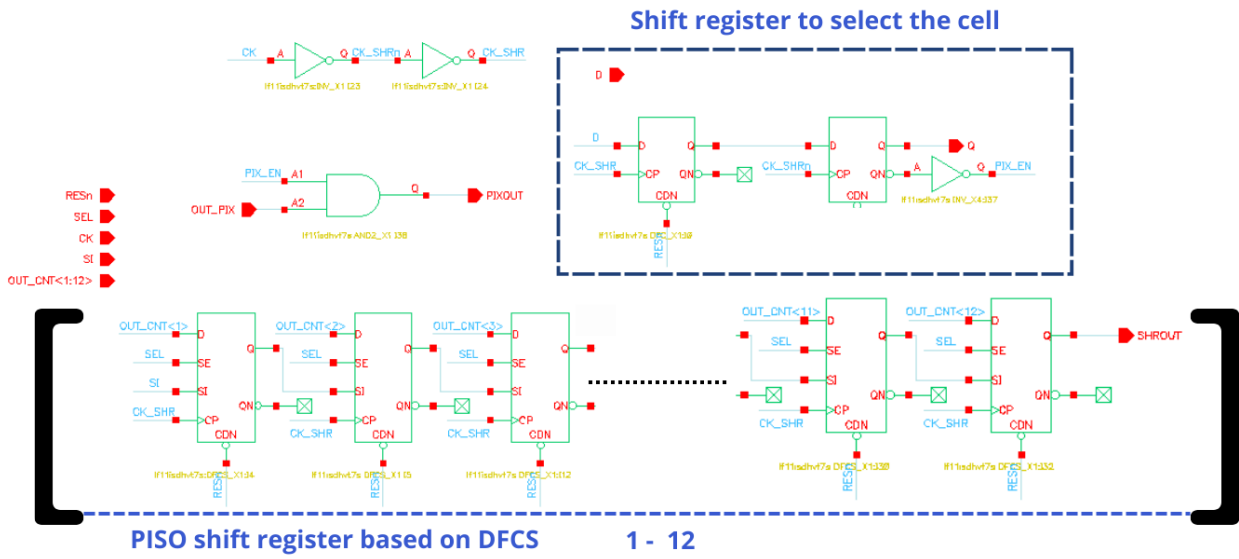


Fig. 4-11. Complete column decoder cell schematic: DFCS-based PISO serializer with integrated pixel output and selection control.

4.2.5 THz Array Complete Frame Readout Timing Diagram and simulation

Fig. 4-12 shows the complete frame acquisition and readout timing for the 2×2 THz array based on a sequential row-by-row scanning operation. The sequence begins with array selection (SELECT_300GHz high), followed by row decoder initialization (RESn_ROWDEC reset). Row selection occurs through CLK_ROW pulses: one pulse selects the first row, two pulses select the second row, as indicated by ROW_EN<1:2>.

After row selection, the counter is reset (RESn_CNT) and then enabled (CNT_EN) to prepare for pulse reception. However, counting only begins when SEL_CNT goes high; defining the integration window during which SEBAT avalanche events are accumulated. The UP_DOWN signal controls the counting direction for optional differential detection schemes. Counter states display "updating" during integration, followed by "Row 1 OUT" and "Row 2 OUT" data output phases

showing the 24-bit parallel counter outputs (OUT_CNT<0:23>) and pixel outputs (OUT_PIX<0:1>).

At the end of integration, LD_SHIFT pulses low to load the parallel counter data (24 bits: 12 bits $\times$ 2 pixels) from the selected row into the shift register, then returns high to initiate serial shifting. CLK_COL provides the shift clock, with each clock edge shifting out one bit on the SHROUT line. The SHROUT signal displays the serial bit stream during the 24-cycle readout period for each row.

The diagram also illustrates the diagnostic bypass mode: when PIX_EN is high, SEBAT avalanche pulses are routed directly to PIXOUT (shown as irregular pulses representing stochastic avalanche events), bypassing the counter entirely for troubleshooting counter malfunctions. The EOF signal pulses high to mark frame completion, enabling synchronization for consecutive frame acquisitions.

At the end of integration, LD_SHIFT pulses low to load the parallel counter data (24 bits: 12 bits $\times$ 2 pixels) from the selected row into the shift register, then returns high to initiate serial shifting through CLK_COL. The SHROUT signal shows the serialized data output with progressive bit extraction (values 15 and 29 indicate the shifting process).

The diagram also illustrates the diagnostic bypass mode: PIX_EN can directly route SEBAT outputs to PIXOUT, bypassing the counter entirely for troubleshooting counter malfunctions. The EOF signal pulses high to mark frame completion, enabling synchronization for consecutive frame acquisitions.

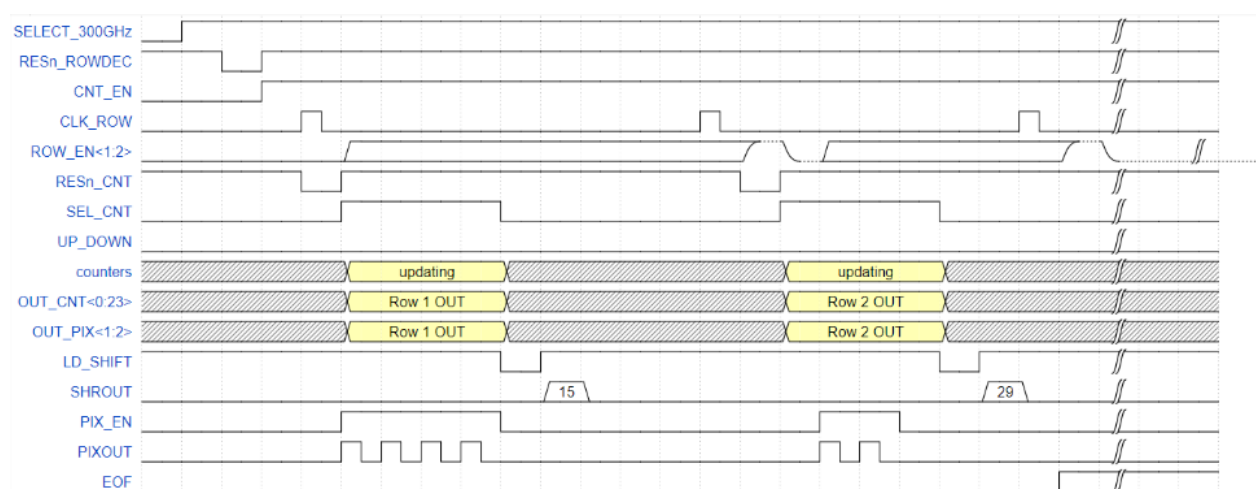


Fig. 4-12. Complete Frame Readout Timing Sequence for 2 $\times$ 2 THz Array with Sequential Row Scanning.

Cadence Virtuoso post-layout simulations, shown in Fig. 4-13, confirm the timing diagram behavior for the 2×2 THz array frame acquisition. The simulation validates the complete sequential scanning operation across two rows (labeled "First row" and "Second row"). Top traces (K<1> through K<4>) show SEBAT cathode pulses, with some pixels intentionally disabled on each row to verify independent pixel operation. The timing clearly shows two operational phases per row:

- 1) "The array is sensitive to incoming THz radiation" during SEL_CNT high (integration windows at ~0-12μs and ~22-36μs), when counters accumulate SEBAT events;
- 2) "Upload and reading out the signals" when SEL_CNT is low (~12-22μs and ~34-48μs), during which LD_SHFT loads counter data into the column decoder and CLK_COL shifts it serially. When all pixels are enabled together during the reading phase (SEL_CNT low), no pulses reach the counters, confirming proper gating control. The SHROUT signal shows the exact digital values that were stored in the counters, verifying correct parallel-to-serial conversion and data integrity. The EOF signal pulses after the third CLK_ROW pulse, correctly indicating frame completion after both rows have been read out.

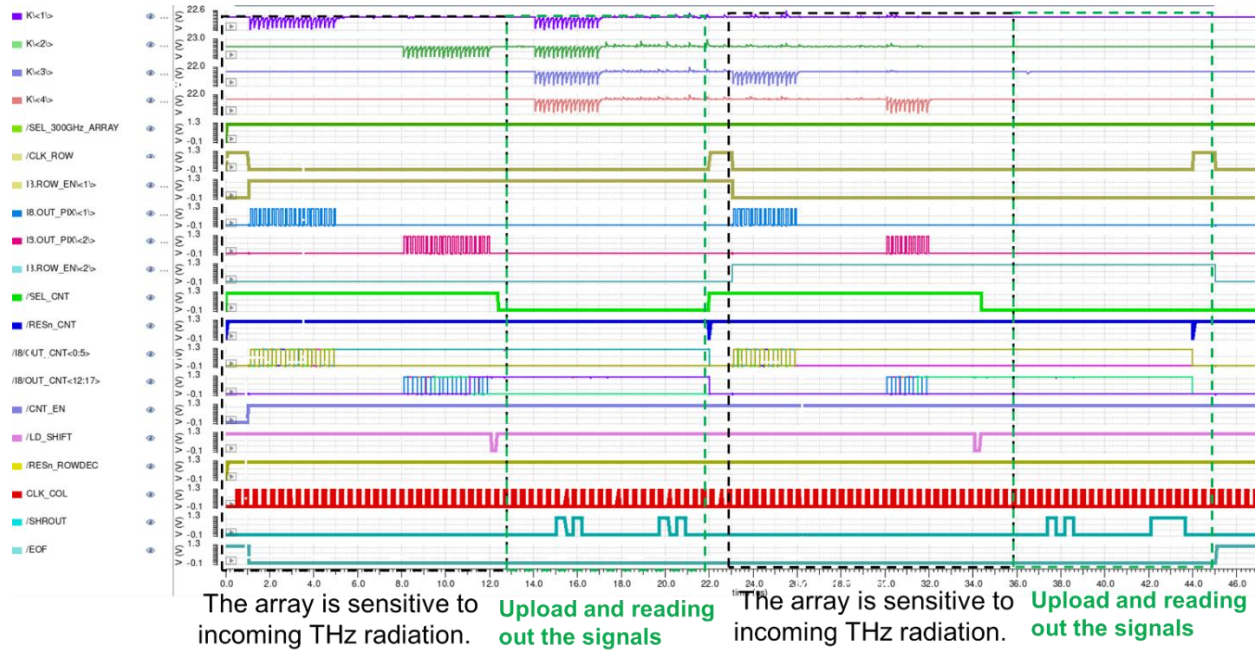


Fig. 4-13. Post-Layout Simulation of Sequential Row Readout for 2×2 THz Array.

This section presented the architecture and operational principles of the THz imaging arrays. The implementation of both arrays (900 GHz and 1.5 THz) follows the same architectural and operational framework, except the antennas have a smaller size for the 1.5 THz, since they are tuned for the higher frequency.

4.3. IR Array Design and Implementation

The IR array is configured for detection in the long-wavelength infrared (LWIR) band (8–14 μm). The array consists of 84×84 pixels arranged in a 28×28 macro-pixel array with $86 \mu\text{m} \times 69 \mu\text{m}$ pitch. Each macro-pixel contains 3×3 FET detectors with $7.9 \mu\text{m}$ spacing. This array adopts a SEBAT-based readout circuit, where each macro-pixel integrates nine bow-tie antennas (approximately $2 \mu\text{m}$ arm length) linked to a shared SEBAT avalanche device. The antennas are designed for infrared radiation in the 8–14 μm wavelength range, which aligns with the thermal emission spectrum of room-temperature objects.

4.3.1 IR Pixel Architecture and Signal Flow

The IR array targets the long-wavelength infrared (LWIR) band (8–14 μm), requiring significantly smaller antenna structures compared to the THz arrays operating at 900 GHz ($\lambda \approx 330 \mu\text{m}$) and 1.5 THz ($\lambda \approx 200 \mu\text{m}$). The IR pixel implements the same fundamental architecture as the THz pixel, utilizing a bow-tie antenna coupled to a SEBAT avalanche detector for infrared photon detection as shown in figure Fig. 4-14.

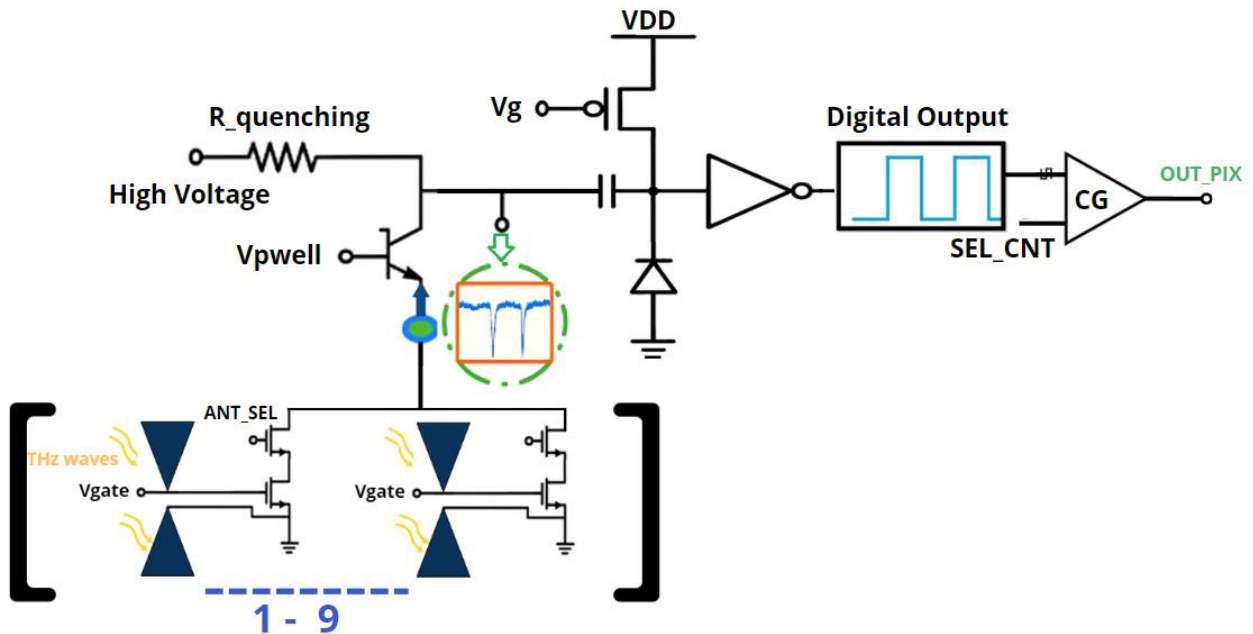


Fig. 4-14. Complete IR Pixel Architecture (IR Detection and Digital Readout).

However, two key distinctions differentiate the IR pixel from the THz implementation: each IR macro pixel integrates 9 small bow-tie antennas connected to a single SEBAT structure, and the 12-bit counters are located in the column decoder rather than within each pixel.

Bow-Tie Antenna Design for IR Detection

The IR pixel employs bow-tie antennas adapted from previous designs [64], with each pixel occupying an $8\ \mu\text{m} \times 8\ \mu\text{m}$ footprint. The antennas are fabricated using the available metal layers (M1-M4) in the CMOS process, with the ground plane implemented in metal 1. Fig. 4-15 shows the detailed layout with the 9-antenna array arrangement in the top three panels and a zoomed view of a single bow-tie antenna structure in the lower panel, clearly depicting the metal layer stack (M1-M4) and the antenna geometry. The compact antenna dimensions, with arm lengths of approximately $2\ \mu\text{m}$ each, enable tight spatial integration of the 9-antenna array within the $8\ \mu\text{m}$ pixel footprint.

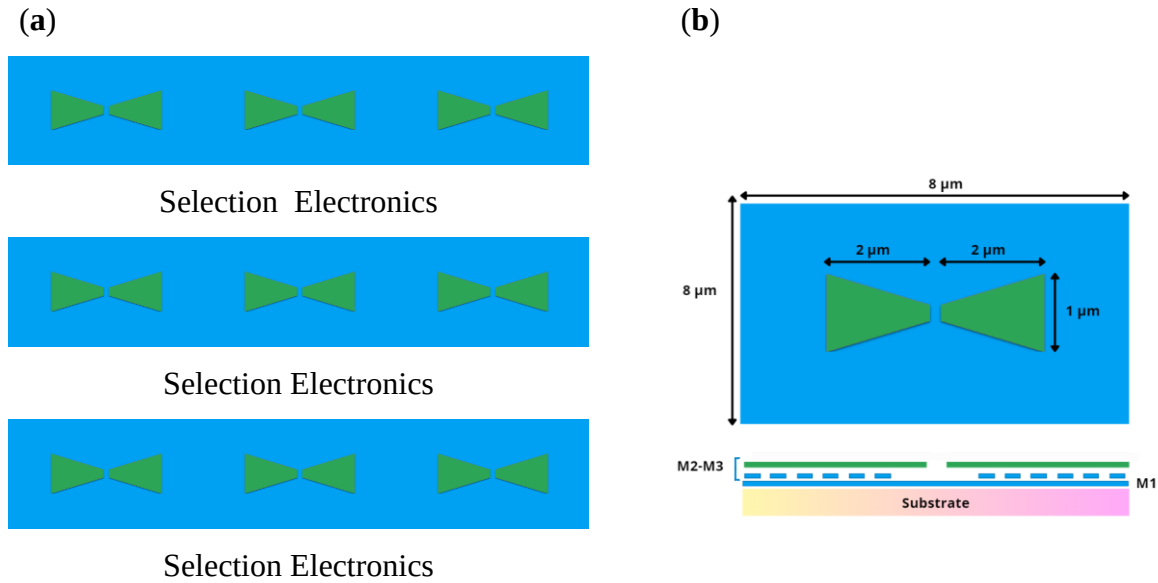


Fig. 4-15. IR Pixel Layout with 9-Antenna Configuration. (a) 3×3 array of bow-tie antennas within a single pixel. (b) Single antenna cross-section ($8\ \mu\text{m} \times 8\ \mu\text{m}$) showing metal layer stack (M1-M2, M3) and substrate.

IR Antenna selection mechanism

The IR pixel implements a 9-cell shift register-based antenna selection mechanism (Fig. 4-16) that enables programmable configuration of the effective detection aperture. Each cell controls the connection of one antenna to the SEBAT input: a '1' bit connects the antenna, while a '0' bit disconnects it. This programmable selection enables flexible tradeoff between spatial resolution and

sensitivity: connecting all 9 antennas maximizes signal collection efficiency for low-light imaging, while connecting fewer antennas (or a single antenna) reduces the effective pixel aperture for improved spatial resolution when sufficient signal is available.

The selection system operates through DATA and CLOCK inputs. When /RESETn is pulsed low, all antenna selection outputs (ANT_SEL<1:9>) default to high, connecting all 9 antennas to ensure maximum sensitivity immediately after initialization. To customize the configuration, a 9-bit pattern is serially shifted into the register: each bit position corresponds to one antenna, and the pattern propagates through the chain with each CLOCK pulse until the desired connection pattern is established across all cells. Each cell utilizes double-sampling D flip-flops to ensure robust state transitions and prevent glitches during the shift operation.

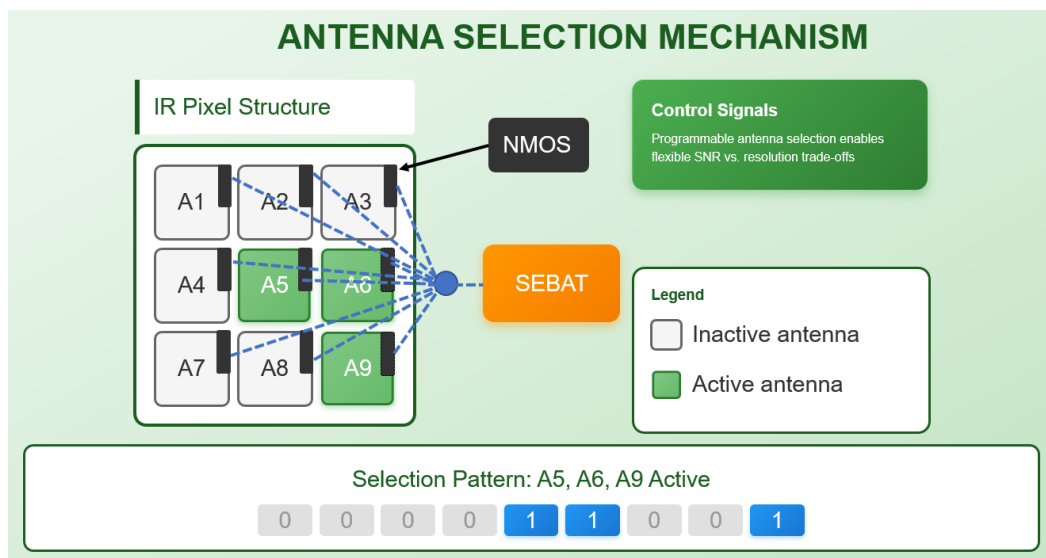


Fig. 4-16. Flexible Antenna Selection Mechanism for 9-Antenna IR Pixel.

The simulation in Fig. 4-17, demonstrates the shift register operation: after reset, all antenna selection signals (ANT_SEL<1:9>) start at logic high. By shifting a binary pattern through DATA, specific antennas can be selectively connected or disconnected: in this example, ANT_SEL<1:8> transition to low while ANT_SEL<9> remains high.

This programmable selection mechanism enables two distinct operational modes with different performance tradeoffs:

Parallel mode (all 9 antennas connected): It provides low spatial resolution due to the large effective pixel aperture ($\sim 9 \times$ single antenna area), but achieves high SNR by collecting signal from all antennas simultaneously and enables high frame rate with a single readout cycle per pixel.

Sequential scanning mode (one antenna at a time): It achieves high spatial resolution by reducing the effective aperture to a single antenna, but requires $9\times$ longer acquisition time (sequential readout of each antenna position) and produces lower SNR per measurement due to reduced collection area.

This flexibility allows the imaging system to be optimized for different application requirements, trading off resolution, sensitivity, and acquisition speed as needed.



Fig. 4-17. Antenna Selection Shift Register Timing Simulation.

4.3.2 Array Architecture and Configuration

Fig. 4-18 shows the array architecture implementing a hierarchical structure with four main functional blocks. The row decoder selects active rows in the 28×28 macro-pixel array, controls timing for the IR detection process, and manages row selection signals for sequential scanning. Each row undergoes a complete measurement cycle before advancing to the next row. The ARRAY_IR features a 28×28 macro-pixel arrangement where each contains 9 pixels with small bow-tie antennas connected to a single SEBAT-based readout circuit. The column readout circuit processes signals from the array and integrates multiple functions: 28 dedicated 12-bit counters (one per column), PDN (Power Down Network) transistors for power management, and parallel-to-serial shift registers for data serialization. Unlike the THz arrays where counters reside within pixels, the IR architecture implements column-level counting, with each counter accumulating avalanche events from its corresponding column during the active integration window. This architectural choice is driven by area efficiency: with 784 macro-pixels (28×28 array), integrating 12-bit counters within each

pixel would result in prohibitively large pixel area and reduced fill factor. The column-level approach requires only 28 counters (one per column) instead of 784, significantly reducing the required silicon area.

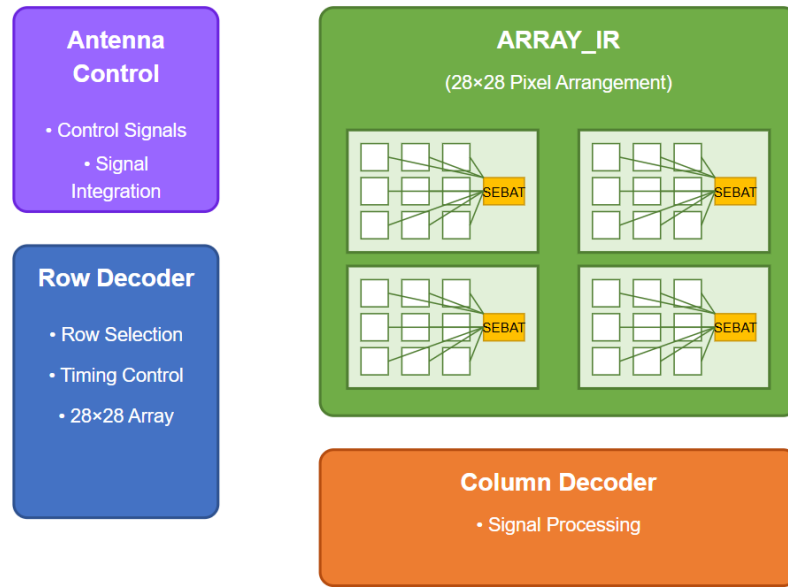


Fig. 4-18. The array architecture implementing a hierarchical control structure with four main functional blocks.

4.3.3 IR Row Decoder Architecture

The 28×28 IR array incorporates a shift register-based row decoder as shown in Fig. 4-19, located on the left side of the array, to enable sequential selection of individual macro-pixel rows. The decoder employs a 28-stage shift register, with each stage corresponding to a distinct row. At any time, only one row is active, achieved by propagating a single '1' bit through the register, thereby ensuring unambiguous "one-hot" row activation. The row decoder is responsible for the management of row selection and timing, controlling the activation of pixel rows during sequential detection and readout cycles: SEL_CNT controls the integration window gating, while PIX_EN enables direct external readout of the SEBAT counts, bypassing the counter readout path for diagnostic purposes. The row_ENn signal masks inactive rows, ensuring non-conflicting operation by keeping all non-selected rows silent during single-row readout.

Additionally, the row decoder generates row-specific reset signals (RESn_CNT) for the column-level counters, ensuring proper synchronization between row activation and counter operation.

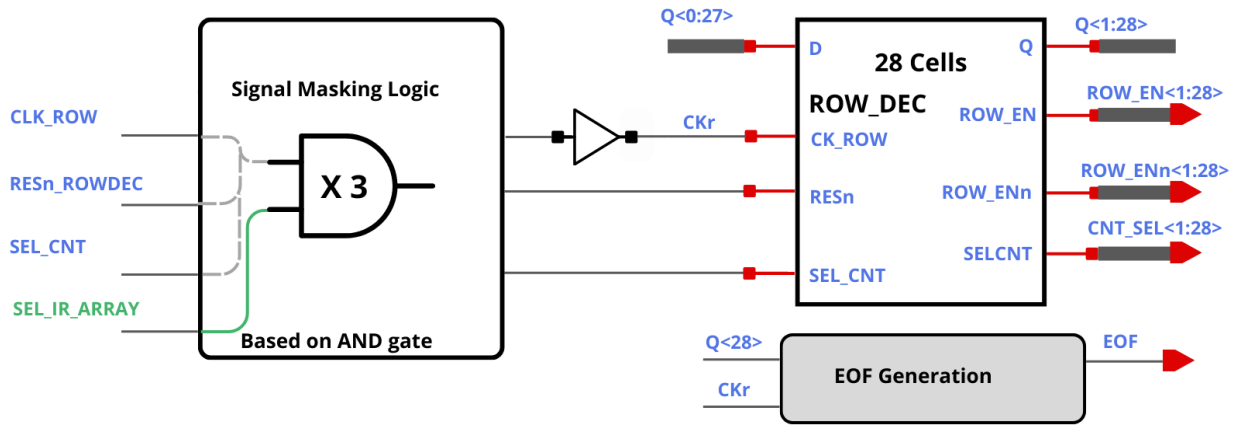


Fig. 4-19. Shift register-based row decoder circuit for the 28×28 IR array.

IR Column Decoder Architecture

The 28×28 IR array incorporates a column decoder (Fig. 4-20) located at the bottom of the array to manage output signal processing and serial data extraction from the pixels. Unlike the THz array where counters reside within pixels, the IR column decoder contains the counting circuits themselves, receiving raw gated SEBAT avalanche pulses directly from pixel outputs and performing on-chip digitization at the column level.

Architecture and Counter Integration

The column decoder is composed of 28 cells, with each cell corresponding to one column of the array and containing a dedicated 12-bit counter. When the row decoder activates a specific row, all 28 pixels in that row output their gated SEBAT avalanche pulses directly to their respective column counters. During the integration window defined by SEL_CNT, each column counter accumulates avalanche events from its corresponding active pixel. The column decoder employs DFCS (D Flip-Flop with Clear and Set) flip-flops to load counter outputs and convert them to serial format through a parallel-to-serial shift register architecture. The column decoder works in coordination with the output shift register to control the continuous serial data stream and arrange the reading sequence of pixels, functioning in tandem with the row decoder for full array addressing.

Control Signals and Operation Key

Control signals governing the column decoder operation include:

LD_SHIFT: A load/shift control that latches parallel counter data from all 28 columns into the shift register and initiates the serial shifting process.

CLK_COL: A clock signal that sequences the shift operation, governing the timing for serial data output.

RESn_CNT: Reset signal for the column counters, synchronized with row transitions to clear accumulated counts before the next row's integration period.

Readout Sequence

Upon row activation, all 28 column counters accumulate events during the integration window. At the end of integration, LD_SHIFT triggers parallel loading of 336 bits (12 bits $\times$ 28 columns) into the shift register, which then serially outputs data over 336 clock cycles. Complete frame readout of the 28 $\times$ 28 array requires sequential processing of all 28 rows.

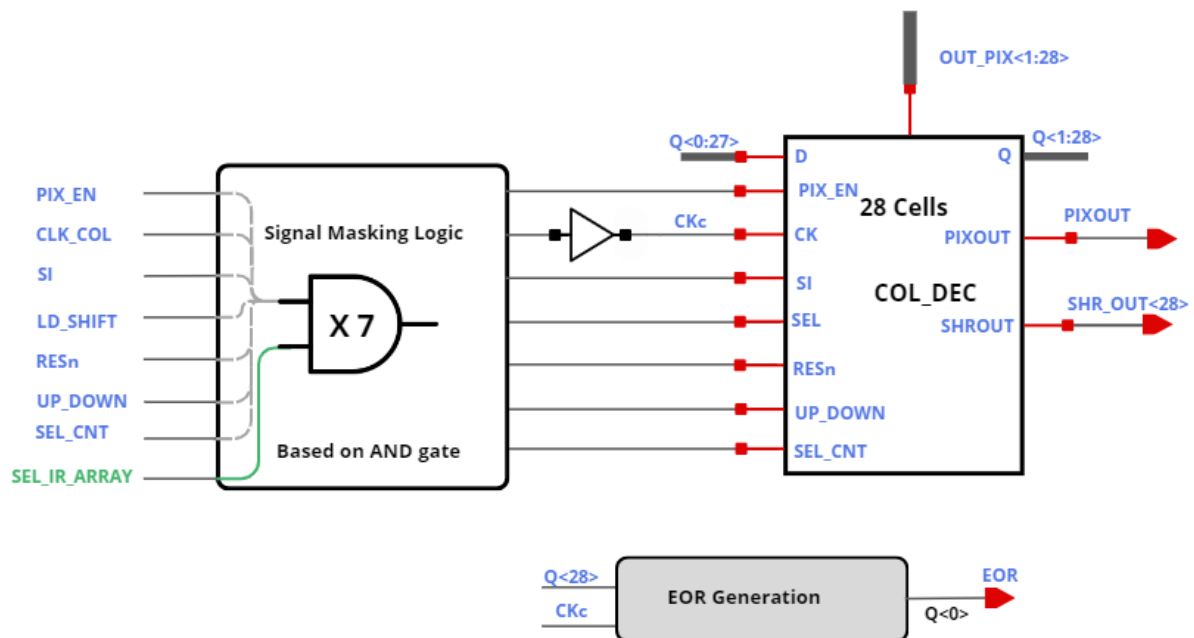


Fig. 4-20. IR Array Column Decoder Schematic Column decoder circuit for the 28 $\times$ 28 IR array.

The column decoder includes diagnostic functionality to bypass counters and directly output SE-BAT pulses when required for testing.

IR array Driving Waveforms

The complete frame readout timing diagram for the 28 $\times$ 28 IR array demonstrating the sequential row-by-row scanning operation is shown in Fig. 4-21. The sequence begins with array selection (SELECT_IR high), followed by row decoder initialization (RESn_ROWDEC reset). Row selection occurs through CLK_ROW pulses: one pulse selects the first row, two pulses select the second row, and so forth through all 28 rows, as indicated by ROW_EN<1:28>. After row selection, the

column counters are reset (RESn_CNT) and prepared for pulse reception. However, counting only begins when SEL_CNT goes high; defining the integration window during which SEBAT avalanche events from the active row's pixels are accumulated in their respective column counters. The UP_DOWN signal controls counting direction for optional background subtraction or differential detection. At the end of integration, LD_SHIFT pulses low to load the parallel counter data (336 bits: 12 bits $\times$ 28 columns) from all column counters into the shift register, then returns high to initiate serial shifting through CLK_COL. The SHROUT signal shows the serialized data output with bit counts (15, 29) indicating progressive data extraction from the shift register over 336 clock cycles per row. The diagram also illustrates the diagnostic bypass mode: PIX_EN can directly route SEBAT outputs from all 28 pixels to OUT_PIX<1:28> and PIXOUT, bypassing the column counters entirely for troubleshooting counter malfunctions. Counter states display "updating" during integration, followed by "Row 1 OUT" and "Row 2 OUT" data output phases showing OUT_CNT<0:336>. The EOF signal pulses high after completing all 28 rows to mark frame completion, enabling synchronization for consecutive frame acquisitions.

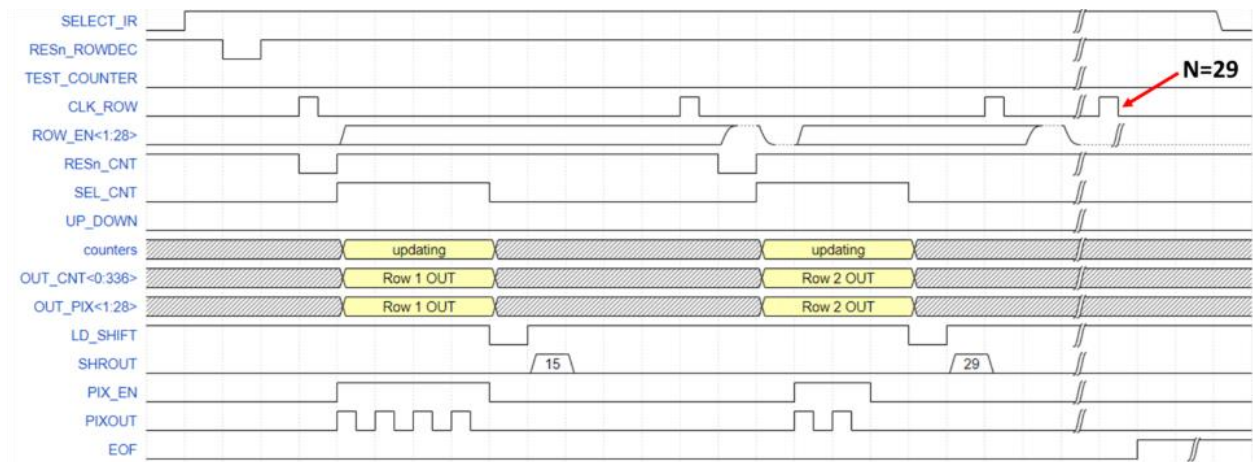


Fig. 4-21. IR Array Sequential Readout Timing Diagram for 28 $\times$ 28 Array.

IR Array Post-Layout Timing Simulation

The simulation validates the complete sequential scanning operation across two rows (labeled "First row" and "Second row") shown in Fig. 4-22. Top traces (K<2>, K<30>) show SEBAT cathode pulses arriving from IR pixels during integration windows. The timing shows two operational phases per row: (1) "The array is sensitive to incoming IR radiation" during SEL_CNT high (integration windows at ~ 0 -14 μ s and ~ 22 -36 μ s), when column counters accumulate SEBAT avalanche events from active pixels, and (2) "load and reading out the signals" when SEL_CNT is low (~ 14 -22 μ s and ~ 36 -44 μ s), during which LD_SHIFT loads the 336-bit parallel counter data

(28 columns $\times$ 12 bits) into the shift register and CLKC shifts it serially. The row enabling signals (ROWEN<1:3>) demonstrate proper sequential one-hot row activation through CLK_ROW pulses. Column counter outputs IPX_OUT<2>, <23>, <26>, <15>) show accumulated values being held during integration and transferred during readout. The OUT_CNT<1> and OUT_CNT<2> signals display the serial data streams being extracted during each row's readout phase, with /SHROUT providing the final serialized output. The simulation verifies correct parallel-to-serial conversion and data integrity, confirming that the column-level counting architecture successfully performs infrared event accumulation and serial data extraction.

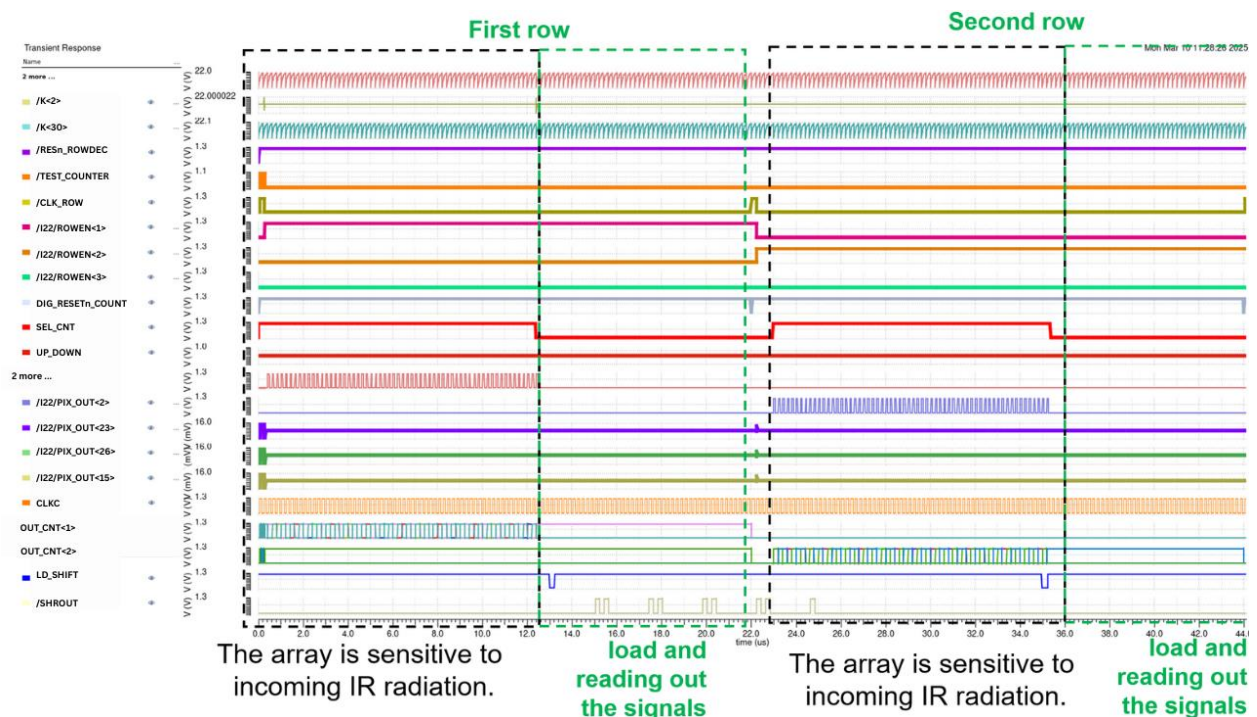


Fig. 4-22. Post-layout simulation of the IR array.

4.3.4 The TOP Level Simulation

Top-level simulation (Fig. 4-23) demonstrated coordinated yet independent operation among all arrays, each addressed via dedicated selection signals and sharing common clock and conversion infrastructure.

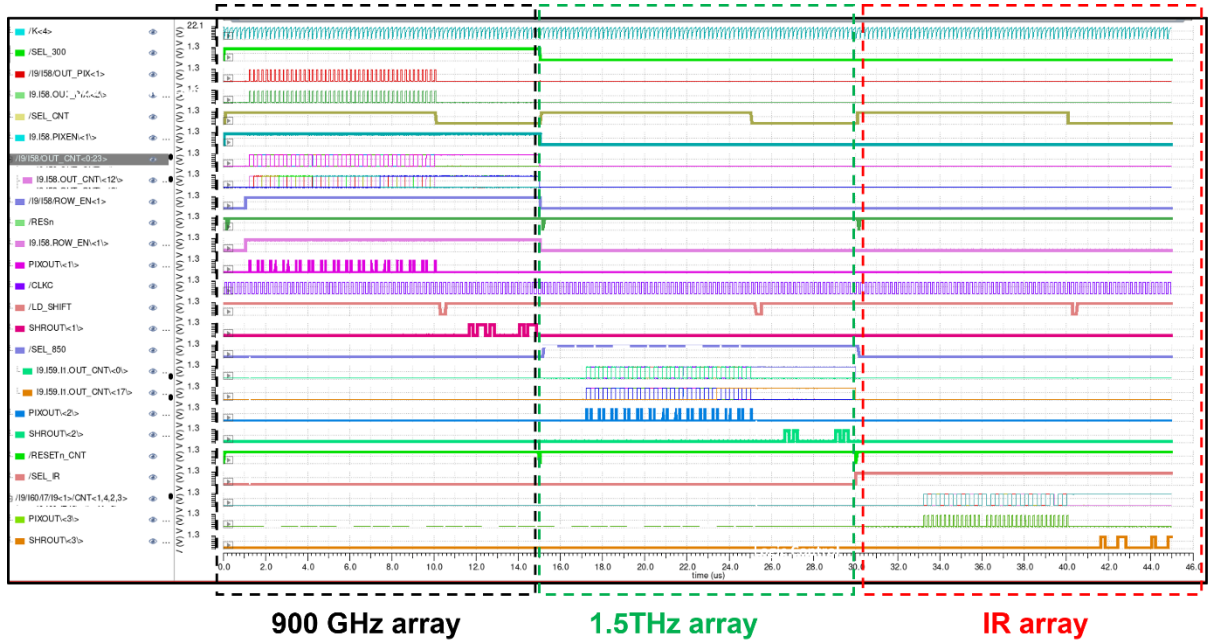


Fig. 4-23. Array Top-Level Integration Simulation.

The 900 GHz and 1.5 THz arrays feature identical control and readout circuitry, while the IR array employs column-level counting with distinct data paths. Multiplexed serial outputs showed successful extraction without crosstalk, enabling sequential or selective imaging across spectral bands. These results confirm the overall SIRTech chip’s functionality.

4.4. Conclusion

This chapter presented the design and implementation of the SIRTech chip, integrating three dedicated imaging arrays (900 GHz, 1.5 THz, and IR) on a single CMOS chip. The architecture makes use of the optimized SEBAT devices described in Chapter 3 to enable detection and digitization of terahertz and infrared radiation signals.

The two THz arrays implement identical 2×2 architectures with in-pixel 12-bit counters for direct power-to-digital conversion. Each pixel integrates the complete signal chain from antenna-coupled FET detection through SEBAT avalanche counting to digital readout, with bow-tie antennas scaled for their respective frequencies. The 28×28 IR array employs a distinct architecture with 9 programmable antennas per pixel and column-level counting, enabling flexible tradeoff between spatial resolution (single-antenna serial acquisition mode) and sensitivity (9-antenna parallel acquisition mode) while maintaining high pixel density.

Post-layout simulations validated timing coordination, event accumulation, and data integrity across all arrays. The chip is scheduled for experimental testing in the near future, with results expected to further validate SEBAT-based avalanche detection as a scalable solution for CMOS-integrated THz and IR focal plane arrays.

Chapter 5

5. Conclusion

5.1. Summary of achievements

This work demonstrates efficient single-electron detection using optimized SEBAT structures in standard CMOS technology. The thesis establishes four main contributions:

- (1) comprehensive TCAD analysis of SEBAT transient behavior, identifying parasitic base resistance and collector capacitance as dominant performance limiters;
- (2) development of a SPICE model to facilitate the design of integrated large-scale antenna-coupled FET detector arrays;
- (3) implementation and experimental validation of CMOS SEBATs in a 110nm CMOS process, achieving 80% electron-to-pulse conversion efficiency and a dynamic range exceeding six orders of magnitude;
- (4) integration of pixel detector arrays with SEBAT-based readout for the THz frequencies of 900 GHz and 1.5 THz, and for the infrared wavelength of 8-14 μm .

Chapter 2 develops predictive device and circuit models for SEBAT operation. The TCAD simulations and SPICE compact model presented in this chapter explain the transient behavior of SEBAT devices and identify base parasitic resistance and collector parasitic capacitance as the dominant performance-limiting factors. TCAD simulations identify the voltage drop across the contact resistance as the primary contributor for the observed inefficiency, while the parasitic capacitance controls avalanche dynamics and recharge timing. The validated SPICE macro-model, tuned using TCAD simulations, accurately reproduces device behavior and provides predictive capability for optimizing SEBAT-based circuits without extensive fabrication iterations. Using this modeling framework, it was established that reducing base parasitic resistance through increased contact area and minimizing collector parasitic capacitance through integrated quenching elements are the key optimization pathways for efficient operation.

Building on these modeling insights, Chapter 3 implements five SEBAT variants in 110 nm CMOS to systematically validate the optimization approach: two devices with ring-contact geometry (gated and gateless), two devices with two-contact configuration (gated and gateless), and a gated

device with externally controllable gate voltage. The parasitic resistance extraction from DC measurements yield values in the 100-200 Ω range for optimized ring-contact devices, compared to 1.4 – 1.5 k Ω range for two-contact implementations. Functional characterization identifies $V_{HV} \approx 20V$ (2.7 V excess bias) as the optimal operational voltage for achieving high-efficiency operation. At this bias voltage, optimized ring-contact devices achieve 74-80% efficiency, measured as the ratio of detected avalanche events to injected electrons. The devices maintain stable operation across count rates exceeding 10^7 cps, spanning more than six orders of magnitude across the operational voltage range. The count rate follows Poisson statistics, enabling signal-to-noise ratio improvement proportional to the square root of total counts. The consistency between experimental results and theoretical predictions reinforces the validity of the modeling approach and provides confidence in predicting SEBAT behavior for different layouts and operating conditions. Comparison between gated and gateless devices (both with optimized ring contacts) yields identical performance, confirming that efficiency is determined by the contact resistance rather than by the presence of the gate. A dark count rate of the order of the 10s cps is measured at $V_{EX} = 2.7V$, establishing the noise floor for electron counting operation.

Chapter 4 uses the optimized SEBATs to develop a new chip called SIRTech, a test vehicle to demonstrate the scalability from single-device to array-level integration of pixels for THz and IR radiation detection. SIRTech addresses the practical requirement for detection systems where radiation in different frequency bands must be sensed. The chip, having a size of $4000 \mu m \times 3000 \mu m$, integrates three detector arrays operating at the frequencies of 900 GHz and 1.5 THz, and 8-14 μm infrared wavelengths. Each array implements optimized SEBAT devices presented in Chapter 3. Post-layout simulations were used to verify the reliable operation of the three arrays, which can operate independently while sharing common clock and control signals for synchronized readout.

5.2. Limitations and Challenges

Several fundamental challenges limit SEBAT-based electron detection in the non-optimized devices presented in Chapter 2. The dark count rate establishes a noise floor that limits the minimum detectable signal level, with thermally generated carriers triggering avalanche events even in the absence of charge injection from the emitter.

The maximum count rate limitation imposed by external quenching circuitry restricts dynamic range at high injection rates in the same device. With 10 M Ω quenching resistance and a collector capacitance of the order of the pF, the RC time constant limits the count rates to approximately 1 MHz. SEBAT integration with low-capacitance quenching elements, as described in Chapter 3,

reduces parasitic capacitance below ~ 100 fF, enabling count rates exceeding 10 MHz while maintaining single-electron sensitivity. This integration requires careful design to limit afterpulsing effects.

Fabrication process variations introduce device-to-device performance differences that affect array uniformity. These variations arise from local doping fluctuations, resulting in contact resistance spread and breakdown voltage non-uniformities within the same fabrication lot.

The measurement setup and the package used to encapsulate the chip pose challenges for SEBAT characterization at very low current levels, where equipment noise and parasitics associated to probes and packaging introduce uncertainties in sub-picoampere measurements. An optically and EM isolated chamber enables DC characterization down to approximately 1 pA injected current (600 kcps electron rate), but efficiency extraction at lower injection levels requires more sensitive instrumentation and high package quality providing ultra-low leakage currents.

5.3. Future Research Directions

The experimental validation and optimization demonstrated in this thesis establish a foundation for advancing SEBAT-based detection toward practical applications. Future work should address the current limitations while exploring pathways for performance enhancement and system-level integration. Three primary directions can be envisaged: experimental validation of the fabricated SIRTech chip, exploration of advanced technologies for next-generation implementations, and extension of SEBAT-based detection to broader applications.

The immediate priorities focus on experimental characterization of the fabricated SIRTech detector chip. Comprehensive testing campaigns will validate array-level performance across 900 GHz, 1.5 THz, and 8-14 μm infrared bands, verifying post-layout simulations for timing, readout architecture, and data integrity. Functional validation with radiation sources and bandpass filters will demonstrate the technology's performance and its applicability in security screening, biomedical diagnostics, and materials characterization.

Advanced CMOS technology nodes (65 nm, 40 nm) offer compact layouts with reduced parasitic capacitances that could further improve maximum count rate performance beyond the current 110 nm implementation. Technology scaling investigations should characterize breakdown voltage uniformity and electron detection efficiency across these nodes. The modeling framework presented in Chapter 2 can provide predictive capability for evaluating process transitions before fabrication.

Detector performance depends on efficient coupling between antenna and detector, requiring co-design of antenna structures with FET detector characteristics. For the THz bands (900 GHz, 1.5

THz), optimizing bow-tie antenna dimensions, substrate effects, and impedance matching maximizes power transfer to the detection circuit. The SIRTech IR array implements nine bow-tie antennas per pixel to increase total collection area: systematic characterization will establish the optimal number and configuration of antennas for each frequency band.

Beyond imaging applications, the SEBAT's ability to convert low-level currents into digital pulse streams opens possibilities for precision current sensing in diverse applications.

These directions build upon the comprehensive optimization framework established in this thesis:

- Experimental validation of fabricated SIRTech chip across 900 GHz and 1.5 THz frequencies, and 8-14 μm infrared band.
- Technology node evaluation (65 nm, 40 nm CMOS) characterizing scaling effects on SEBAT parasitic capacitance, resistance and breakdown voltage.
- Antenna-FET co-design optimization for frequency-specific performance enhancement.
- Large-format array development (64 $\times$ 64 or 128 $\times$ 128 pixels) leveraging the validated integrated readout architecture.
- Extension of SEBAT-based detection to precision current sensing applications beyond imaging (for example Quantum Random number generation).

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