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Control and read-out of the HEPD-02 tracking system onboard CSES-02 satellite

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ABSTRACT: The High Energy Particle Detector (HEPD-02) is a payload of the second China Seismo-Electromagnetic Satellite (CSES-02), designed and built by the Italian Limadou collaboration. Its purpose is to detect cosmic rays and trapped particles of radiation belts, in the kinetic energy range 3–100 MeV for electrons, 30–200 MeV for protons. HEPD-02 is the first space detector to use a tracking detector based on Monolithic Active Pixel Sensors (MAPS). The MAPS provides high

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spatial resolution, low noise, increased robustness, and low production costs. Operating MAPS in space presents a significant challenge due to strict power consumption requirements. To meet such constraints, a custom Tracker Data Acquisition (TDAQ) board and firmware have been designed and implemented, by using a commercial low-power Field Programmable Gate Array (FPGA). This paper addresses the design features of the TDAQ unit, enabling the tracking detector to be operated efficiently, with particular focus on the power consumption performance.

KEYWORDS: Data acquisition circuits; Particle tracking detectors; Front-end electronics for detector readout

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1 Introduction

The China Seismo-Electromagnetic Satellite CSES-02 is part of a scientific multi-spacecraft program devoted to studying the electromagnetic, plasma and particle environment in the Low Earth Orbit (LEO) region, in a collaboration framework led by the China National Space Administration (CNSA) and the Italian Space Agency (ASI).

The most relevant objective of the CSES program is the observation of perturbations, involving the inner Van Allen belt and the Earth’s atmosphere, originated by solar [1–3] or terrestrial phenomena, producing changes in the electromagnetic fields and in the population of trapped charged particles. CSES aims to establish possible statistical correlation between such transients and seismic phenomena [4, 5]. The first satellite, CSES-01, was launched in 2018, whereas the second, CSES-02, has been launched on June 14th 2025.

The High Energy Particle Detector HEPD-02 [6, 7], built by the Italian *Limadou* collaboration, is one of the CSES-02 payloads, specifically designed to study cosmic-ray electrons and protons in the kinetic energy range from 3 to 100 MeV and from 30 to 200 MeV, respectively. HEPD-02 is an upgraded version of the predecessor HEPD-01 [8, 9] onboard CSES-01. It is capable of performing event-based particle identification through a simultaneous measurement of the incoming particle direction and energy.

HEPD-02 is composed of a set of specialized particle detectors, depicted in figure 1, which are installed in a volume of dimensions 37 cm × 53 cm × 39 cm together with the relevant electronics. At the top side, facing the zenith direction during orbital flight, the tracker — or direction detector (DIR) [10–12] — is composed of three layers of Monolithic Active Pixel Sensors (MAPS) described in section 2. Above and below the DIR, the trigger planes TR1 and the TR2 are composed of mutually orthogonal bars of plastic scintillators; by design, the geometrical dimensions of the TR1 five bars match the five underlying DIR detector elements.

This front part is followed by the range calorimeter (RAN) made of 12 square plastic scintillator elements and by the energy calorimeter (EN) made of two layers of LYSO (lutetium-yttrium oxyorthosilicate) crystals. Scintillator panels at the bottom (BOT) and on the sides (LAT_01 to

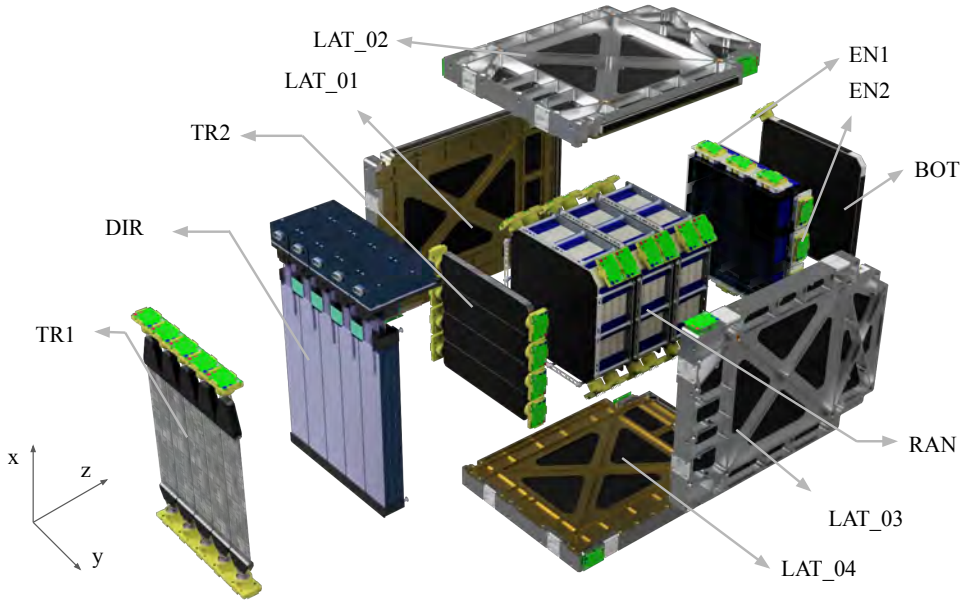


Figure 1. Exploded view of the HEPD-02 detectors: trigger planes (TR1 and TR2), silicon pixel tracker (DIR), range calorimeter (RAN), energy calorimeter (EN1, EN2), bottom (BOT) and lateral (LAT_01..04) containment detectors.

LAT_04) surround the calorimeter with the main purpose of tagging events with particles not fully contained. The TR1, TR2, RAN, EN1, EN2, BOT and LAT units are read-out by photomultiplier tubes (PMTs), for a grand total of 64 PMTs.

The detector control and data acquisition (DAQ) is implemented in three distinct electronic units.

The data processing and control unit (DPCU) [13] is the main HEPD-02 computer, controlling data interfaces with satellite and configuring the entire instrument. In particular, the DPCU collects the scientific data produced by the detectors and arranges them for transmission to the satellite via a dedicated RS-422 link.

The trigger (TRIG) board [14, 15] is dedicated to the read-out of PMT signals and to initiate the general event DAQ when an incoming particle activates specific patterns of hit PMTs.

The tracker data acquisition (TDAQ) board is dedicated to the read-out of DIR. In section 3 and following ones, the design of the TDAQ board and the solutions implemented in its functional architecture are discussed, with particular attention to the strategies for keeping the combined DIR and TDAQ power consumption within the limited budget allowed by the specific satellite application.

2 The silicon pixel tracker

The HEPD-02 direction detector (DIR) is the first silicon pixel tracker ever deployed in space, marking a major advancement in particle spectrometry for space applications. Unlike the microstrip detectors used in previous missions such as AMS-02 [16] and PAMELA [17], HEPD-02 employs Monolithic Active Pixel Sensors (MAPS), which offer key benefits including higher spatial resolution, reduced noise, lower power consumption, a more compact form factor, and cost-effective fabrication. Further details on the design, construction and qualification of the DIR detector can be found in [18].

HEPD-02 DIR uses the ALTAI MAPS sensor, selected for its excellent noise and resolution performance, low power requirements, and ultra-thin substrate, which minimizes multiple scattering. The choice also builds on the extensive experience and documentation from the ALICE experiment at CERN [19], which uses the closely related ALPIDE sensor. One of the most relevant differences is the case use, several simultaneous tracks at trigger rate of ~ 40 MHz for ALICE and typically single or few tracks at few kHz for HEPD-02.

The ALTAI sensor is fabricated by Tower Semiconductor LTD with a 180 nm CMOS process over a silicon substrate of $50\text{ }\mu\text{m}$ only. It features an array of 512×1024 pixels over an area of $15 \times 30\text{ mm}^2$, with $\sim 28\text{ }\mu\text{m}$ pitch in both directions, thus providing a very high spatial resolution. Each pixel cell contains a sensing diode read-out by an analog circuit (amplifier, shaper and threshold discriminator) that generates a binary hit information. This is then stored and processed in the digital part of the device.

The DIR is composed of five identical modules called *turrets*, arranged side by side, covering an area of $150 \times 150\text{ mm}^2$. Each turret (see figure 2) is an independent direction detector, made of a stack of three MAPS layers, vertically spaced by 8.5 mm. A small lateral tracker splitter (TSP) board, equipped with Glenair Micro-D connectors, constitutes the interface with the HEPD-02 power supply unit, delivering circuit power and silicon bias, and with the TDAQ board for digital lines.

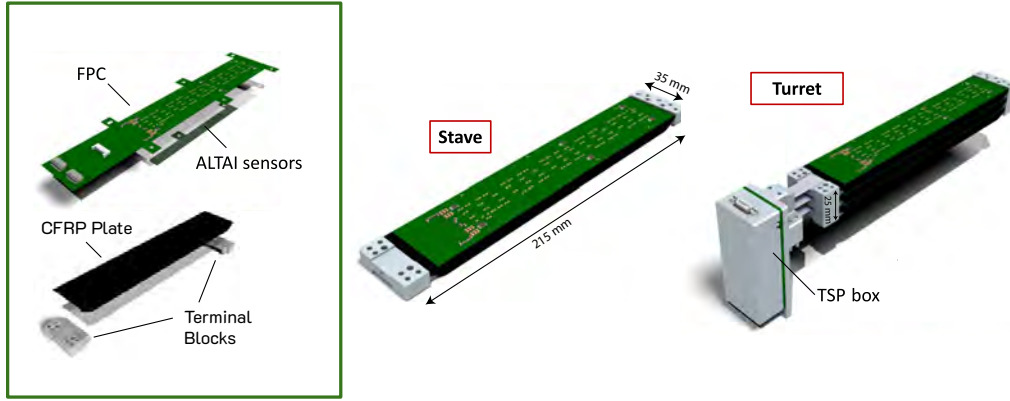


Figure 2. Visualization of DIR turret assembly. In a turret, 3 staves are vertically stacked and connected to the lateral TSP board. Each stave contains 2 columns of 5 ALTAI chips.

The turret stack element, called *stave*, is the fundamental mechanical and electrical unit of the DIR. The stave is formed by a custom-designed U-shaped carbon-fiber reinforced polymer (CFRP) plate [12] supporting 10 ALTAI chips, organized in two columns of 5 chips each, for a total area $30 \times 150\text{ mm}^2$. The CFRP plate provides structural strength, capable of withstanding the stresses expected during launch and orbital maneuvers; it also offers good thermal conductivity for transportation of the heat generated by the MAPS towards the aluminum terminal blocks, which constitute the mechanical and thermal interface of the stave with HEPD-02 structure.

A flexible printed circuit (FPC) is glued on top of the ALTAI chips, providing the routing of power, bias and data lines. Ultrasonic wire bonding is used to obtain the electrical connections between the FPC and the underlying ALTAI bonding pads, that are accessible through corresponding FPC holes. For redundancy, each connection is performed with three bonding wires.

For each column, one ALTAI chip is configured as master and the other 4 chips as slaves. Each slave is connected with the master by means of a multi-drop LVDS (MLVDS) input clock, a CMOS

bidirectional control data line and 4 CMOS read-out lines operating in double data rate mode, thus providing 8 bit per clock cycle. The master is in turn connected with the TDAQ via 2 MLVDS lines (input clock and bidirectional serial data); the two master ALTAI on a stave share the same physical connections with TDAQ, which means that the serial data line is actually a shared bus.

3 The Tracker Data Acquisition (TDAQ) board

The TDAQ board has been implemented with a custom design of both hardware and firmware, with a parallel architecture for a fast enough read-out speed, while keeping the board power consumption within the required limits. The preliminary design of TDAQ was presented in a short conference report [20], while in this paper we discuss the motivations for a custom design and the details of its implementation.

The primary task of the TDAQ board is to operate the DIR detector by acquiring pixel data, delivering them to the DPCU and managing the ALTAI configuration and calibration tasks. The TDAQ board is also responsible for controlling the on/off state of power and bias for each of the 15 DIR staves, by operating solid-state switches located on the TSPs.

The TDAQ board circuitry is composed of three parts: the Common Connections Section (CCS), the Hot Digital Section (HDS) and the Cold Digital Section (CDS), as depicted in figure 3. The HDS and the CDS are identical, according to a hot/cold redundancy scheme, like for most of the HEPD-02 electronics: the HDS is normally operating, while the CDS is normally kept powered-off. In case of unrecoverable failure of HDS, the DPCU will switch HEPD-02 to safe mode and wait for a command issued from ground to change the payload configuration, enabling the CDS instead of the HDS.

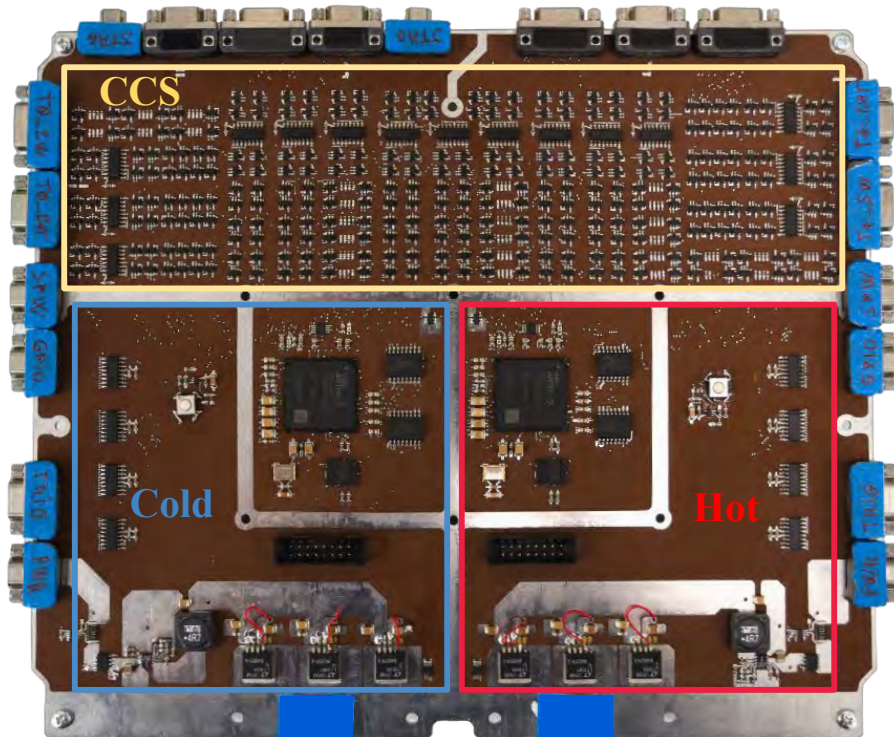


Figure 3. Visualization of the TDAQ board. In the illustration, the hot/cold redundancy is emphasized by the red/blue contours.

The CCS hosts the interface with DIR, with two connections (data and service) for each turret, implemented with Glenair Micro-D GMR7590 connectors (figure 4). The data connection carries six MLVDS lines, implemented with Texas Instruments SN65LVDM051 high-speed transceivers. Each stave of the turret uses two lines: one for the clock output and one for bidirectional serial data. The service connector hosts single digital signals to manage the stave: analog-part power enable, digital-part power enable, power good status, silicon bias on/off, and a 1-wire line for temperature sensor chain read-out. For each line, a specially designed circuit, built with two complementary switches (Analog Device ADG701), automatically handles the correct connection to either HDS or CDS, according to which one is currently powered.

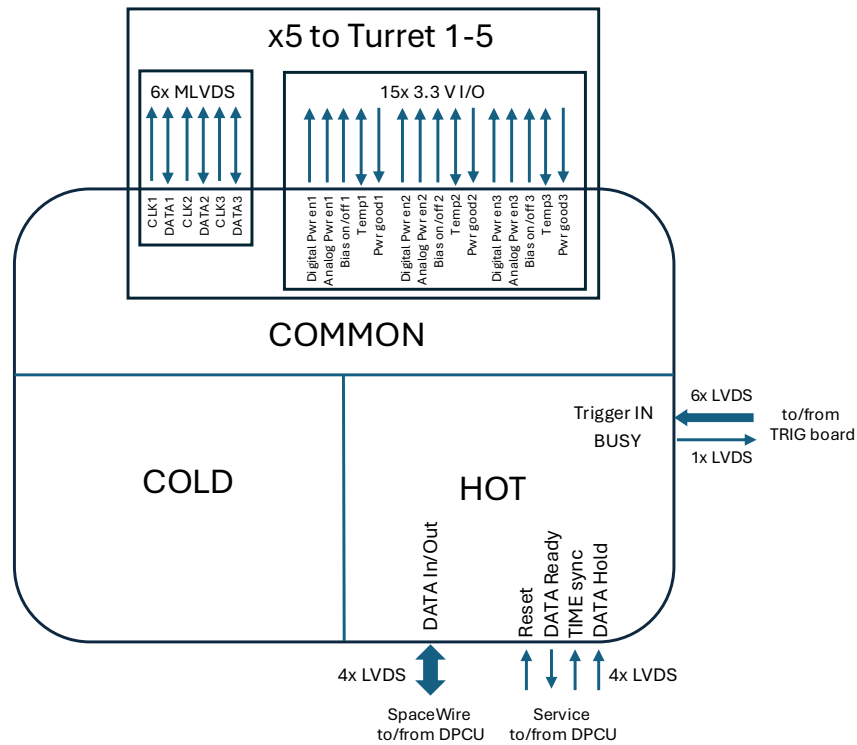


Figure 4. Schematic of the TDAQ connections with the DIR detector, the DPCU, and the TRIG boards. The cold section hosts the same set of connections (not drawn) as the hot one.

The HDS/CDS contains the board control logics, the communication interfaces with DPCU and TRIG boards (both hot/cold redundant) and the internal power distribution network. The control logics is implemented on a FPGA from the Xilinx Artix 7 series, characterized by low power consumption (L1 type, 0.95 V core voltage) and wide operating range for junction temperature (-40°C to $+100^{\circ}\text{C}$). Two 16 MB flash memories, Cypress S25FL256S, are present: the first stores the FPGA configuration code, and the second acts as a mass storage for the soft MicroBlaze processor instantiated within the FPGA (described in section 4). An auxiliary 4 MB SRAM (Cypress CY7C1071DV33) is also present. The connections with the DPCU and TRIG boards (figure 4) are implemented using standard LVDS channels, driven by Texas Instruments transceivers of the SN65LVDS3x family, for discrete control signals and data link, which are described in section 4.

The selected components comply with the automotive or industrial qualification and were successfully used for several years during previous low-Earth space missions, such as HEPD-01. In particular, the Xilinx Artix 7 FPGA features adequately small cross sections for SEU (Single Event Upset) on configuration memory and programmable logic bits [21] as well as stable operation with no functional errors in all critical parts irradiated with doses up to 2 Mrad [22]. Given the irradiation conditions for the CSES-02 mission, even taking into account enhancements driven by solar activity, the expected SEU rate for the whole TDAQ amounts to less than 1 event in 10 years.

4 The TDAQ firmware

The TDAQ firmware is implemented in the Xilinx Artix 7 FPGA and includes a finite state machine (FSM) section, for data acquisition and external interfaces with DPCU and TRIG boards, and a soft microcontroller unit (MCU) for executing the more complex calibration tasks of ALTAI chips. The structure of the TDAQ firmware is shown in figure 5.

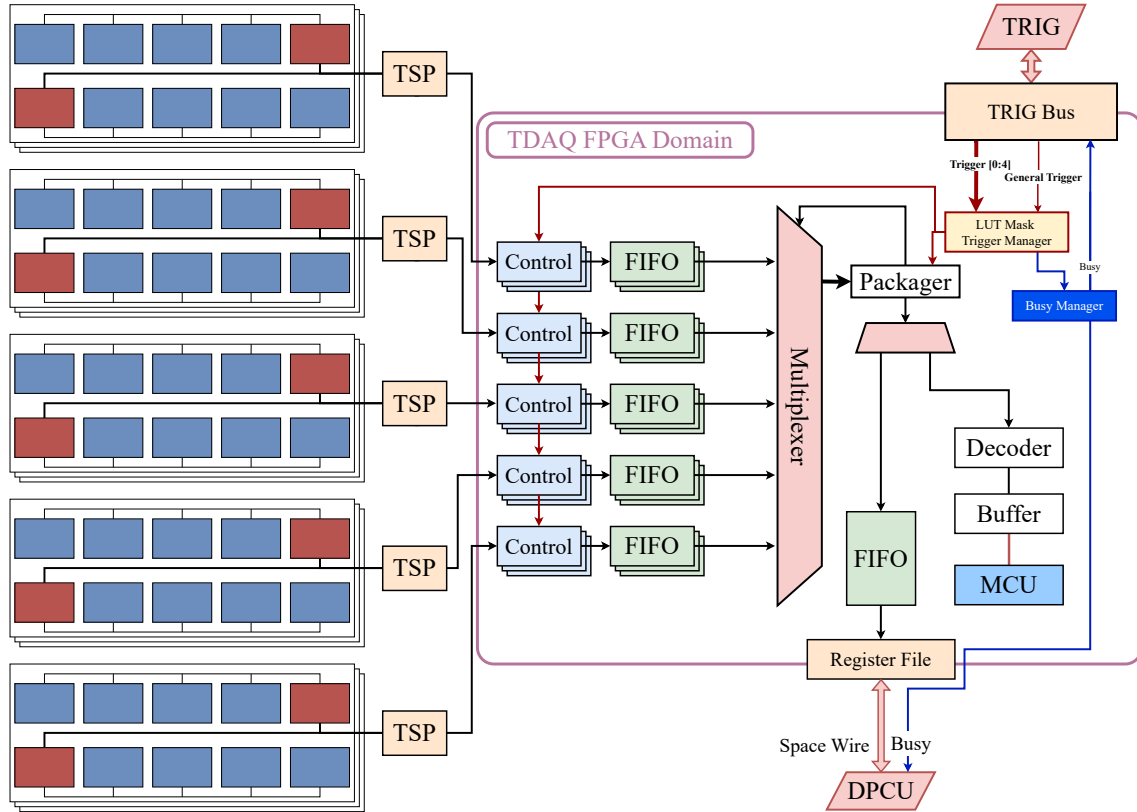


Figure 5. Schematic view of the DIR with the connections to the TDAQ board, ALTAI Master (red squares) chips, ALTAI slaves (blue squares). The internal architecture of the TDAQ firmware is depicted on the right.

The FSM section has been fully developed in VHDL (Standard IEEE 1076-2019) and profits of the reliability of circuits implemented on the FPGA fabric. The design is based on modularity and parallelization. During the development, the design modularity allowed to readily adapt to changes in the detector requirements and ensured high reusability across different devices within the same family. Parallelization, a notable strength of FPGA-based firmware, has been leveraged to

address the relatively slow communication speed with the ALTAI sensors, as discussed later. The synthesis, implementation, testing, and installation of the firmware were all carried out using the Vivado suite provided by Xilinx.

The TDAQ is designed to operate either in DAQ or idle mode, according to the general operation of HEPD-02, which dedicates most of its time to the acquisition of particle events, with interspersed phases for instrument calibration or self-testing.

In DAQ mode, the TDAQ responds to trigger signals from the TRIG board, i.e. the general trigger and 5 additional signals indicating the single activated TR1 bars; it sends back a busy signal, inhibiting further triggering until the DIR data (i.e. the information on hit pixels) have been fully collected and processed.

Stave data are read-out in parallel: for each of the 15 staves, the corresponding Control module sends a read-out command to the master ALTAI chips; after a suitably tuned time delay, it collects the data and puts them in an internal FIFO buffer. The time interval between trigger pulse and data collection is thus fixed (with a negligible synchronization jitter) and chosen in such a way to match the time window for which the ALTAI threshold discriminator binary output is kept to 1 after each hit.

The Packager module acts as event builder, asynchronously pulling data from the 15 Control modules and rearranging them into a DIR event packet, optimized for space saving and with a Cyclic Redundancy Check (CRC) word for data consistency check. The DIR event packet includes an event number and time stamp of trigger reception, to ensure unique correlation with the corresponding TRIG event packet. The DIR event packets are stored in a FIFO output buffer for subsequent asynchronous read-out by DPCU, while the busy signal is negated, except in case the buffer is full because of the accumulation of event packets to be read. The DIR event packets have variable size, of the order of few hundreds bytes, depending on the pattern of hit pixels. The time needed after trigger reception, for data read-out, processing and storage on FIFO output, increases with the number of hit pixels; for typical events with single or few tracks it amounts to few hundreds μ s, fully compatible with the trigger rates of few kHz maximum which can be managed by HEPD-02.

In DAQ mode the TDAQ responds only a reduced set of commands from DPCU, such as reading event packets or the essential diagnostic information to assess the correct DIR operation.

In idle mode, the TDAQ serves all commands from DPCU, including read/write operations on any register, configuration operations and requests for different kinds of ALTAI calibrations or self-test operations; these last more complex commands are executed autonomously by the MCU, which operates on the data diverted from the Packager to a Decoder module and then to a MCU accessible RAM buffer.

The interface with DPCU is established by exposing a shared memory segment, called register file, that can be read or written by the DPCU. In particular, the register file contains a command register, where the DPCU can write a code corresponding to the action to be executed by the TDAQ; the command output is then available in a dedicated section of the memory segment. Two other register file notable sections contain the first available event packet and the status/health data of DIR and TDAQ.

DPCU and TDAQ communicate using the SpaceWire Lite protocol (IEEE 1355-1995) [23], implemented over a full-duplex SpaceWire standard digital connection driven at 20 Mbps, where DPCU acts as master and TDAQ as slave. Additional single digital lines are used as TDAQ service inputs (board reset, time counter synchronization, event packaging hold) and output (event packet ready).

The MCU has been implemented using a Microblaze soft micro-controller. Its purpose is to execute tasks involving data processing to determine the optimal configuration parameters for each of the 150 ALTAI chips and to execute calibrations. The ability to write standard code for these tasks and use flash memory for mass storage broadens the scope of operations that can be conducted in-flight, offering enhanced flexibility to adapt to unforeseen post-launch conditions. With respect to a multi-core ARM processor, this solution has the advantage of configuring the features according to the needed set of tasks; furthermore, when not in use, the soft microcontroller can be disabled, minimizing the power consumption.

The MCU is complemented by other Xilinx IPs, including two AXI Timers, the AXI External Memory Controller, and the AXI Quad SPI for interface with the flash memories. To enhance system reliability, an AXI Timebase Watchdog Timer was integrated into the design together with the MCU. Its purpose is to prevent the software running on the MCU from freezing: if the MCU does not regularly reset the watchdog timer, a signal is generated that triggers a soft reset of the MCU.

The TDAQ firmware adopts mitigation techniques for single-event upsets (SEU) which may be induced by radiation in the LEO environment. For the FPGA internal SRAM configuration memory, we implemented the Soft Error Mitigation Controller (SEM) IP core by Xilinx [24, 25]. The SEM continuously reads the configuration memory and performs integrity checks. It can thus detect errors and automatically rewrite the affected configuration data.

Even after the configuration memory is restored, the FSM may be stuck in an invalid state, thus preventing proper device functioning. To handle such situations, the TDAQ FSM can set specific error flags in the status/health data regularly monitored by the DPCU: in such cases, the DPCU may apply a reset of the logic or eventually reconfigure the FPGA.

Additional mitigation techniques for SEU consequences are adopted for FSM state registers, which are configured with Hamming(7,4) encoding, i.e. with automatic correction of single bit upset. The MCU core memory and the FIFO/RAM buffers use a similar Error Correcting Code to automatically fix single bit upsets.

5 Strategies for an efficient power management

The ALTAI chip is the non dual-use version of the ALPIDE chip, originally developed for the HL-LHC upgrade of the ALICE experiment, operated at CERN LHC collider. These devices are designed for fast data delivery but not optimized for power consumption. In fact, when used at CERN, the chips are cooled with a water circuit so as to draw as much power as needed. On the other hand, using them in space missions requires careful considerations about power consumption.

To deploy the ALTAI chips in HEPD-02, we developed a novel approach with respect to the ALICE experiment, aiming at reducing the power absorbed by the digital part while leaving the analog part unchanged, thus maintaining the excellent detection performances of ALTAI sensors and, at the same time, obtaining a combined power consumption of DIR and TDAQ compliant with the stringent 13 W budget allowed by the specific application in the CSES-02 satellite.

As a main design guideline, we exploited the fact that in a satellite experiment such as HEPD-02, the trigger rates and amount of information to be read-out (i.e. hit pixels) are orders of magnitude smaller than in the ALICE experiment. In particular, HEPD-02 is configured to manage trigger frequencies up to few kHz at peak, with few hundreds of bytes of information produced by the

whole tracker. This allowed to slow down the DIR read-out while still maintaining it compatible with the instrument operation.

We chose to operate ALTAI in the master/slave mode: each stave hosts 10 chips organized in two groups, each with a master and four slaves. The master is the sole interface with TDAQ board and the data transmission is serialized through it, with significant power saving and reduction of the physical connections towards TDAQ. This is important given the strict geometrical constraints for wire routing in the compact HEPD-02 geometry. Measurements of power consumption indicate that the use of master/slave mode allows to reduce the overall DIR power consumption by $\sim 30\%$ with respect to a solution employing stand-alone ALTAI chips, i.e. from 22 W to 15 W (1 W per stave).

The ALTAI device is designed for a serial read-out of master chips by means of the built-in fast (1200 Mbps/400 Mbps) Serial Data Transmission Module (SDTM), accounting for a power consumption of ~ 90 mW. We found that it is possible to implement an alternative read-out using the much slower Control Logic Bus (CLB), a half-duplex serial line with a bandwidth of 40 Mbps. At the same time, the ALTAI modular design allows to keep the SDTM logics permanently powered off. The CLB is normally used to configure the chip and deliver the trigger, but it also gives access to the ALTAI output buffers and can be used as an alternative data read-out path. Since, in its original purpose, the CLB was not intended for sustained data reading, we had to design from scratch a new implementation of the ALTAI communication protocol over the CLB in the TDAQ FSM section. The time needed to transmit the event data to TDAQ is typically of a few hundreds μ s, fully compatible with trigger rates. With this solution, the overall DIR power consumption is expected to be further reduced by $\sim 20\%$, i.e. from 15 W to 12 W (0.8 W per stave).

As an additional measure to comply with the power limit, we introduced a time gating of the digital clock signal. In DAQ mode, the clock is normally kept off and turned on when the TDAQ receives a trigger signal; it is then kept running while the TDAQ sends a read-out command and the event data are read by the TDAQ, then it is turned off again. With clock gating, the absorbed power is high only for a very limited time after each trigger; on the other hand, when the clock is off the ALTAI digital part is not active and the overall DIR power consumption is expected to be reduced to ~ 6 W (0.4 W per stave). This measure is feasible because the ALTAI analog part remains always active: when a pixel collects charge, a signal with a shaping time of few μ s is immediately formed, and a corresponding pixel-hit line is asserted for all the time this signal is above a given threshold. An incoming read-out command initiates the check of all pixel-hit lines, with the addresses of hit pixels added to the output data stream. On the other hand, the time passing from the particle crossing to the transmission of read-out command from TDAQ to a stave is of few hundreds ns, still compatible with the shaping time.

For what said above, with clock gating the power consumption increases with the trigger frequency and duration of the clock gate itself. Laboratory measurements were performed (section 6) to accurately assess the trigger rate dependence of the absorbed power. The combined DIR and TDAQ power turned out to be well within the allowed 13 W budget.

If necessary, further power reduction can be achieved by working on the spatial domain. As already reported, each DIR turret is matched with a scintillation bar of the first trigger plane TR1, with the TRIG board generating 5 specialized trigger signals corresponding to the pattern of hit TR1 bars. The TDAQ firmware was configured in such a way that it is possible to enable a reduced-power operation, with read-out of just one turret or up to 3 turrets, centered on the hit TR1 bar, which is feasible for the majority of events, with only one TR1 hit.

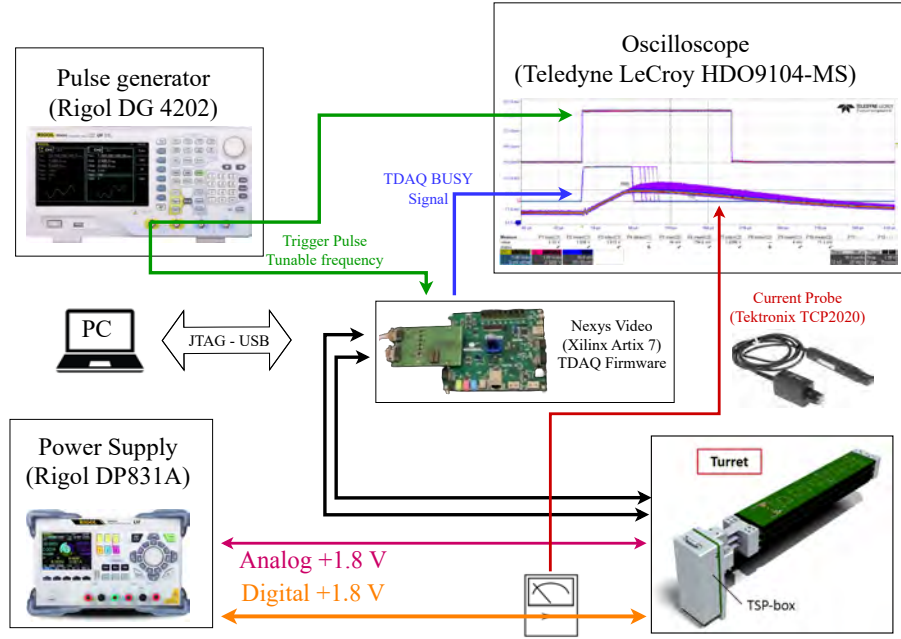


Figure 6. Schematic representation of the experimental setup recreated in the TIFPA laboratory for the characterization of the DIR power consumption. The TDAQ firmware is instantiated on the Xilinx Artix 7 FPGA mounted on the Digilent’s Nexys Video evaluation board. The connections between the FPGA board and the DIR turret (via the TSP) are made through a custom expansion board. To study the power consumption versus the trigger frequency, the DAQ chain was triggered by a pulse generator. The average power consumption was measured by the power supply unit (see text for details).

6 Measured power consumption performances

We implemented an experimental setup (see figure 6) to accurately measure the power needed to operate the DIR and thus confirm the effectiveness of the design features introduced to maintain the power consumption within the allowed budget.

A DIR turret was connected to a bench power supply unit (Rigol DP831A) providing the 1.8 V analog and digital power supply lines and measuring the current delivered on each output. Additionally, a current probe (Tektronix TCP2020) was applied across the digital power supply line for prompt measurement of current variations as a consequence of read-out activity. The absorbed power was directly determined by measuring the current values on the analog and digital supply lines, together with the supply voltage.

The turret was controlled by an engineering model TDAQ, implemented on a Digilent Nexys Video evaluation board, completed with a custom expansion board with all the necessary connectors and interfaces. The TDAQ, in turn, was operated from a laptop PC delivering commands to set up the turret, initialize the ALTAI chips, control the DAQ and perform calibrations.

Trigger pulses were provided to TDAQ by a waveform generator (Rigol DG4202) operated in pulse mode, which allowed to vary the trigger frequency during the test. The duration of the clock gate was monitored indirectly by checking the TDAQ output busy signal, which stays asserted for approximately the same time. The trigger and busy signals were monitored with an oscilloscope (LeCroy HDO 9104-MS), together with the current probe output.

To simulate the passage of a charged particle through the turret, one ALTAI chip per stave was programmed to generate a pattern of nearby hit pixels (known as a *cluster*), by using the internal configurable test-in functionality. The number of pixels composing the cluster (known as cluster size) determines the amount of transferred data and, therefore, the duration of the clock gate and busy signal.

With this experimental setup, we measured the average power consumption of a single turret as a function of trigger frequency up to 1 kHz, for varying cluster sizes. The power measurement was performed through the calibrated voltage and current meters integrated in the power supply unit; with this method, once applied a fixed and continuous trigger rate, the resulting current represents the average value over the periodic bursts of activity initiated by the triggers. These data were employed to determine the DIR power consumption with DAQ activity on 1, 3 or all 5 turrets, as presented in figure 7, by simple multiplication of single turret consumption; the approach was possible since the expected impact of fabrication tolerances on power consumption of involved parts is order of % (as also verified by measurements) and hence negligible within the scope of the present evaluation.

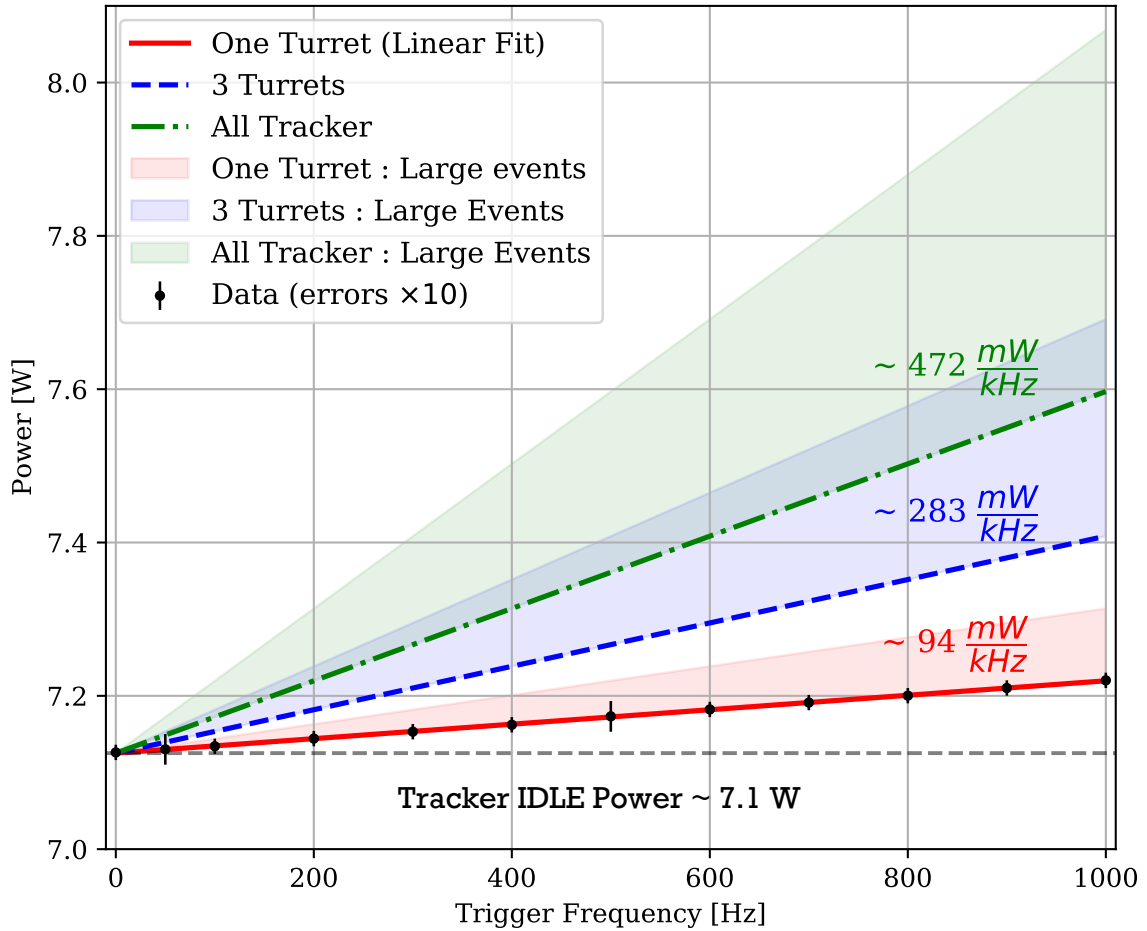


Figure 7. Power consumption of 1, 3 or 5 simultaneously read-out DIR turrets, as a function of trigger frequency. The black points represent the experimental data for DAQ operation of a single turret for small events (cluster size set to 2), superimposed on the baseline DIR power with no triggers. The quoted errors correspond to the standard deviation of repeated measurements.

The baseline DIR power consumption in idle mode, i.e. with no triggers at all and therefore no clock gates, was determined to be 7.1 W, higher than the 6 W value estimated during design (as reported in section 5), but still acceptable; the difference comes from the approximations of the employed circuital model of ALTAI device, before performing the actual measurement.

An additional contribution, linearly increasing with trigger frequency, arises from DAQ activity. As a first step we set the ALTAI cluster size to 2 pixels; this size is typical for the passage of a minimum ionizing particle, such as an electron in the energy range from 3 to 100 MeV. The experimental results for DAQ activity on a single turret are shown in figure 7 by the black points and the superimposed linear fit. The duration of the busy signal is 70 μ s for most of these events, with some fluctuations up to 100 μ s for a few of them, due to communication latencies related to the firmware version operating in the engineering model TDAQ, as shown in the upper-right panel of figure 6. The measured increase of power consumption with trigger frequency turns out to be (94 ± 1) mW/kHz for one read-out turret; this value was extrapolated to the case of 3 and 5 simultaneously read-out turrets, respectively giving (283 ± 3) mW/kHz and (472 ± 5) mW/kHz.

Subsequently, we set the ALTAI chips to create larger pixel clusters, typically produced by highly ionizing particles such as nuclei, which would generate longer busy signal durations, up to the maximum allowed (200 μ s), saturating the memory space allocated for event data on TDAQ. The regions covered by such events are identified with the shaded filled areas in figure 7, whose upper limits approximately correspond to twice the slope obtained for minimal cluster sizes.

The maximum DIR power consumption, with all 5 turrets simultaneously read-out, turns out to be less than 8.1 W at 1 kHz trigger frequency. On the other hand, the measured TDAQ power turns out to be 2.6 W at full operation. The combined power thus amounts to 10.7 W, well below the allocated 13 W power budget. This allows to sustain even higher trigger rates (since HEPD-02 can manage peak rates of few kHz) and to take into account in-flight aging of the HEPD-02 power supply unit, which in turn causes loss of efficiency and higher power consumption. In the extreme case of power consumption exceeding the budget, it will be possible to modify the HEPD-02 instrument configuration by suitable telecommands from ground, for example to reduce trigger rates by applying higher pre-scaling factors.

7 Conclusion

The HEPD-02 direction detector is the first space-borne silicon pixel tracker employing the ALTAI Monolithic Active Pixel Sensor (MAPS).

A custom data acquisition (TDAQ) board and firmware have been implemented to exploit the excellent detection performances of the MAPS, while keeping the power consumption within the strict limits imposed by the satellite mission. This original design includes a read-out protocol implemented with the ALTAI slow-control bus, coupled with extensive use of clock gating.

The direction detector and TDAQ board have been successfully integrated in the HEPD-02 flight and qualification models, which underwent extensive tests with particle beams and cosmic rays at ground level.

Our application shows the feasibility of using MAPS in space with a limited power consumption. This, in turn, opens to the design of large tracking detectors using MAPS, at a scale not previously attainable with strips detectors in terms of costs, complexity and 2-D point resolution [26]. The next generation of MAPS [27, 28] is currently being designed considering the possibility of space application and consequently implementing built-in power saving solutions.

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