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38050 Povo – Trento (Italy), Via Sommarive 14
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Leandro Lorenzelli[*], Kamal J Rangra[1] ,Cristian Collini, Flavio Giacomozzi, Benno Margesin*
Fernando Pianegiani[1]
ITC-irst Microsystems Division, Via Sommarive,18 38050 Povo-Trento - Italy
[1]Department of Information Technology, University of Trento,
Via Sommarive,14 38050, Povo-Trento - Italy

ABSTRACT

The feasibility of integrating the RF MEMS switches in space and wireless communication systems has generated tremendous interest in related design, fabrication and characterization methodologies. The space applications make long term reliability of the devices a very pertinent issue and involves both the process and device characterization. In this paper we describe the experimental setup and measurement results on RF MEMS switches fabricated for DC to 30GHz applications. The on-wafer experimental setup, based on standard manual microprobe station provides dual pulse actuation voltage waveforms with programmable period and amplitude, ranging from 10^{-5} to 1sec and 0-200 volts respectively. The usefulness of the dual-pulse testing is demonstrated by the minimal charge generation in the dielectric layer and capacitance measurements with negligible variations over long measurement periods.

1. INTRODUCTION

RF-MEMS devices and applications thereof are relatively new, among the prevalent MEMS technologies. The superior performance, volume, weight and cost reduction and the world wide market for communication systems with ever increasing emphasis on mentioned attributes make it a technology being followed by large number of research groups in industry and universities. RF-MEMS switch, most promising of the RF devices, is being explored as "near ideal" switching device in a number of existing communication systems and subsystems with frequency range up to 80GHz [1,2]. The electrostatically actuated metal beam based switches out perform the other solid state switches such as FETs, HEMTs and PIN diodes [3], currently being in use. Although , RF MEMS switches have the speed limitation as compared to the semiconductor counterparts, they exhibit very low insertion loss due the low resitivity of the metal and high isolation due to 1-3 microns of physical separation between switching elements. The inevitable I-V non-linearities associated with semiconductor junctions in PIN and FET devices are also non-existent in such devices, except for the minor hysterises in C-V in shunt switches. This improves the distortion characteristics and power handling capabilities in the devices which becomes important consideration in systems having large number of switches and limited power resources. The RF MEMS switches exhibit no measurable harmonics or intermodulations and require negligible quiescent current consumption; typical switching energy is less than 10nJ [4]. The monolithic batch fabrication of switches when used as components in an integrated RF system, improves the overall performance and makes it more cost effective as compared to the design approach with solid state switches.

The electro-mechanical response of the RF MEMS switch can be approximated by a lumped one dimensional model [5]. The model considers the capacitive switch as a single rigid parallel plate capacitor, with top plate suspended over the fixed bottom plate by an ideal linear spring. The capacitor has effective area $\boldsymbol{A}$ and is separated by distance $\boldsymbol{g_o}$. The upper plate, with material spring constant $\boldsymbol{k}$ also referred to as membrane is movable under electrostatic actuation when a suitable bias is applied between the plates, bringing the gap to a minimum depending upon the dielectric layer thickness on the bottom plate. The same configuration can be used as a series switch with minor modification on the signal carrying conductor. The membrane consists of a thin metal layer (Au, Al or Cu, 2-3 μm thick) suspended across dielectric or polymer posts. The bottom plate is a 1.5 - 2 μm

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[*] *Corresponding author, e-mail address: lorenzel@itc.it*

thick metal layer with a 200-300 nm of dielectric layer on it. In the 'OFF' state, large air gap between the top and bottom metal plates constitutes a high impedance. The thin metal membrane deflects towards the bottom electrode under the effect of a bias voltage and is capacitibly coupled to the bottom electrode when the applied bias exceeds the pull-in voltage ***Vpi***, thus lowering the switch impedance. The 'ON' to 'OFF' capacitance ratio determines the isolation and insertion loss of the device. The pull-in bias for this simple lumped model is given by [5],

$$\mathbf{Vpi} = \sqrt{\frac{8kg_0^{\ 3}}{27e_0A}}$$

where e_o is the dielectric constant of the dielectric material. The spring constant for a switch depends on the geometrical dimensions of the beam, Young's modulus and Poisson's ratio. The process related residual stress (of the beam) dependence of ***Vpi*** coupled with environmental effects such humidity in the measurement setup and charge injection into the dielectric insulation layer, lead to drifts in ***Vpi*** over time and shorter life span of the devices. In view of the long term reliability issues for applications such as space communication variations in ***Vpi***, switching speed and the life time are of crucial importance. In the following sections we discuss the variation in actuation voltage, bridge capacitance, signal rise and fall time for the fabricated RF MEMS test structures using an experimental setup developed around a standard micro probe station.

2. FABRICATION

A series of test structures implemented for the technology characterization have been fabricated using a SPST/SPDT RF-MEMS switch fabrication process on 5kΩcm, <100> p-type Si wafers. To minimize the dielectric losses devices and test structures are implemented in CPW configuration with standard 50Ω line impedance. The fabrication steps for a representative RF MEMS switch are outlined in Figure 1. In order to integrate the 50kΩ resistors and DC blocking capacitors, devices are fabricated using a seven mask fabrication process. As shown in Fig.1a the biasing resistors are patterned in 300nm LPCVD polysilicon layer deposited on 1000 nm thick thermal oxide. The contact holes are patterned in 200 nm TEOS SiO_2 layer, deposited on boron implanted poly silicon with a dopant activation cycle at 925° C for 60 minutes. This is followed by sputter deposition of 60 nm of Ti layer and 200 nm of TiN, by reactive sputter deposition technique to define underpass lines and diffusion barriers on the polysilicon contacts (Fig.1b). The underpass and actuation pad areas are also fabricated in polysilicon in a separate process run with thicker oxide insulation layer to achieve better isolation. Via holes are defined in low temperature SiO_2 or PECVD Si_3N_4 in step (Fig.1c). Si_3N_4 covered actuation pads are used for analyzing the drift in Vpi due to charge injection compared to SiO_2 insulation.

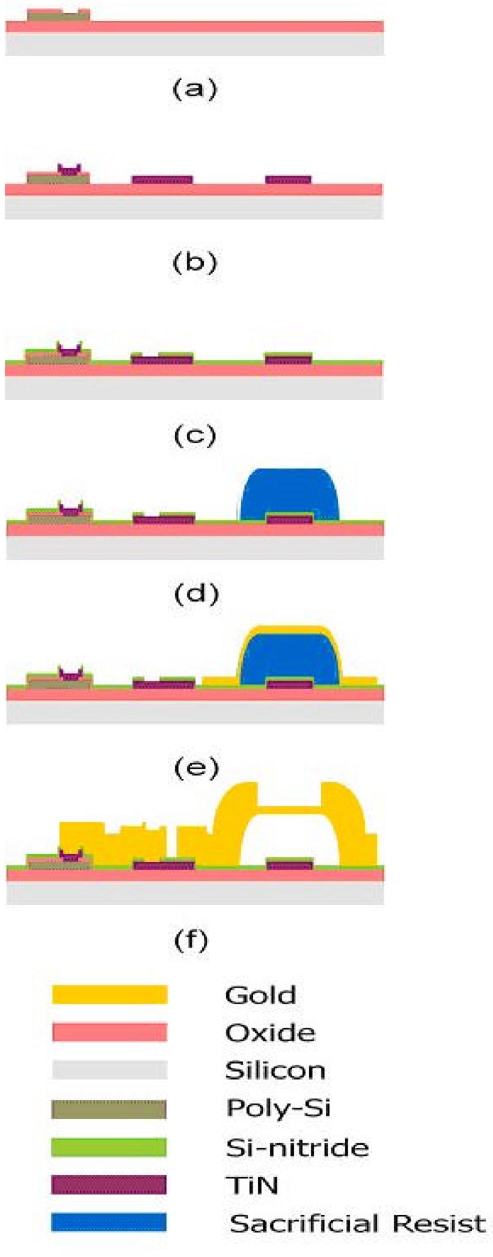
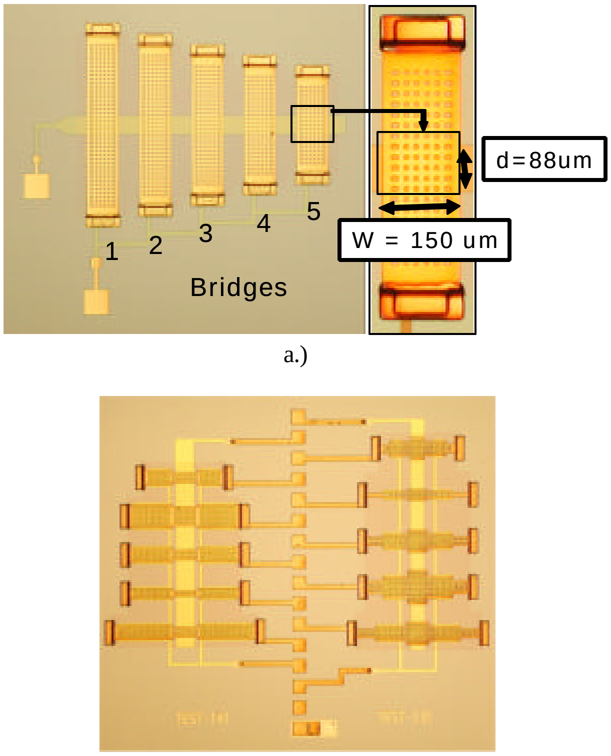


Figure 1. Schematic outline of the fabrication process for RF-MEMS switch.

To pattern the movable membrane a 3 micron thick photo resist layer, hard backed at 200^{o} C to ensure good step coverage, is used as sacrificial layer (Fig.1d). As a seed layer for electrochemical deposition of Au , a 20/100/10 nm thick Cr/Au/Cr layer is deposited by PVD followed by a 3 μm thick photoresist layer to define the interconnects and the movable membrane in step (e). After a wet Cr etch, 1.5 micron Au layer is selectively grown in gold sulfite bath. The selected electroplating parameters result in required tensile stress. The next photolithography (Fig.1e) defines the CPW lines and anchor posts for the microbridge. It is further followed by the selective deposition of 4 μm thick gold layer. After the removal of last masking and seed layers, the membrane is released using a modified plasma ashing process to avoid stiction problems.

3. TEST STRUCTURES DESIGN

The mechanical properties of the fabricated switches are characterized using composite electromechanical test structures specially designed and fabricated for easy access and shorter measurement cycles.



a.)

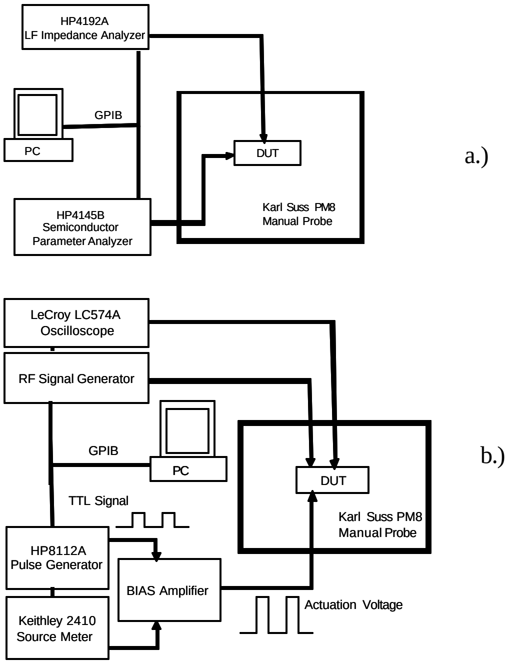
b.)

Figure 2. a.) Photograph of a test structure with contemporaneously actuated bridge; b.) Photograph of an other test structure with separately bridge contact.

In order to study the geometrical contributes in the elctromechanical actuation, test structures having bridge with different length and width have been described. Each structure consists of five microbridges with length (850 to 450 μm), width (150μm), thickness (1μm) and gap (3μm) corresponding to the SPST and SPDT devices under consideration. Different configuration of microbridges have been implemented to be actuated individually or contemporaneously. Figure 2 shows the photograph of a basic test structures utilized for the electromechanical tests.

4. EXPERIMENTAL RESULTS

The experimental setups used for studying the mechanical properties and experimental verification of the parameter such as actuation voltage, capacitance and ON – OFF timings are shown by the block diagram in Figure 3.



a.)

b.)

Figure 3. Experimental setups for a.) quasi-static C-V measurements, b) life time measurements.

The quasi-static CV measurements on the structures are performed using the setup shown in Figure 3a consisting of an HP 4192A impedance analyzer, HP 4145B semiconductor parameter analyzer and Karl Suss PM8 probe station. Measurements with applied actuation voltage in the range of 0 - 35 volts show minor increase in the obtained capacitance values due the lowering of the air bridges during the subsequent measurements. Increasing the applied voltage range to 1.5 to 2 times the pull-in voltage provides direct measurements of the pull-in voltage and capacitance of each bridge.

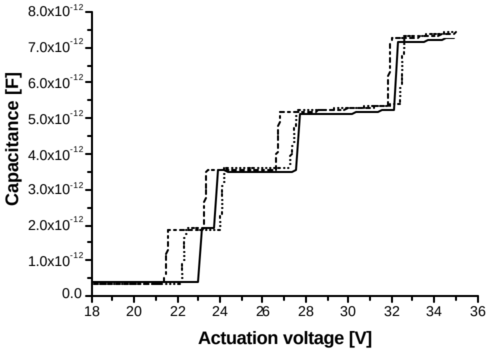
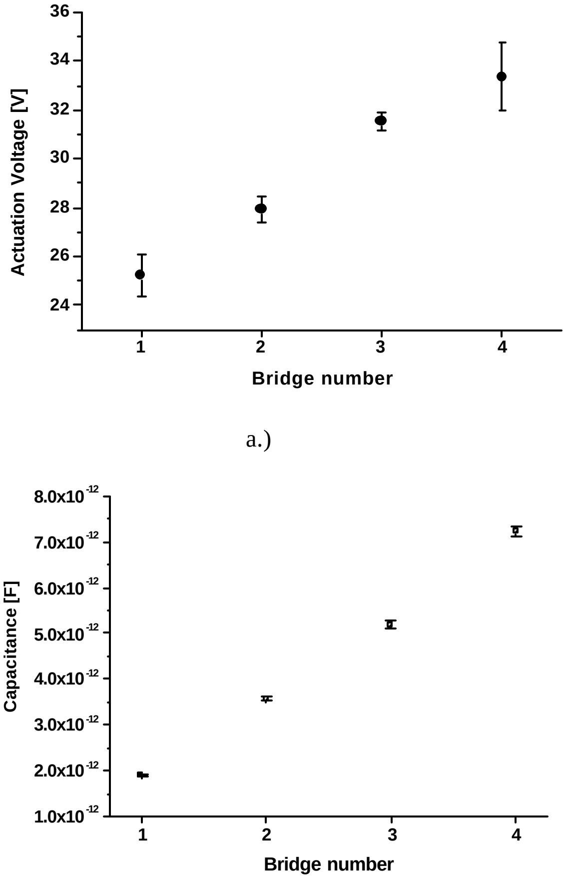


Figure 4. Set of three successive C-V measurement of four (1-4) microbridges.

Figure 4 shows the CV plots for three structures having the same geometrical characteristics on a wafer with SiO_2 as dielectric material, clearly identifying the individual actuation steps corresponding to respective ON – capacitance values.

The variations in the pull-in voltage and associated capacitance for 4 composite test structures are shown by Figure 5a and 5b. The comparatively large variations in pull-in voltage and corresponding capacitance in the case of a few microbridges, may be attributed to the process non-uniformities and deformation of the membranes, changing the effective spring constant. CV measurements repeated over a time period, in case of devices with silicon nitride on actuation pads show a significant drift in pull-in voltage values as compared to the devices with oxide insulation. Changes in capacitance values for certain devices may be due to the initial beam deformation and subsequent non-uniform bending of the beam under actuation force, as shown in Figure 6.



a.)

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Figure 5. a.) Actuation voltage and b.) capacitance vs bridge plots.

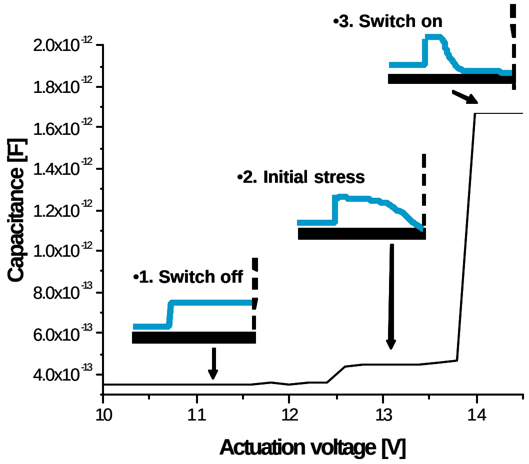

Figure 6. Different capacitance values ascribed to different microbridge bending effect .

The block diagram of the set up for life time measurements and quasi static CV measurements using custom built actuation signal source is shown in Figure 3b. The actuation signal amplitude can be varied from 0-200 volts while 50% duty period ranges from 10^{-5} sec to 1sec. The reduction in actuation signal amplitude after the device has switched on results in reduction of electric field across the dielectric layer by more than 1 MV/cm. The field is enough to keep the device in on state while reducing the charging effects considerably.

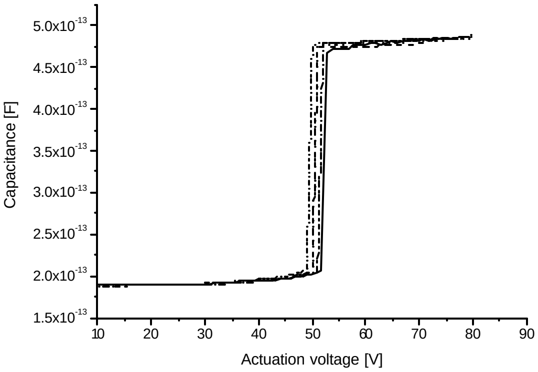

Figure 7. C-V measurements after cycle of stress procedures.

The drift in pull-in voltage is considerably reduced for repeated measurements on the device as shown in Figure 7. The field reduction also averts the stiction problems and premature failure of the switch [6].

5 CONCLUSIONS

In this preliminary work, an experimental setup and test structures for on-wafer characterization of the electromechanical performances of the suspended bridge have been illustrated in depth. The bridge capacitance and actuation voltage variations due to charging effects during quasi-static C-V measurements have been investigated. In the experimental measurements the large variations in pull-in voltage and corresponding capacitance, have been observed in silicon nitride based devices with respect the silicon oxide based one. The different behavior may be attributed both to the charge stored in the silicon nitride during the fabrication and in the minor charge mobility in the silicon oxide.

Future work will be devoted to examine carefully the minimal charge generation in the dielectric layer and capacitance measurements over long measurement periods.

ACKNOLEDGMENTS

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