



Sensor Design Optimization of Innovative Low-Power, Large Area FD-MAPS for HEP and Applied Science

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Fully depleted monolithic active pixel sensors (FD-MAPSs) represent a state-of-the-art detector technology and profit from a low material budget and cost for high-energy physics experiments and other fields of research like medical imaging and astro-particle physics. Compared to the MAPS currently in use, fully depleted pixel sensors have the advantage of charge collection by drift, which enables a fast and uniform response overall to the pixel matrix. The functionality of these devices has been shown in previous proof-of-concept productions. In this article, we describe the optimization of the test pixel designs that will be implemented in the first engineering run of the demonstrator chip of the ARCADIA project. These optimization procedures include radiation damage models that have been employed in Technology Computer Aided Design simulations to predict the sensors' behavior in different working environments.

Keywords: MAPS, radiation detectors, CMOS, TCAD simulations, pixel detectors

1 INTRODUCTION

Silicon pixel detectors generally consist of a matrix of sensing diodes connected to readout electronics. Currently, there are two major types of technology used to implement this class of devices. First, hybrid detectors that have the electronics integrated readout circuit on a separate die from the sensing active silicon substrate. In these devices, each pixel is connected via bump bonding to the readout circuitry [1]. Second, monolithic detectors that have the electronics integrated into the same Si substrate according to three main technological realizations: (semi-monolithic) depleted field effect transistor (DEPFET) pixels [2, 3], silicon-on-insulator (SOI) active pixels [4], and CMOS monolithic active pixels [5, 6]. The DEPFET pixel technology offers very low-noise characteristics due to the small capacitance of the collection node. It is used in the Belle II experiment [7] as well as light source facilities and astronomy [8]. The limitation of this technology lies in the necessary discharge of the collected electrons below the collection node, which requires comparatively low occupancy and low radiation environments, and the necessity of additional external circuits for control and readout. The SOI sensors use a thin low-resistivity Si layer for the circuit implementation and a high-resistivity bottom wafer. These two layers are separated by a buried oxide layer, which enables thin substrate thicknesses and small pitches with low capacitance [9]. However, these devices suffer from high sensitivity to radiation mainly due to the accumulation of positive oxide charges in the buried oxide layer [10].

Recent advancements in CMOS monolithic active pixel sensors (MAPSs) have demonstrated their ability to operate in high-radiation environments of up to multiple kGy's [11], which increased their

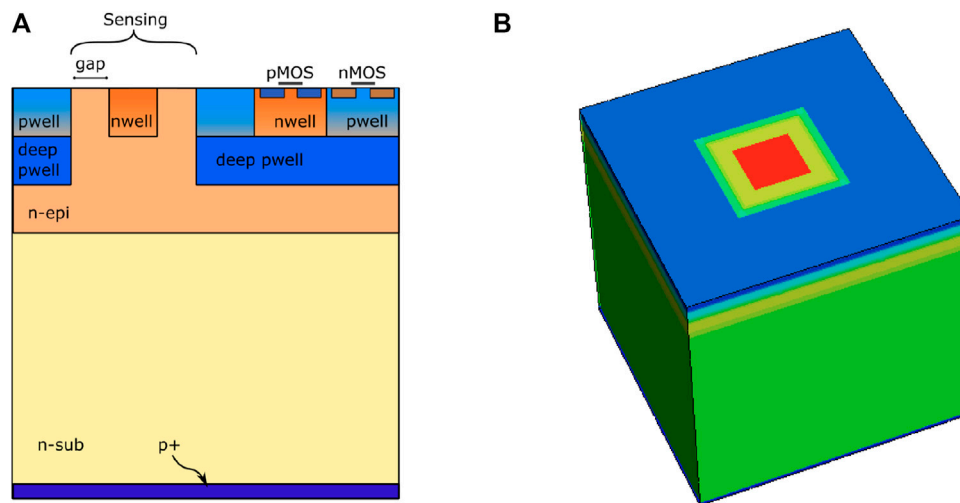


FIGURE 1 | (A) Schematic of the ARCADIA pixel. **(B)** TCAD 3D single-pixel simulation domain. The color scale refers to the doping concentration.

appeal as sensors for high-energy physics detectors. The most recent example in such an application is the new ALICE Inner Tracking System [12], entirely instrumented with CMOS MAPS, that covers an area of about 10 m^2 . However, the full potential of such devices has not yet been fully exploited, especially with respect to the size of the active area, power consumption, and timing capabilities. Ongoing developments concentrate on FD-MAPS that profit from a charge collection by drift [13–15].

The ARCADIA project is developing FD-MAPS with an innovative sensor design, which uses backside bias to improve the charge collection efficiency and timing over a wide range of operational and environmental conditions. The sensor design targets very low power consumption, in the order of 20 mW cm^{-2} at 100 MHz cm^{-2} particle flux, to enable air-cooled operation. Another key design parameter is the ability to further reduce the power regime of the sensor, down to 5 mW cm^{-2} or lower, for low hit rates, e.g., in space applications. The FD-MAPS architecture, initially embodied in a 512×512 pixel matrix, should enable the scalability of the sensor up to matrix sizes of 2048×2048 pixels. Maximizing the active area of the single sensor (10 cm^2 or bigger) simplifies and reduces the costs of detector construction and even enables applications where no support material over the entire sensor area can be tolerated (e.g., medical scanners).

The sensor design is based on a modified 110 nm CMOS process and incorporates a low-doped n-type silicon active volume with a p^+ region at the bottom (Figure 1). This structure will be obtained using two alternative approaches depending on the thickness of the active volume. For thick sensors, exceeding $100 \mu\text{m}$, the fabrication will be based on high-resistivity n-type substrates, and the p^+ region will be formed by backside processing. For sensors thinner than $100 \mu\text{m}$, on the contrary, low-doped n-on- p^+ epitaxial substrates will be used. The p-n junction sits on the bottom of the sensor, which results in the depletion region growing from the backside surface with increasing bias voltage. These FD-MAPS are thus operational at low front-side supply voltages while providing a

fully depleted silicon bulk, which allows the electrode on the top to read out fast electron signals produced by drift.

The process allows for the integration of both analog and digital CMOS circuits based on 1.2 V transistors and thus a readout electronic circuit similar to the one of a previous prototype [17]. A more compact circuit, such as the one used in the ALPIDE chip [12], has also been designed and will be tested in a dedicated prototype. A more detailed description of the processing is provided in [16].

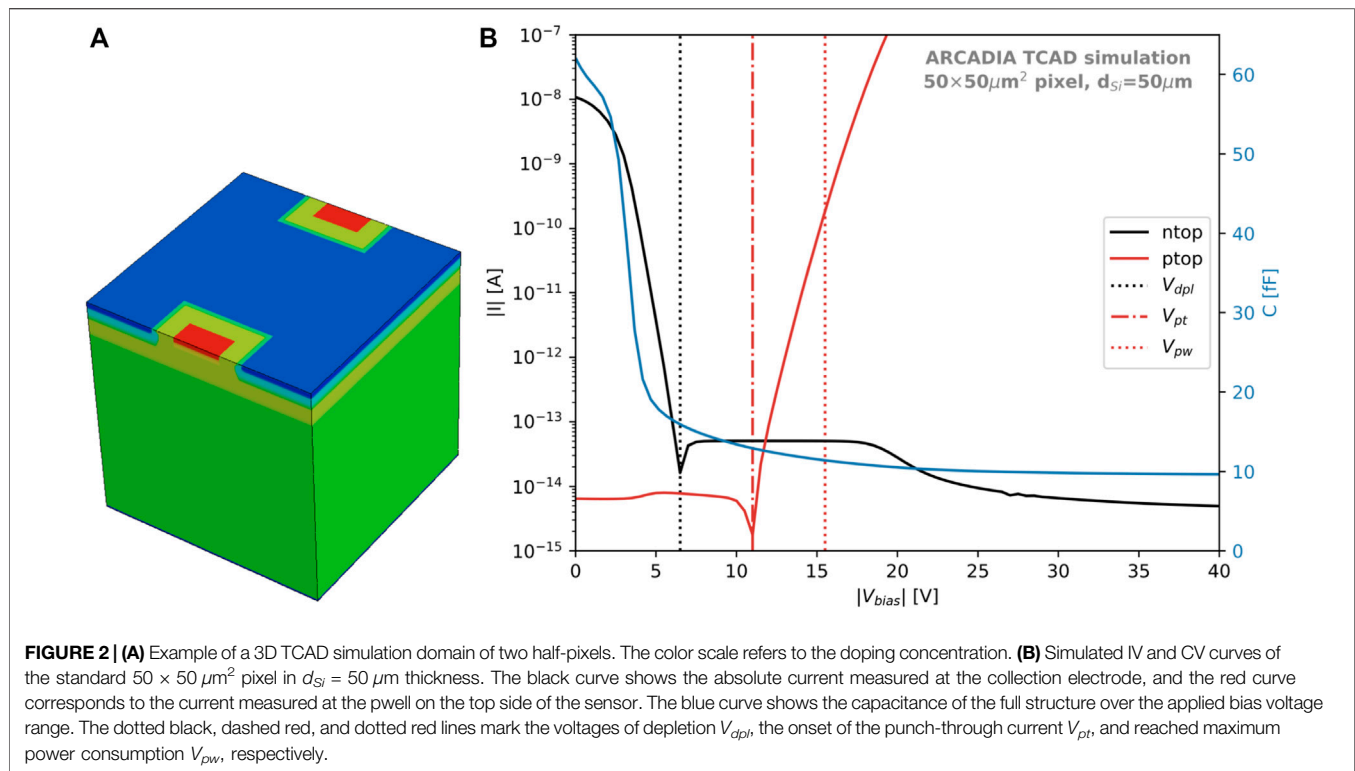
The ARCADIA collaboration is currently working on a large-area prototype of $1.3 \times 1.3 \text{ cm}^2$ active area consisting of 512×512 pixels with $25 \mu\text{m}$ pitch, to be realized in a first engineering run with integrated digital electronics. Additional test structures of pixel matrices with pixel pitches ranging from 10 to $50 \mu\text{m}$ and total thicknesses of $50\text{--}300 \mu\text{m}$ will also be produced. In the following, we report on the simulations and the optimization procedures of the sensor designs that have been developed in preparation of the production run.

This study is organized as follows: **Section 2** describes the pixel geometry and the simulation settings that were used in the analysis of the device characteristics. Additionally, the radiation damage models used for the predictions after irradiation are introduced, and the first observations are discussed. The optimization targets, methods, and results are described in **Section 3**. The conclusions are given in **Section 4**.

2 TCAD SIMULATIONS

The electrical characteristics of the pixels are analyzed using Technology Computer Aided Design (TCAD) simulations¹. The TCAD simulation domains are realized in 3D, as visualized for a single-pixel domain with $50 \mu\text{m}$ thickness, in Figure 1B. The

¹Synopsys Sentaurus Version P-2019.03-SP1.



collection electrode is biased at $+0.8 \text{ V}$, and the reverse bias voltage is applied from the back side of the pixel. Three different substrate thicknesses of 50, 100, and $300 \mu\text{m}$ are simulated, using the same doping profiles provided by the foundry. This basic simulation setup has been previously validated with a production series, under the SEED project [17].

All simulations, if not stated otherwise in the figures, are performed at 300 K .

The simulations neglect the nwell regions used in the implementation of PMOS transistors, assuming that the electrical characteristic and the radiation detection are not significantly affected.

Due to the wide range of planned applications, these studies include a detailed analysis of the impact of different radiation levels on the pixel characteristics using radiation damage models for both the silicon bulk and the Si-SiO₂ interface. The adopted models, as well as the simulation results, are discussed in **Section 2.2**.

2.1 Electrical Characterization

An example of the capacitance-voltage (CV) and current-voltage (IV) curves of a $50 \times 50 \mu\text{m}^2$ pixel is shown in **Figure 2B**. The CV characteristics are, if not stated differently, simulated in AC with a frequency of 10 kHz . The black curve in **Figure 2B** represents the current measured at the collection diode and has been obtained from two half-pixel domains, shown in **Figure 2A**, with a 10 mV voltage difference applied at the top electrodes. In this way, a non-negligible current is flowing between the pixels if the substrate is not fully depleted. The red and blue curves correspond to the current measured at the top pwell and

capacitance measured at the collection electrode in single-pixel simulations, respectively. The dotted and dashed lines highlight the depletion voltage and onset of the punch-through currents, respectively. Both IV curves feature the point of sign change from negative to positive current values in the form of dips in their absolute spectrum. These are defined as the voltage needed for full depletion V_{dpl} and onset of the punch-through currents V_{pt} and correspond to the moment in which the single pixels become isolated from each other through the depletion region and the moment in which the exponential increase of hole current between the pwell implantations and the backside p⁺ contact starts. The sensors can be biased at a voltage higher than V_{pt} as long as the power consumption is not too large. Therefore, it is useful to extract the maximum allowed bias voltage at which a power consumption of 0.1 mW/cm^2 is reached. This voltage is marked as a dotted red line and will be referred to as V_{pw} in the following.

As it is visible in **Figure 2B**, comparing the black dotted line and blue curve, the depletion voltage of these devices does not necessarily correspond to the voltage at which the minimum capacitance is reached. Due to the low-doped epitaxial layer, full depletion of the substrate including the epi-layer is only achieved at much higher voltages.

In the following analysis, capacitances and leakage currents are extracted at V_{pt} , which have been chosen as an optimal and safe operating point.

2.2 Prediction of Radiation Tolerance

The ARCADIA sensors are designed for a wide range of applications, which include HEP collider experiments. Future

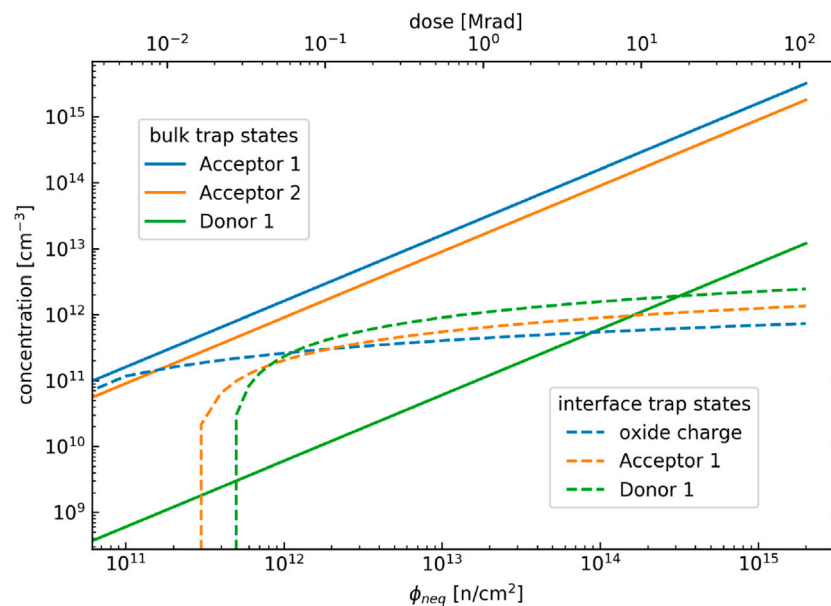


FIGURE 3 | Trap concentrations as a function of the neutron equivalent fluence (bottom axis) and total ionizing dose (top axis) [21]. The solid and dashed lines correspond to the trap states in the silicon bulk and at the Si-SiO₂ interface, respectively. The trap properties are listed in **Table 1**.

collider experiments, like the FCC, require good timing performance and (partially) high-radiation tolerance, especially for the central tracking and vertex detectors [18, 19].

Ionizing radiation not only damages the surface of the sensor, which produces oxide charges at the interface between the Si and SiO₂ surface, but also creates cluster and point-like defects in the silicon crystal lattice. These defects result in new energy levels within the bandgap and can function as traps, which get electrically active when

occupied, thus changing the electrical properties of the sensors, such as the depletion voltage (effective doping concentration) and the leakage (or dark) current.

For a most realistic prediction of the impact of these defects, we have modeled both damage types, following the so-called *new Perugia model* [20, 21]. This three-trap model introduces two acceptors and one donor state in the bandgap for the description of non-ionizing radiation damage in the silicon bulk. In addition, two trap states at the Si-SiO₂ interface are

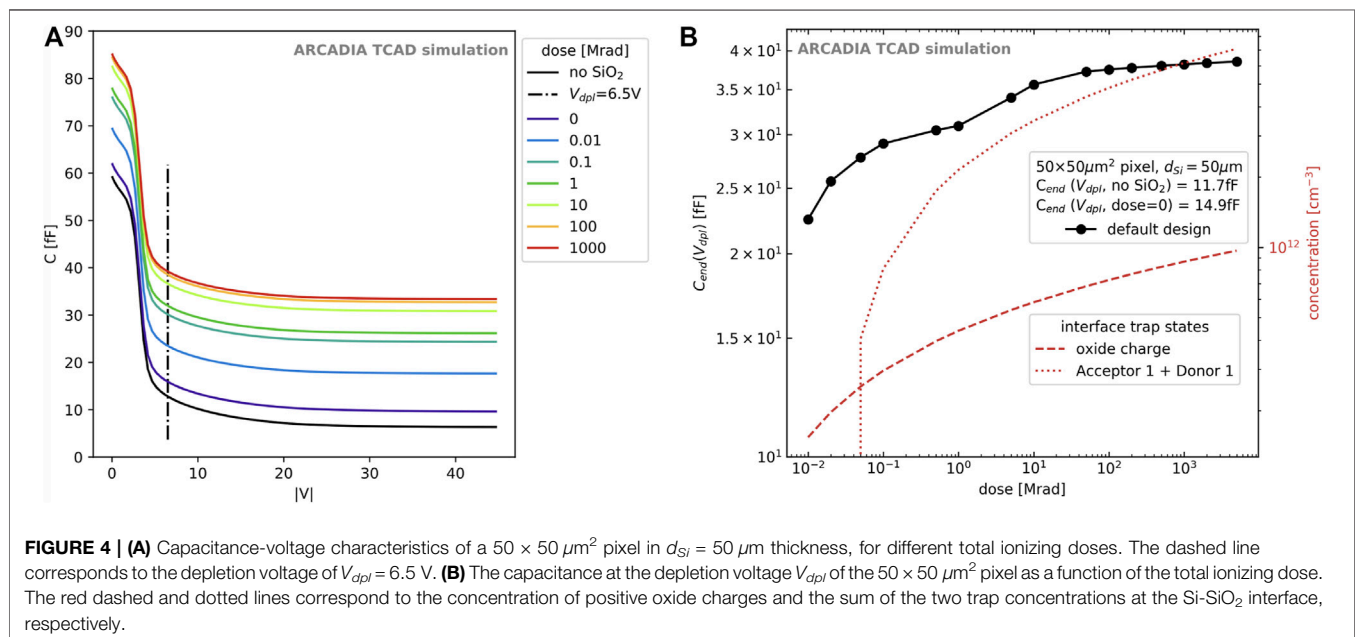


FIGURE 4 | (A) Capacitance-voltage characteristics of a $50 \times 50 \mu\text{m}^2$ pixel in $d_{\text{Si}} = 50 \mu\text{m}$ thickness, for different total ionizing doses. The dashed line corresponds to the depletion voltage of $V_{\text{dpl}} = 6.5 \text{ V}$. **(B)** The capacitance at the depletion voltage V_{dpl} of the $50 \times 50 \mu\text{m}^2$ pixel as a function of the total ionizing dose. The red dashed and dotted lines correspond to the concentration of positive oxide charges and the sum of the two trap concentrations at the Si-SiO₂ interface, respectively.

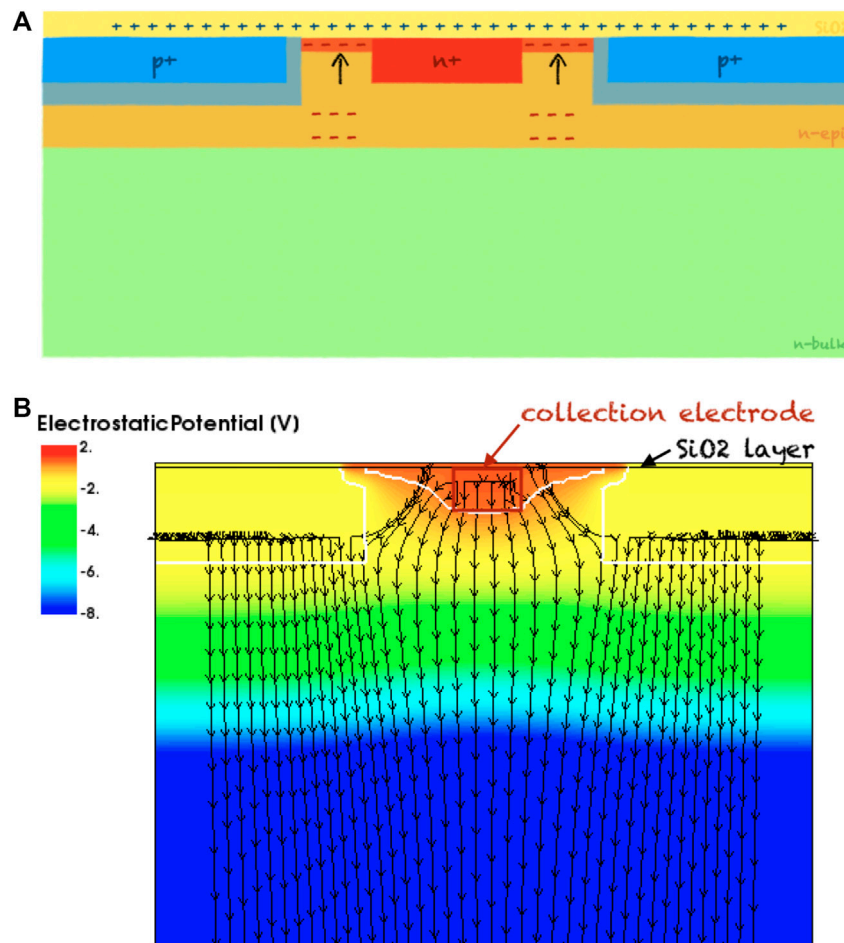


FIGURE 5 | (A) Schematic of the impact of positive oxide charges at the interface between silicon and Si-SiO₂. **(B)** Electrostatic potential across the center of a 25 × 25 μm² pixel including a SiO₂ layer and positive oxide charges corresponding to 50 Mrad total ionizing dose. The black arrows show the electric field lines, and the white lines mark the depletion region.

TABLE 1 | Properties for the two surface and three bulk traps [21]; listed as in which material they are introduced, how they are named in **Figure 3**, which energy level in the Si bandgap they occupy, and their electron σ_e and hole σ_h capture cross-sections, respectively.

| Material | Name | Energy level (eV) | σ_e (cm ²) | σ_h (cm ²) |
|------------------|------------|-------------------|-------------------------------|-------------------------------|
| SiO ₂ | Acceptor 1 | $E_C - 0.56$ | 1×10^{-16} | 1×10^{-15} |
| | Donor 1 | $E_V + 0.6$ | 1×10^{-15} | 1×10^{-15} |
| Si bulk | Acceptor 1 | $E_C - 0.42$ | 1×10^{-15} | 1×10^{-14} |
| | Acceptor 2 | $E_C - 0.46$ | 7×10^{-14} | 7×10^{-13} |
| | Donor 1 | $E_C - 0.23$ | 2.3×10^{-14} | 2.3×10^{-15} |

introduced to describe the effects of ionizing energy losses, together with fixed oxide charges which build up due to trapped charges in the SiO₂ layer.

While this model has been tuned and validated on p-type silicon, it has shown good performance for sensors produced by different vendors [20]. These results make us confident that the model has a good qualitative predictive power also for the ARCADIA sensors. However, a variation in absolute values of

leakage current and capacitance can be expected due to varying impurity concentrations in the substrate.

2.2.1 Surface Damage

To estimate the impact of surface damage on the sensor properties, we have employed a SiO₂ layer that features positive oxide charges. The concentration of these charges increases with the modeled total ionizing dose (TID), along with defect levels in the bandgap. We are following the model introduced and summarized in [21]. The trap and oxide charge concentrations are plotted as a function of the 1 MeV neutron equivalent fluences and the dose in **Figure 3**. Here, the fluence dose relation is used for 24 GeV protons of the CERN Proton Synchrotron with a proton hardness factor of 0.6 and a damage factor of $D/\phi = 3.3 \times 10^{-8} \text{ rad}/(\text{proton}/\text{cm}^2)$ [22]. Because most potential applications of the ARCADIA technology do not expect doses greater than 10 krad, this value has been chosen as a reference for capacitance and leakage current estimates. This study, however, includes predictions for doses of up to 1 Grad, due to the availability of models describing radiation damage

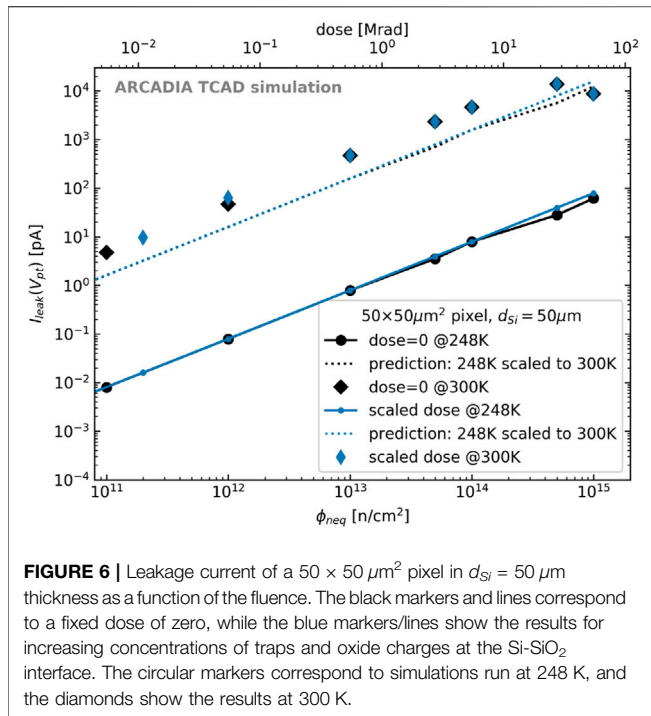


FIGURE 6 | Leakage current of a $50 \times 50 \mu\text{m}^2$ pixel in $d_{\text{Si}} = 50 \mu\text{m}$ thickness as a function of the fluence. The black markers and lines correspond to a fixed dose of zero, while the blue markers/lines show the results for increasing concentrations of traps and oxide charges at the Si-SiO₂ interface. The circular markers correspond to simulations run at 248 K, and the diamonds show the results at 300 K.

induced by high doses and in view of a validation of this technology for harsh environments.

The impact of the SiO₂ and of the induced positive oxide charges is visible in the CV curves, as presented in **Figure 4A**, of the example of a $50 \times 50 \mu\text{m}^2$ pixel. An increase of the capacitance is observed over the full voltage range (from 0 to -50 V). This effect is present for all the pixel pitches. The CV curve without the SiO₂ layer is represented by the black line and shows the smallest values. When the SiO₂ layer is included, with a minimal concentration of positive oxide charge and traps, an increase of about 3 fF at the depletion voltage (-6.5 V) is observed. The capacitance more than doubles with an increasing dose of up to 5 Grad (50 MGy), the capacitance more than doubles. The first increase of the capacitance at the depletion voltage $C_{\text{end}}(V_{\text{dpl}})$ for low doses ($< 1 \text{ Mrad}$), a second increase after 1 Mrad, and a saturation above 100 Mrad are shown in **Figure 4B**. The two steps can be directly correlated to the positive oxide charge and trap concentrations at the Si-SiO₂ interface, as shown in red dashed and dotted lines, respectively.

The main impact of the increased trap concentration is a higher surface recombination velocity, while the positive oxide charges attract free electrons from the n-type epi layer and create an effective extension of the collection electrode. This effect is schematically visualized in the top plot of **Figure 5A**, and its impact on the electrostatic potential and the electric field lines is shown in **Figure 5B**.

The strength of this effect depends on the sizes of the collection electrode and of the implant-free gap size between the diode and the pwell of the pixel. This allows for an optimization of the geometry and will be further discussed in **Section 3.1**.

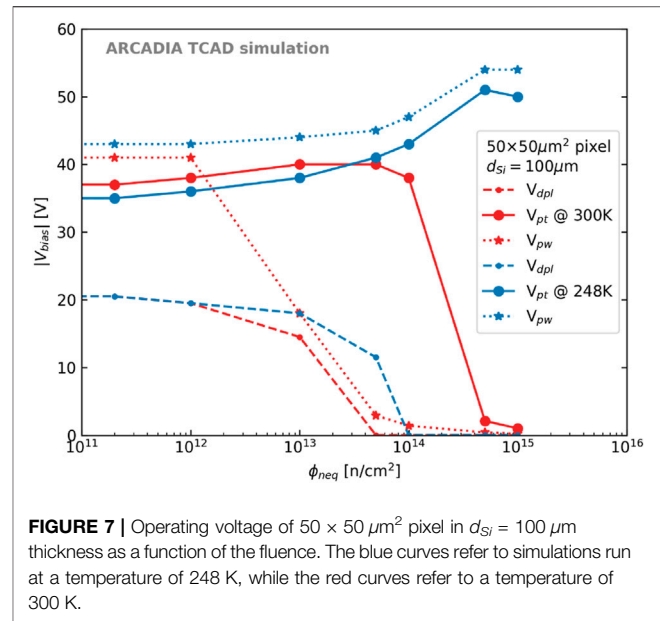


FIGURE 7 | Operating voltage of $50 \times 50 \mu\text{m}^2$ pixel in $d_{\text{Si}} = 100 \mu\text{m}$ thickness as a function of the fluence. The blue curves refer to simulations run at a temperature of 248 K, while the red curves refer to a temperature of 300 K.

2.2.2 Bulk Damage

To simulate the pixels' electrical characteristics after irradiation with hadrons, we have employed three trap models, similar to [23, 24]. The main properties, like the activation energy, and the capture/emission cross-sections for electrons and holes of the defect levels are summarized in **Table 1**.

The concentration of these traps increases linearly with the fluence, as shown in **Figure 3**, and this results in a linear increase of the leakage current. This effect is shown in **Figure 6**, together with the comparison of a simple scaling of the current from low ($T_1 = 248 \text{ K}$) to high ($T_2 = 300 \text{ K}$) temperatures, following [25]:

$$\frac{I(T_2)}{I(T_1)} = \left(\frac{T_2}{T_1}\right)^2 \exp\left(-\frac{E_{g,\text{eff}}}{2 \cdot k_B} \left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right), \quad (1)$$

with $E_{g,\text{eff}} = 1.214 \text{ eV}$. **Figure 6** shows the measured leakage current at V_{pt} as a function of the fluence ϕ_{neq} for $50 \times 50 \mu\text{m}^2$ pixels in $50 \mu\text{m}$ thickness. The first observation is that the induced surface damage has no significant impact on the leakage current, which is dominated by the volume generation currents induced by the bulk defects.

The second observation is made using **Eq. 1** to scale the values measured at 248 K up to room temperature (shown in dotted lines). Since the model parameters are fitted to measurements at 248 K, it has to be mentioned that we observe a difference between the simulation results at 300 K and the scaling from 248 K, of factor three.

Evaluating the operating voltages as a function of the fluence (**Figure 7**), a drop in the depletion voltage is visible for fluences $> 1 \times 10^{13} \text{ cm}^{-2}$. This is consistent with a change of the effective doping concentration within the Si bulk, due to the introduced trap levels. The added acceptor levels first neutralize the n-type doping of the bulk and, with increasing concentration, invert the doping to p-type. Consequently, the pn junction is moved from

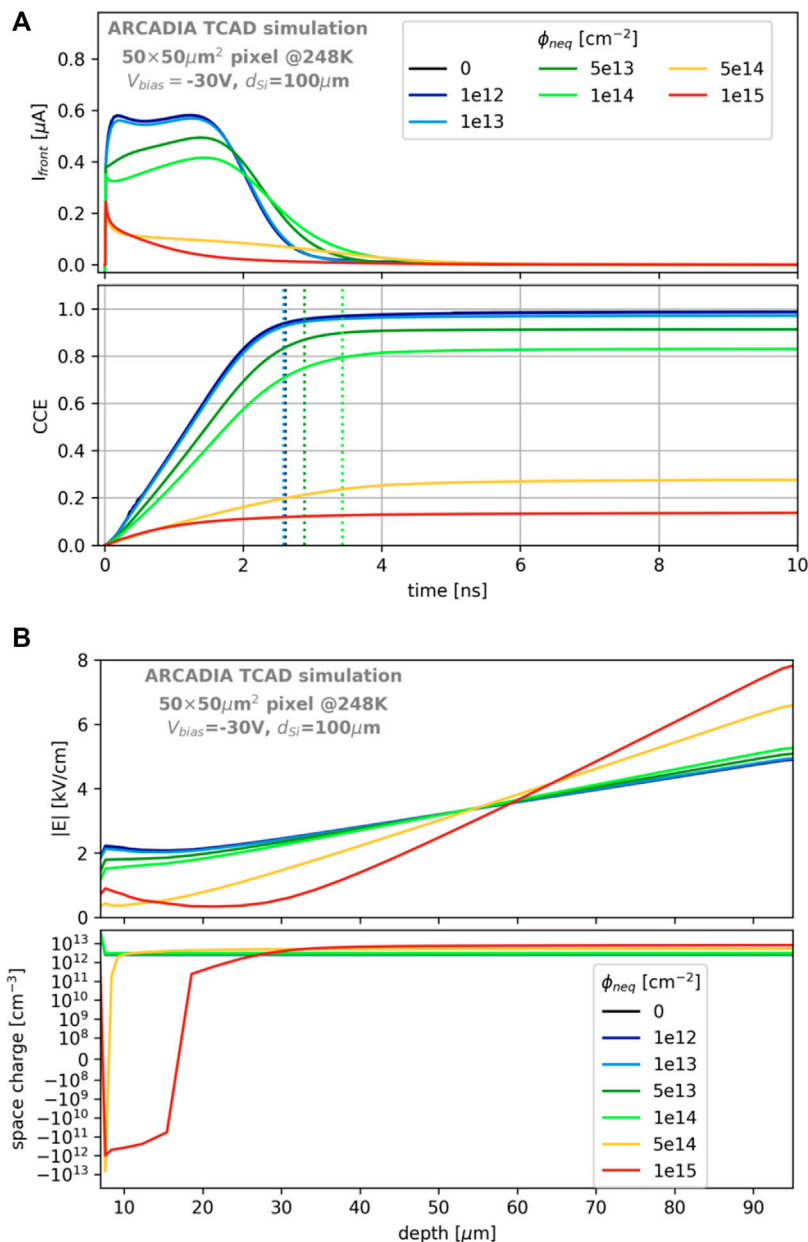


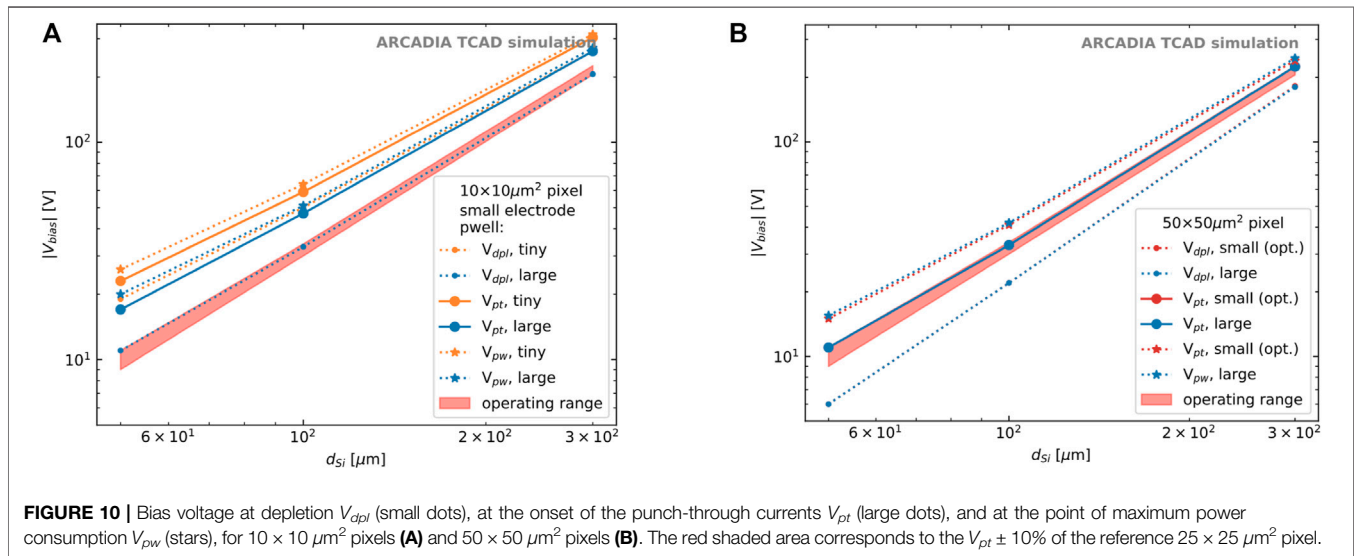
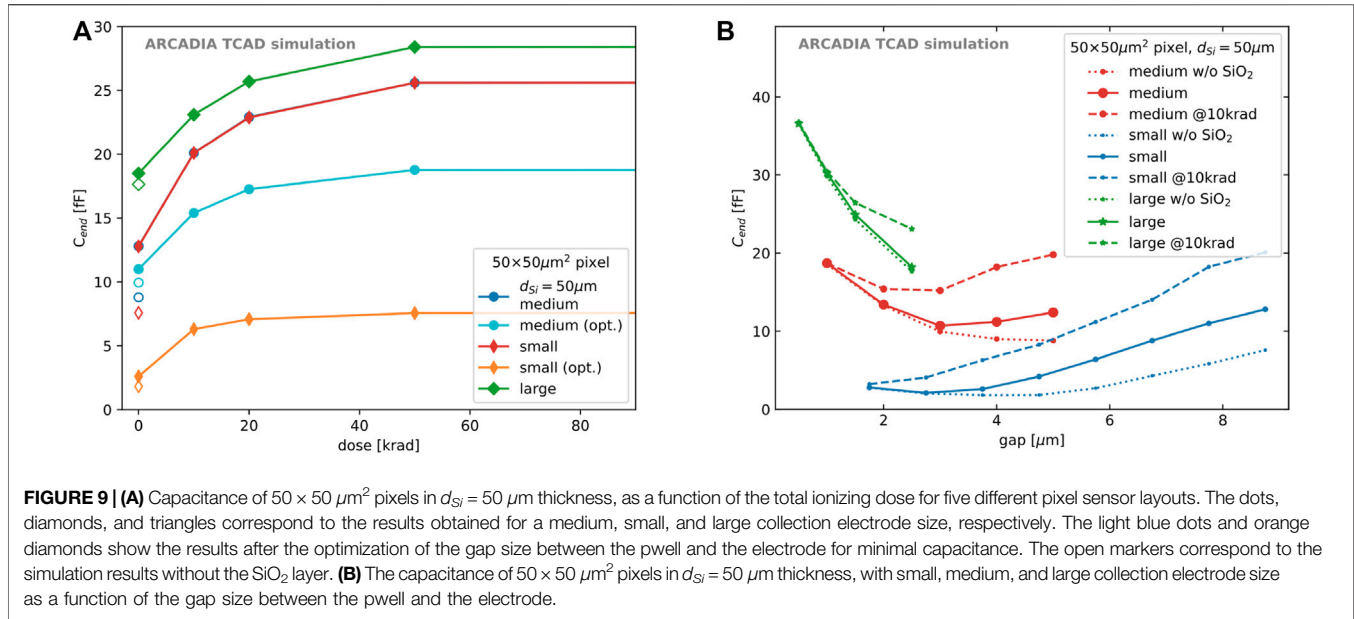
FIGURE 8 | (A) Current signals (**top**) and charge collection efficiency (**bottom**) of a $50 \times 50 \mu\text{m}^2$ pixel in $d_{\text{Si}} = 100 \mu\text{m}$ thickness, after neutron equivalent fluences of $0-1 \times 10^{15} \text{cm}^{-2}$, simulated at $V_{\text{bias}} = -30 \text{V}$. The dotted lines mark the time of 95% charge collection. **(B)** Electric field (**top**) and space charge (**bottom**) as a function of the sensor depth for different fluences in the same pixel sensor.

the back side to the border of the epi layer and the bulk to the front side of the sensor.

In conventional Si diodes, the depletion voltage is expected to increase after the inversion of the effective doping of the silicon bulk [26]. However, for these pixel sensors, the depletion voltage is defined as the reverse voltage at which neighboring pixels become isolated by a depletion region, which corresponds to full bulk depletion before irradiation. But as soon as the bulk is type-inverted, the depletion region starts to grow from the front side between the epi layer and the bulk; therefore, already with the small

applied voltage of 0.8 V at the collection electrode, the electrodes of the pixels become isolated without any reverse bias applied.

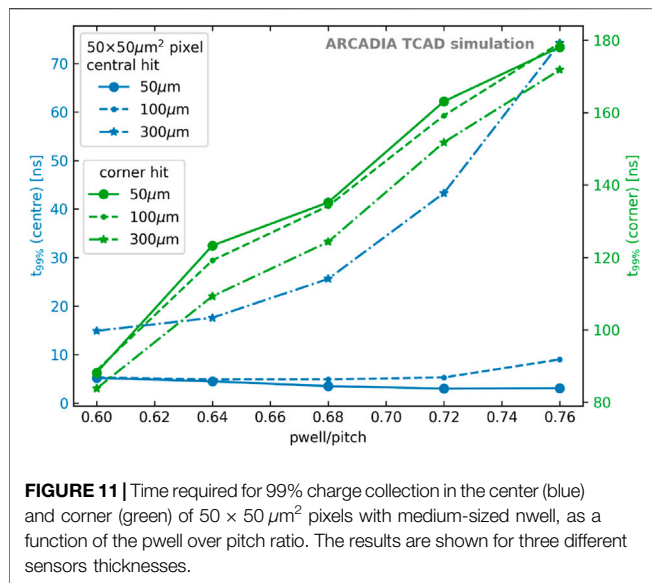
The type-inversion of the sensors above fluences of $1 \times 10^{14} \text{cm}^{-2}$ can be confirmed by comparing transient simulations of minimum ionizing particles (MIPs) using the *HeavyIonModel* of TCAD [27]. This model was used to simulate the charge deposition along a track within the sensor, defining the amount of generated charge as a function of the path length by the linear energy transfer (LET). Complementary GEANT4 simulations have been used to confirm the average charge deposition of MIPs of



$\sim 80 \text{ e/h}$ pairs or $1.28 \times 10^{-5} \text{ pC per } \mu\text{m}$. The charge deposition is instantaneously introduced after 10 ps, and the resulting transient signal is shown in the top plot of **Figure 8A** for a MIP incident in the pixel center, along a perfectly perpendicular trajectory, for fluences from zero up to $1 \times 10^{15} \text{ cm}^{-2}$. The transients have been simulated at $V_{bias} = -30 \text{ V}$, thus well above the depletion voltage over the full fluence range, and the time necessary to reach 95 and 99% charge collection efficiency (t_{95} and t_{99}), respectively, is reported in the plot on the bottom. In order to avoid inaccuracies of the simulation that impact the results, these times are defined as:

$$\frac{\int_t^{t_{95/99}} I_{front} \cdot dt}{\int_t^{t=200\text{ns}} I_{front} \cdot dt} = 0.95/0.99. \quad (2)$$

At low fluences $< 5 \times 10^{13} \text{ cm}^{-2}$, the pulse shapes present a fast component due to the quickly collected electrons near the collection electrode and a second peak due to the strong electric field at the pn junction on the back side of the sensor, which results in a higher drift speed of the charges generated close to the back side compares to the charges originating at the pixel center. The electric field at $V_{bias} = -30 \text{ V}$ is shown in the top plot of **Figure 8B** at different fluences. After moderate irradiation of up to $1 \times 10^{14} \text{ cm}^{-2}$, the electric field at the front becomes weaker, and the electrons get trapped by the increasing concentration of acceptor levels. For the highest fluences, a critical amount of the acceptors gets ionized and thus contributes to the space charge, as shown in the bottom plot in **Figure 8B**. The space charge becomes negative below the electrode, where the electron density is highest, which results in a double peak in the electric field [28]. Additionally,



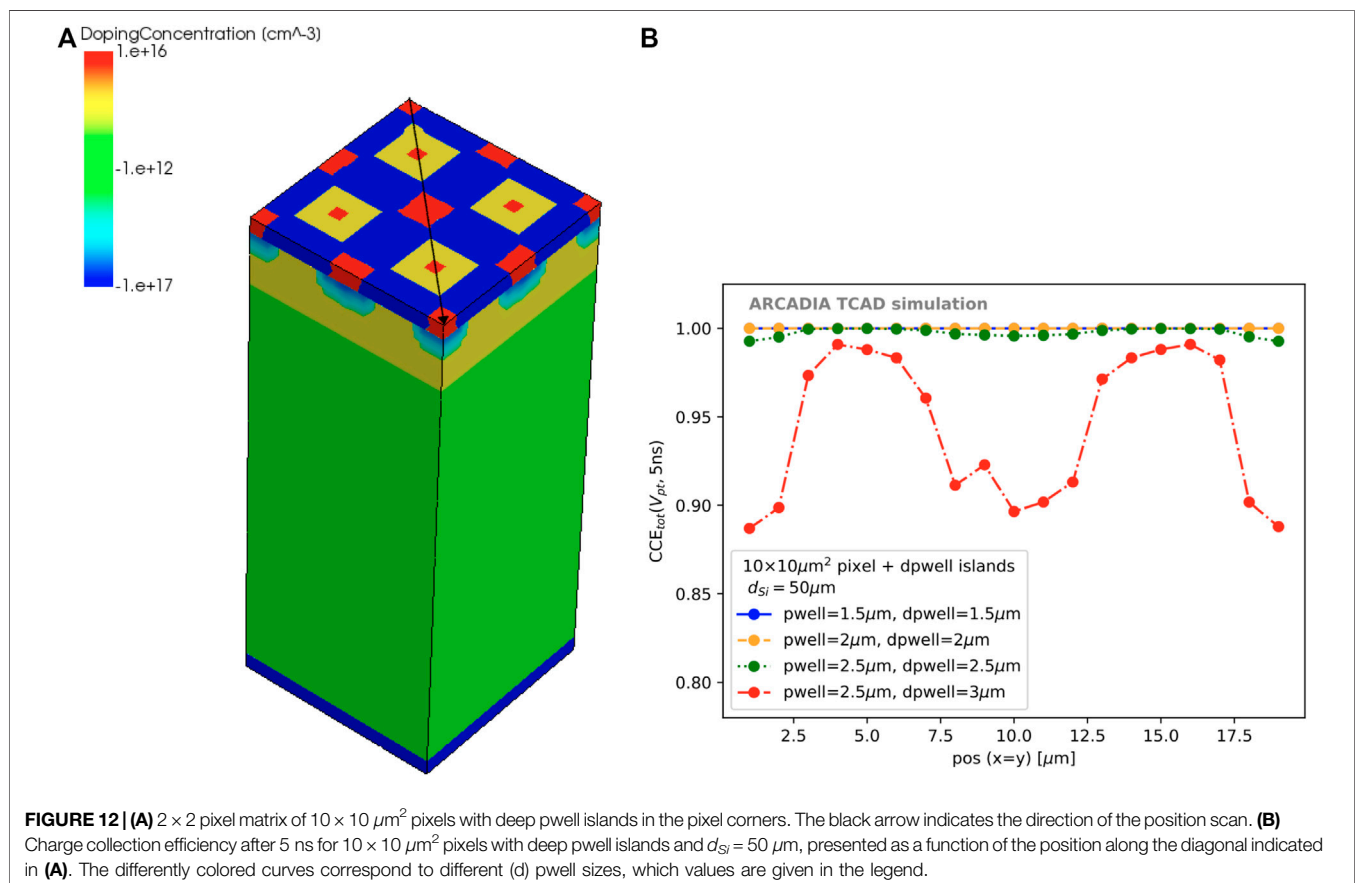
the total collected charge significantly decreases at these extreme fluences due to the high concentration of donor as well as acceptor traps. The hole contribution to the signal seems to vanish completely after a fluence of $\phi_{neq} = 1 \times 10^{15} \text{ cm}^{-2}$, and the total collected charge lies below 20%.

The occupation of traps is dependent on the amount of available free charge carriers, as well as on the leakage current, the applied bias voltage, and the capture cross-sections. This results, e.g., in a stronger double junction at higher temperatures due to easier occupation of the traps and higher leakage currents. Since the employed trap model has been fit to data at 248 K [21], we report here only the results at 248 K. It should be mentioned that the amount and the type of radiation-induced bulk defects depend on the particle type as well as on the particle energy of the irradiation [29]. In addition, the original impurities within the Si, like oxygen, can support or prevent the creation of certain defects [30, 31].

3 DESIGN OPTIMIZATIONS

The pixel design optimization targets a small pixel capacitance to ensure low electronics noise, thus maximum signal to noise ratio, and high charge collection efficiencies within the smallest possible time windows in order to decrease dead-times for high particle rates.

To choose only a few geometries for each pixel pitch ($10 \mu\text{m}$, $25 \mu\text{m}$, and $50 \mu\text{m}$) with optimal performance, a large range of simulations with the different electrode and pwell sizes has been performed. The results of this simulation campaign are



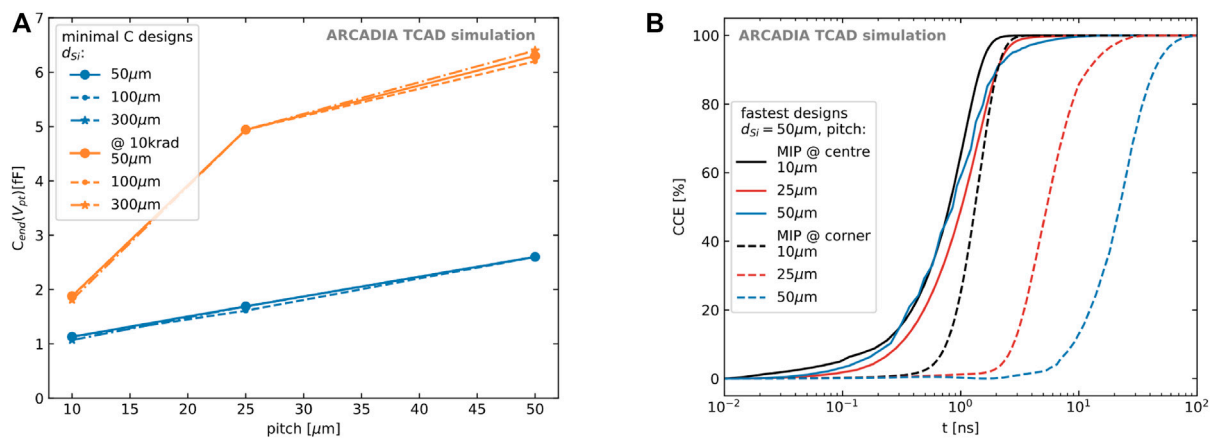


FIGURE 13 | (A) Capacitance at V_{pt} for the optimized designs of pixels with 10, 25, and 50 μm pitch, at a dose equal to 0 in blue and after a dose of 10 krad in orange. **(B)** Charge collection efficiencies for MIPs impinging at the center (straight lines) and corner (dashed lines) of the pixels, for the selected design of pixels with 10, 25, and 50 μm pitch, before irradiation.

TABLE 2 | Times for 99% charge collection for MIP-like charge depositions at the center and the corner for pixels with three different pitches, given for three substrate thicknesses (50/100/300) μm .

| pitch (μm) | t_{99} (centre) (ns) | | | t_{99} (corner) (ns) | | |
|-------------------------|------------------------|-------------------|-------------------|------------------------|-------------------|-------------------|
| | 50 μm | 100 μm | 300 μm | 50 μm | 100 μm | 300 μm |
| 10 | 2.1 | 3.2 | 7.0 | 2.8 | 3.6 | 6.9 |
| 25 | 3.6 | 8.0 | 16.5 | 27.9 | 25.8 | 21.3 |
| 50 | 7.7 | 6.3 | 14.9 | 73.2 | 74.3 | 82.6 |

summarized into three different categories, focusing 1) on the pixel capacitance (Section 3.1), 2) on the bias voltage operating range (Section 2.1), and 3) on the charge collection (Section 3.3).

3.1 Minimizing the Pixel Capacitance

The pixel capacitance can be lowered by decreasing the size of the collection electrode. However, due to the impact of the positive oxide charges within the gap between the electrode and the pwell, the gap size plays a major role, and both quantities have to be analyzed in parallel. In the following, bulk damage is not considered in the comparisons between pixel designs, due to a negligible impact on the pixels' capacitance. An example of the importance of the gap size is visible in Figure 9A. The capacitance is shown as a function of the dose for small, medium, and large electrode sizes with default and optimized gap sizes. Here, the dose range has been limited to (0–100) krad, which covers the expected doses reached after a few years of operation within a medical scanner used for proton CT. Comparing the small electrode with the default gap size shows, without the recognition of the SiO_2 layer and without positive oxide charges, a smaller capacitance than the medium electrode with optimized gap size. However, as soon as oxide charges are introduced, the trend turns around, and the capacitance of the medium electrode stays ~30% lower than the capacitance of the non-optimized small electrode. While Figure 9A only shows the results for the 50 μm thick sensor, the same effect and very

comparable absolute values have been found for thicker substrates.

The capacitance for three different electrode sizes is shown as a function of the gap size for $50 \times 50 \mu\text{m}^2$ pixels in Figure 9B. Due to boundary conditions, the pwell has a minimum size to facilitate the integration of transistors for the electronics; hence, the gap size range is limited and most restricted for the largest electrode. For the $50 \times 50 \mu\text{m}^2$ pixel, we find a minimum capacitance for all electrode sizes at ~2.5 μm gap size, for simulations that include the SiO_2 layer. In the case of the large electrode size, it can be clearly seen that the capacitance decreases with increasing gap size, which corresponds to a smaller pwell size.

3.2 Operating Bias Voltage

The pixel designs for the different pitches impact these parameters due to changes in the electrostatic potential. Since the pixel design for the 25 μm pitch of the ARCADIA main demonstrator chip is fixed, its operating parameters are used as a reference to allow the operation of different pixel flavors on the test-structure.

Figure 10 shows the bias voltages (V_{dpl} , V_{pt} , and V_{pw}) for the three different thicknesses of the $10 \times 10 \mu\text{m}^2$ pixels (a) and $50 \times 50 \mu\text{m}^2$ pixels (b). The red shaded area marks the $V_{pt} \pm 10\%$ of the reference $25 \times 25 \mu\text{m}^2$ pixels. While the reference voltage lies nicely within the limits of all $50 \times 50 \mu\text{m}^2$ pixel designs, the minimum bias voltage of the $10 \times 10 \mu\text{m}^2$ pixels varies strongly for the different designs. Only one design, with a large pwell, can be considered operational (depleted) at the reference voltage.

The large difference in the operating bias voltage for the $10 \times 10 \mu\text{m}^2$ pixels has been an important observation and led to the conclusion that the test-structures with these pitches will be separated from the others in the final layout. This will ensure that a sufficient bias voltage can be applied from the front and back sides of the sensors for thicknesses of 50 μm and 100/300 μm , respectively.

3.3 Uniform Response

Transient simulations of MIP-like tracks have been used to evaluate the charge collection and response across the pixels. To evaluate the signals, usually the best- and worst-case scenarios are studied, which correspond to a traversing particle at the center and the corner of the pixel. For the comparison of different pixel designs, the time to collect 95 and 99% of the generated charges has been used. While charge losses due to radiation damage in the silicon crystal are not expected to vary between the pixel designs but rather with the substrate thickness, the study of response uniformity is neglecting bulk damage. The impact of surface damage on the signal formation has been tested in transient simulations and has been found to be negligible.

A general observation of the necessary time to collect 99% of all charges in the pixel corner is the strong dependence on the pwell width (**Figure 11**). Additionally, a large collection electrode size improves the collection of the charges from the corners of the pixels. However, the electric field strength below the collection electrode decreases with an increased collection node, which results in a slightly slower collection in the pixel center. Considering a homogeneous distribution of particles across the full area of the chip, this motivates an optimization for uniformity rather than peak performance in localized areas.

These considerations lead to a choice of $25 \times 25 \mu\text{m}^2$ and $50 \times 50 \mu\text{m}^2$ pixels, with minimum pwell and maximal electrode size. Due to the small pitch, the $10 \times 10 \mu\text{m}^2$ pixels are much less affected by slow charge collections in the pixels' corners. Instead, charge sharing is much more pronounced, and the larger concern lies in the so-called *channel choking*, which describes the effect of a potential barrier occurring when the sensing window becomes too small in comparison to the pwell size. To overcome this problem, a design that features the electronics in islands of deep pwells within the pixel corners has been studied, and a picture of a 2×2 pixel matrix is shown in **Figure 12A**. With this approach, a large enough (deep) pwell size can be achieved to allow for the integration of the electronics without the risk of a non-functional diode.

The resulting charge collection efficiencies for a range of (deep) pwell sizes, given here in half-sizes, are presented in **Figure 12B** at $t = 5 \text{ ns}$ for particles incident along the diagonal of the 2×2 pixel matrix. The first observation is that for deep pwell size $< 3 \mu\text{m}$, the charge collection after 5 ns is always above 99%. The second observation is that even with a deep pwell size of $3 \mu\text{m}$, the charge collection still reaches 90% after 5 ns. This feature of fast and uniform responses motivates further studies towards the integration of fast monolithic pixel designs for applications that require fast timing capabilities.

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4 CONCLUSION

The first engineering run of the ARCADIA main demonstrator is currently in production. The preparations have been accompanied by a large simulation campaign to study possible improvements of the pixel designs in order to decrease the pixel capacitance and optimize the charge collection. This campaign included first tests of radiation tolerance, using the latest radiation damage models, and has investigated in detail the impact of surface charges on the electrical properties. The capacitance of the selected designs is summarized in **Figure 13A** and is shown before and after a dose of 10 krad is applied. Without surface damage, all pixels feature a single-pixel capacitance $< 3 \text{ fF}$.

The charge collection efficiencies for the fastest designs are shown in **Figure 13B**, for central (straight) and corner (dashed) hits. The times for 99% CC are summarized in **Table 2**.

These studies led to the choice of a few different designs of pixels with $10/25/50 \mu\text{m}$ pitch that will be realized in a number of test-structures, such as matrices of 1×1 and $2 \times 2 \text{ mm}^2$. These structures will allow a validation of the physics models used in the simulation and will be characterized using, besides basic IV and CV measurements, radioactive sources and a laser for e/h pair generation.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

TC contributed with TCAD simulations. LD contributed to the development of the software to analyze the simulation data. G-FB contributed to discussions and help in the implementation of the radiation damage models in TCAD. LP contributed with computing resources, discussions, and simulations. All authors reviewed the text of the paper. The manuscript was written by CN.

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